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Design of a Temperature-Aware Voltage Generator for 2-Bit Read Operation in STT-MRAM Based SIMPLY Architecture

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***Abstract*—This paper investigates the reliability of the 2-bit read operation under temperature variations in the Smart Material Implication (SIMPLY) Logic-in-Memory (LIM) scheme when implemented within a Spin-Transfer Torque Magnetic Random-Access Memory (STT-MRAM). To be executed, such an operation requires the generation of a proper reference voltage (V_{REF}). As a result of our study, such a V_{REF} must take a proportional to absolute temperature (PTAT) behavior to alleviate the detrimental temperature effect on the bit error rate. Accordingly, starting from a prior art subthreshold two-transistor (2T) reference circuit, a V_{REF} generator employing an 18T topology was designed in the adopted 65-nm CMOS technology and its effect on the reliability of the 2-bit read operation was evaluated across temperatures.**

Keywords*—SIMPLY, STT-MRAM, temperature variations, voltage reference, read operation.

I. INTRODUCTION

The Smart Material Implication (SIMPLY) logic is a Logic-in-Memory (LIM) solution based on non-volatile resistive memory devices, which has been recently proposed to overcome the limitations of the conventional IMPLY scheme [1]-[7]. Among these ones, the degradation of the logic states of the memristive devices and the very narrow window for the choice of voltages to be applied for proper operation [4]-[7]. The basic scheme of the SIMPLY cell, when implemented with Spin-Transfer Torque Magnetic Random-Access Memory (STT-MRAM) devices, is depicted in Fig. 1(a) along with the truth table of the IMPLY operation. Along with the FALSE operation the latter forms a computationally complete logic basis [3]. The SIMPLY cell includes two STT-Magnetic Tunnel Junction (STT-MTJ) devices (P and Q), a tail transistor M_T (instead of a resistor as in [6], [7]), a voltage generator, a comparator and a control logic block.

The structure of the STT-MTJ is detailed in Fig. 1(b), consisting of three layers, i.e., a thin MgO oxide between two CoFeB ferromagnetic layers. The reference layer (RL) has fixed magnetization orientation, whereas the free layer (FL) has variable magnetization orientation. The state of this device and hence the associated resistance is determined by the relative magnetization orientation of the FL with respect to the RL: parallel or antiparallel, respectively corresponding to low resistance (R_L) and high resistance (R_H), here bit 1 and bit 0, whose difference is given by the tunnel magnetoresistance (TMR) ratio. The switching from one state to the opposite is performed by applying a proper current through the device [8].

Within the SIMPLY scheme, the control logic drives the top electrodes of the two MTJs with appropriate voltages (V_P and V_Q). These voltages are set depending on the specific operation and on the output of the comparator, whose inputs are driven by the voltage V_N developed across the transistor M_T and a reference voltage V_{REF} provided by the voltage generator. The inputs of the IMPLY operation are the initially stored states of P and Q, while the output is the state of Q after processing (Q'). According to the truth table of Fig. 1(a), such an operation requires that P keeps its state regardless of the input combination, whereas Q must switch from 0 to 1 only when P=Q=0. In the SIMPLY cell this is achieved by performing the operation in two steps, as described in Fig. 1(c). The first one consists of a preliminary 2-bit read operation by applying a voltage pulse with amplitude V_{READ} and width t_{READ} on both MTJs (as well as a proper voltage V_G on the gate of M_T) and then comparing the V_N with the V_{REF} through the comparator. This allows distinguishing the input combination P=Q=0 from the others. Accordingly, the second step involves a set operation on Q (i.e., 0→1 switching by applying a voltage pulse with proper amplitude V_{SET} and width t_{SET}) only when the input combination P=Q=0 is

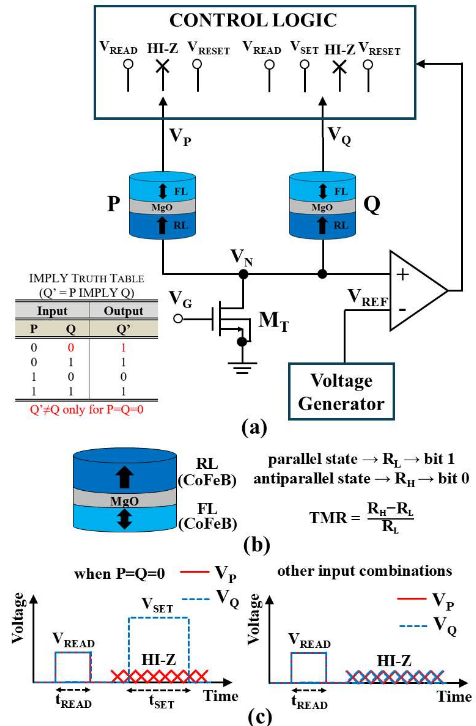

Fig. 1. (a) Scheme of the STT-MRAM based SIMPLY cell along with the truth table of the IMPLY logic operation. (b) Detail of the STT-MRAM device with its resistive states. (c) Time diagram of applied voltage pulses to execute the IMPLY operation within the SIMPLY cell.

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detected during the preliminary operation. Conversely, for the other input combinations the control logic forces the top electrodes of both MTJs to the high impedance (HI-Z) state, thus ensuring significant energy saving [4]-[7].

As proven in our previous studies [6], [7], the reliability of the IMPLY operation when performed within the STT-MRAM based SIMPLY scheme is mainly affected by the preliminary 2-bit read operation. This comes from the relatively narrow memory window provided by MTJs. Taking this into account, this work was focused on investigating the reliability of the 2-bit read operation under temperature variations. First, we evaluated the required V_{REF} to keep the bit error rate (BER) as low as possible across temperatures, while also accounting for the effect of the V_{REF} variability. Then, a voltage generator relying on an 18-transistor (18T) topology was designed to track the proportional to absolute temperature (PTAT) behavior found in our analysis. Our study was performed through simulations into Cadence Virtuoso environment based on a Verilog-A code [8] to model a 30-nm STT-MTJ device (whose characteristics are better detailed in [6], [7]) including the effect of process, voltage and temperature variations, and a 65-nm commercial CMOS technology. Electrical results were then exploited for analytical estimation of the BER and the required V_{REF}.

II. BER and V_{REF} Estimation Across Temperatures

For given voltage and temperature conditions, the reliability of the 2-bit read operation is affected by the effect of process variations on the MTJs, the transistor M_T, the V_{REF} generator and the comparator. More specifically, the BER for the X-th input combination (BER_X) is quantified by the corresponding read margin (RM_X), whose mean ($\mu_{RM,X}$) and standard deviation ($\sigma_{RM,X}$) depend on the V_N, the V_{REF} and the comparator input offset V_{OS} as given by [9], [10]

$$\mu_{RM,X} = \left|\mu_{V_{REF}} - \mu_{V_{N,X}}\right| \quad (1)$$

$$\sigma_{RM,X} = \sqrt{\sigma_{V_{N,X}}{}^2 + \sigma_{V_{REF}}{}^2 + \sigma_{V_{OS}}{}^2} \quad (2)$$

since the V_{OS} is with zero mean and the variations in V_N, V_{REF} and V_{OS} are independent. Assuming the RM Gaussian distributed, the BER_X can be then expressed as [9], [10]

$$BER_X = CDF_{Normal}\left(-\frac{1}{\sigma_{RM,X}/\mu_{RM,X}}\right) \quad (3)$$

The overall BER is typically defined by the worst-case value (i.e., the largest) amongst the different input combinations. Therefore, the minimum or optimal BER (BER_{opt}) is achieved when V_{REF} is chosen to make the BER for the input combinations P=Q=0 and P≠Q equal, i.e., $BER_{opt} = BER_{P=Q=0} = BER_{P\neq Q}$ since $\sigma_{RM,P=Q=0}/\mu_{RM,P=Q=0} = \sigma_{RM,P\neq Q}/\mu_{RM,P\neq Q}$. Such a V_{REF} value (i.e., $V_{REF,opt}$) is given by [9], [10]

$$V_{REF,opt} = \mu_{V_{N,P=Q=0}} + \sigma_{RM,P=Q=0}\frac{\mu_{V_{N,P\neq Q}} - \mu_{V_{N,P=Q=0}}}{\sigma_{RM,P=Q=0} + \sigma_{RM,P\neq Q}} \quad (4)$$

It is worth pointing out that in this study the comparator was considered ideal, thus not affecting the BER (i.e., $\sigma_{V_{OS}} = 0$).

Fig. 2(a)-(b) report the simulation results obtained at room temperature (T = 300 K) in terms of V_N distributions for the different input combinations, along with the estimation of $V_{REF,opt}$ and BER_{opt} according to (1)-(4) while neglecting the effect of V_{REF} variability (i.e., $\sigma_{V_{REF}} = 0$). The data refer to 1k-run Monte Carlo simulations with the transistor M_T consisting of a regular threshold voltage (RVT) device with size equal to $W_T/L_T = 1\mu m/3\mu m$ [11], $V_{READ} = 0.5$ V and $V_G = 1.1$ V. Such voltages were properly set to keep the read disturbance rate (RDR), i.e., the probability of unintentionally switching the stored data during the read operation, sufficiently low for P=Q=0 (i.e., the worst case) assuming $t_{READ} = 10$ ns [7], as well as to reach a sufficiently large RM. From Fig. 2(a), the achieved nominal RM (RM_{nom}) as given by the difference between the mean values of V_N distributions for the cases P≠Q and P=Q=0 is 63.7 mV. From Fig. 2(b), the $V_{REF,opt}$ is 298.2 mV, which leads to a BER_{opt} on the order of 6.6×10^{-5}.

Such an analysis was repeated across temperatures (from 275 K up to 350 K), while also including the effect of V_{REF} variability in (2)-(4) for $\sigma_{V_{REF}}$ ranging from 0 up to 5 mV. Obtained results are summarized in Fig. 3(a)-(d). More specifically, Fig. 3(a) shows the RM_{nom} vs T, which exhibits a decreasing trend with increasing temperature. This is ascribed to the narrowing of the memory window in the STT-MTJ devices for higher temperature, owing to the corresponding decrease of the TMR ratio [7]. As the RM_{nom}, the standard deviation of the V_N shows a decreasing trend with T in Fig. 3(b). Then, Fig. 3(c) shows the estimated $V_{REF,opt}$ across temperatures for different $\sigma_{V_{REF}}$ values as given by (4). Here, data prove that the voltage generator (whose design is addressed in the next section) must generate a PTAT V_{REF} with a temperature coefficient (TC) in the order of about 1900 ppm/°C to mitigate the temperature effect on the reliability of the 2-bit read operation. As a further result, the required $V_{REF,opt}$ is quite independent from $\sigma_{V_{REF}}$ within the considered range for the V_{REF} variability. Fig. 3(d) shows the BER_{opt} vs T

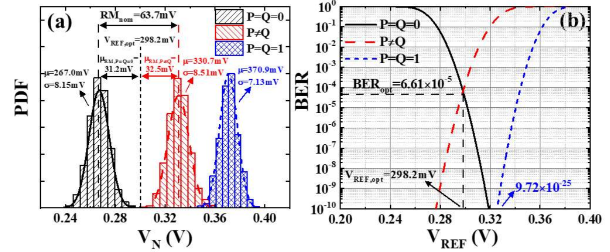

Fig. 2. Simulation results (1k-run Monte Carlo) at T = 300 K related to the 2-bit read operation within the SIMPLY architecture with transistor M_T size equal to $W_T/L_T = 1\mu m/3\mu m$, $V_{READ} = 0.5$ V, $V_G = 1.1$ V and assuming ideal voltage generator and comparator (i.e., $\sigma_{V_{REF}} = \sigma_{V_{OS}} = 0$): (a) V_N statistical distributions for the different input combinations under process variations, (b) BER vs V_{REF} for the estimation of $V_{REF,opt}$ and BER_{opt}.

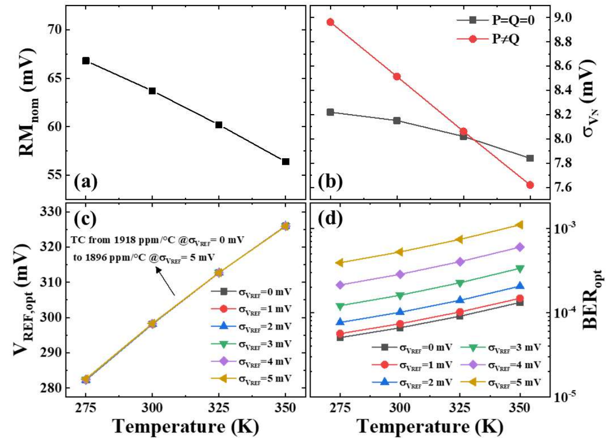

Fig. 3. Simulation results (1k-run Monte Carlo) across temperatures related to the 2-bit read operation within the SIMPLY architecture with transistor M_T size equal to $W_T/L_T = 1\mu m/3\mu m$, $V_{READ} = 0.5$ V, $V_G = 1.1$ V and assuming ideal comparator ($\sigma_{V_{OS}} = 0$): (a) nominal RM, (b) V_N standard deviation for P=Q=0 and P≠Q input combinations, (c) $V_{REF,opt}$ and (d) BER_{opt} for different $\sigma_{V_{REF}}$ values.

corresponding to $V_{REF,opt}$ values reported in Fig. 3(c). From this figure, the BER_{opt} shows a degradation for higher temperature. This is because the reduction in the RM_{nom} at high temperature is more significant than the decrease in the σ_{VN}. Moreover, the BER_{opt} expectedly increases for higher σ_{VREF}, ranging from 5.1×10^{-5} up to 1.3×10^{-4} for $\sigma_{VREF} = 0$ and from 3.9×10^{-4} up to 1.1×10^{-3} for $\sigma_{VREF} = 5$ mV.

III. PTAT Voltage Generator

The starting point for the design of the PTAT voltage generator was the subthreshold 2T reference circuit proposed in [12], [13], whose scheme is depicted in Fig. 4(a). It consists of a native (NVT) NMOS transistor M_1 with its gate grounded (i.e., operating in reverse gate biasing) connected to a diode-connected high threshold voltage (HVT) NMOS transistor M_2. As a consequence, the generated V_{REF} is mainly determined by the difference in the threshold voltage (V_{TH}) of the two transistors. Taking into account the bias and temperature dependence of the V_{TH} and assuming both transistors operating in subthreshold regime, the V_{REF} of the 2T circuit can be expressed as

$$V_{REF} = \frac{n_1 V_{TH0,2} - n_2 V_{TH0,1} + n_2 \lambda_{D1} V_{DD}}{n_2(1+\lambda_{D1}+\lambda_{B1}) + n_1(1+\lambda_{D2})} + \frac{n_1 n_2 V_T \ln\left(\frac{I_{0,1} W_1 L_2}{I_{0,2} L_1 W_2}\right) + (n_2 k_{T1} - n_1 k_{T2})(T - T_0)}{n_2(1+\lambda_{D1}+\lambda_{B1}) + n_1(1+\lambda_{D2})} \quad (5)$$

where n is the subthreshold slope factor, V_{TH0} the V_{TH} at zero bias and $T = T_0$, λ_D is the drain-induced barrier lowering coefficient, λ_B is the body coefficient, V_{DD} the supply voltage, $V_T = k_B T/q$ the thermal voltage with k_B being the Boltzmann constant and q the elementary charge, I_0 the intrinsic subthreshold current, and k_T the V_{TH} temperature coefficient.

With the aim of keeping the line sensitivity (LS) of the circuit as low as possible, i.e., improving its robustness against V_{DD} variations, here we propose a 4T topological variant, as shown in Fig. 4(b). More specifically, by following the approach proposed in [14], two reverse-gate biased transistors (i.e., whose gate is connected to the source of the underlying transistor) with same flavor and size as M_1 were cascaded on the top part of the circuit. This allows better shielding the V_{REF} from V_{DD} variations. The benefit of the 4T topology in terms of LS can be appreciated in Fig. 4(c), which reports the V_{REF} vs V_{DD} at 300 K for the two circuits while using the same transistor size, i.e., $W_1 = W_{1,x} = W_2 = L_1 = L_{1,x} = L_2 = 1$ μm where x = 1, 2, 3 in the 4T circuit. From this figure, the LS of the 4T circuit is more than halved compared to its 2T counterpart. The same figure highlights that the 4T topology has no practical impact on the minimum operating voltage ($V_{DD,min}$), as well as on the TC of the V_{REF} as shown in Fig. 4(d) reporting the V_{REF} vs T at $V_{DD} = 1.2$ V for the two circuits.

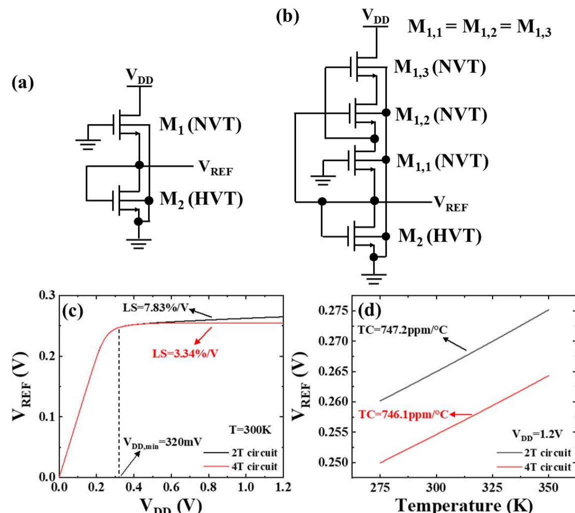

Fig. 4. (a) Scheme of the prior art 2T reference circuit [10], [11]. (b) Scheme of the 4T variant. (c) V_{REF} vs V_{DD} at T = 300 K and (d) V_{REF} vs T at V_{DD} = 1.2 V for the 2T and 4T circuits with same transistor size (i.e., $W_1 = W_{1,x} = W_2 = L_1 = L_{1,x} = L_2 = 1$ μm where x = 1, 2, 3 in the 4T circuit).

To find out a strategy aiming at enhancing the PTAT behavior of the generated V_{REF}, it is useful to derive the temperature dependence of the V_{REF} from (5), thus obtaining

$$\frac{\partial V_{REF}}{\partial T} = \frac{(n_2 K_{T1} - n_1 K_{T2})}{n_2(1+\lambda_{D1}+\lambda_{B1}) + n_1(1+\lambda_{D2})} + \frac{n_1 n_2 (k_B/q) \ln\left(\frac{I_{0,1} W_1 L_2}{I_{0,2} L_1 W_2}\right)}{n_2(1+\lambda_{D1}+\lambda_{B1}) + n_1(1+\lambda_{D2})} \quad (6)$$

From the second term of (6), we can observe that the transistor sizing has clear impact on the TC. In particular, to increase the TC, we could set $W_1 >> W_2$ and/or $L_2 >> L_1$. Between these two options, acting on the L is more effective considering that, unlike W, L also strongly influences both λ_D and k_T. Taking this into account, L was used as a tuning parameter to get closer to the target TC for the V_{REF}, i.e., about 1900 ppm/°C as in the previous section. At the same time, W was exploited to track the desired V_{REF} values at different temperatures, as well as to keep the $\sigma_{V_{REF}}$ as low as possible.

The effect of the L on the TC can be appreciated in Fig. 5(a). The latter illustrates the color map of the TC as a function of the L of the transistors ranging from 1 μm up to 20 μm (i.e., the maximum value allowed in the adopted CMOS technology) in the 4T circuit with $V_{DD} = 1.2$ V and $W_{1,x} = W_2 = 1$ μm. According to (6), the highest TC (around 1200 ppm/°C) is achieved with $L_2 = 20$ μm and $L_{1,x} = 1$ μm. However, this TC is well below the target value of about 1900 ppm/°C. In order to overcome such technological limitation, an additional circuit variant was introduced. This consists of

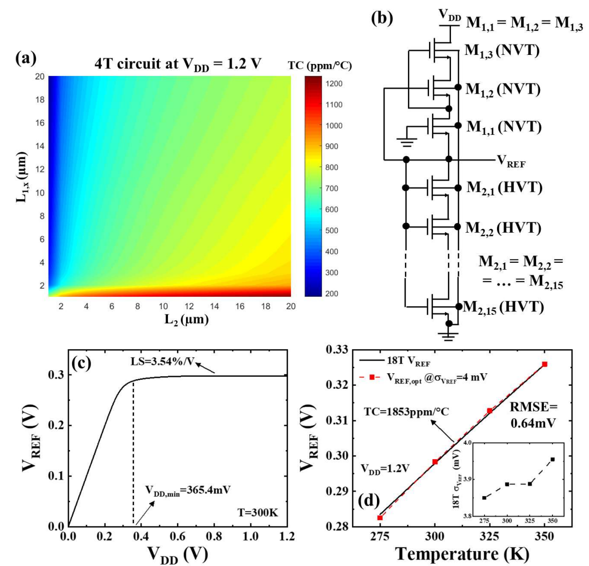

Fig. 5. (a) TC as a function of $L_{1,x}$ and L_2 in the 4T circuit with V_{DD} = 1.2 V and $W_{1,x} = W_2 = 1$ μm. (b) Scheme of the designed 18T PTAT voltage generator with $L_{1,x} = 1$ μm, $W_{1,x} = 100\times120.7$ μm, $L_{2,y} = 20$ μm, $W_{2,y} = 100\times269.8$ μm where x = 1, 2, 3 and y = 1, 2,…, 15. (c) V_{REF} vs V_{DD} at T = 300 K in the 18T circuit. (d) V_{REF} vs T at V_{DD} = 1.2 V in the 18T circuit and comparison with the estimated $V_{REF,opt}$ for σ_{VREF} = 4 mV (in the inset standard deviation of the V_{REF} as given by 1k-run Monte Carlo simulations).

stacking more transistors (same flavor and size as M_2) in the bottom part of the circuit, whose gates are connected to each other, as shown in Fig. 5(b). This allows obtaining an equivalent diode-connected transistor with an effective L greater than 20 µm. More specifically, to reach a TC close to the target value of 1900 ppm/°C, 15 transistors were stacked in the bottom subcircuit, thus leading to a PTAT voltage generator design employing an 18T scheme (see Fig. 5(b)). Within this circuit, the transistor were sized as follows: $L_{1,x}$ = 1 µm, $W_{1,x}$ = 100×120.7 µm, $L_{2,y}$ = 20 µm, $W_{2,y}$ = 100×269.8 µm where x = 1, 2, 3 and y = 1, 2,…, 15. Fig. 5(c) shows the generated V_{REF} vs V_{DD} at 300 K for the 18T circuit, whereas Fig. 5(d) reports the V_{REF} across temperatures at V_{DD} = 1.2 V. The latter is compared with the previously estimated $V_{REF,opt}$ for σ_{VREF} = 4 mV, i.e., a V_{REF} variability close to that obtained in the designed circuit, as shown in the inset of Fig. 5(d). From this comparison, the V_{REF} provided by the 18T circuit well tracks the estimated $V_{REF,opt}$ with a root mean square error (RMSE) of 0.64 mV across the considered temperature range.

The outcomes of the designed voltage generator were finally exploited to evaluate the BER of the 2-bit read operation within the SIMPLY scheme, as done in the previous section. In this regard, Fig. 6 reports the worst-case BER (i.e., between P=Q=0 and P≠Q cases) across temperatures when the PTAT V_{REF} is provided by the 18T circuit of Fig. 5(b). Achieved results show a BER ranging from 2.8×10^{-4} at 275 K up to 6.4×10^{-4} at 350 K. In the same figure, these BER data are compared with those obtained in other two cases: (*i*) the BER_{opt} when using the estimated PTAT $V_{REF,opt}$ for σ_{VREF} = 4 mV, (*ii*) the worst-case BER when using an ideally stable V_{REF} across temperatures (i.e., with TC = 0) at the $V_{REF,opt}$ value estimated at 300 K for σ_{VREF} = 4 mV. The comparison against (*i*) again confirms the good tracking of the estimated PTAT $V_{REF,opt}$ achieved through the V_{REF} generated by the designed 18T circuit. On the other hand, from the comparison with BER data achieved with a constant V_{REF} across temperatures, we can appreciate how crucial this tracking is to avoid a BER degradation up to unacceptable values, i.e., higher than 10^{-1}.

IV. Conclusion

In this work, we analyzed the reliability of the 2-bit read operation across temperatures within the STT-MRAM based SIMPLY architecture. The study employed simulations assisted by an analytical framework for the estimation of the required V_{REF} and corresponding BER, considering the effect of process variability. We found that the V_{REF} must assume a PTAT behavior to alleviate the BER degradation under temperature variations. Then, starting from a prior art 2T circuit, we designed a voltage generator to provide such PTAT V_{REF}, as well as to keep its variability sufficiently low. This was achieved by an 18T topology and proper transistor sizing at the cost of larger area. However, the area overhead is mitigated within a memory array since the voltage generator is shared among cells belonging to same row or column.

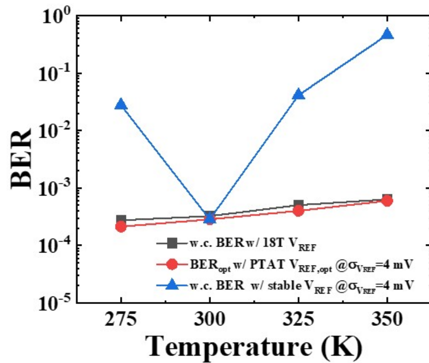

Fig. 6. Comparison of BER results (from 1k-run Monte Carlo simulations) under temperature variations related to the 2-bit read operation within the SIMPLY architecture with transistor M_T size equal to W_T/L_T = 1µm/3µm, V_{READ} = 0.5 V, V_G = 1.1 V and assuming ideal comparator (σ_{VOS} = 0): worst-case BER with the PTAT V_{REF} provided by the designed 18T voltage generator, BER_{opt} with the estimated PTAT $V_{REF,opt}$ for σ_{VREF} = 4 mV, and worst-case BER with an ideally stable V_{REF} at the $V_{REF,opt}$ value estimated at 300 K for σ_{VREF} = 4 mV.

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