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Generazione di frequenza per applicazioni a onde millimetriche in tecnologia CMOS.

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...to those which I have devoted little time.

Contents

Abstract

In the near future new electronic applications, operating in the millimeter wave band ($30GHz - 300GHz$), will allow us wireless communications with unprecedented speed, radars to improve safety in the automotive field and new scanners for image reconstruction, useful for diagnostic, industrial and security systems. For a widespread diffusion in the mass market of these applications, as it has been for mobile phones and personal computers, it is required that electronic circuits are made in CMOS technology. These technologies bring benefits in terms of cost but, on the other hand, introduce several challenges in the design of circuits with adequate performances.

The first part of the thesis presents an overview of future applications at millimeter-wave (mm-Waves). These are divided into three classes: wireless communications, automotive radar and systems for mm-Wave image reconstruction. The design and realization of circuits with CMOS technology is presently still very difficult. The thesis focuses on the challenges related to the mm-Waves frequency generation. The oscillator circuits are fundamental in any transceiver and there are still several unresolved issues.

The quadrature oscillators, that are fundamental in direct conversion receivers, present particular difficulties due to the trade-offs between power consumption, spectral purity, phase error and tuning range. These trade-offs are emphasized at mm-Waves. During the PhD it has been proposed a new circuit solution which is based on a ring of two LC-VCOs with resonators magnetically coupled to each other. The circuit has an oscillation frequency dependent on passive components only and presents a lower phase noise, if compared with the state of the art, and good quadrature accuracy. Prototypes, realized in $65 - nm$ CMOS, show $56 - 60.4GHz$ tunable oscillation frequency, phase noise better than $-95dBc/Hz$ at $1 - MHz$ offset in the tuning range, 1.5^o maximum phase error while consuming $22mA$ from a $1 - V$ supply.

In the continuous research high performance oscillators at higher and higher frequencies it has been studied, as part of the doctorate,

the use of a frequency multiplier. Using a multiplier by two (doubler) connected in cascade, the VCO (voltage controller oscillator) can be designed at half the required output frequency getting benefits of passive components (especially varactors) with higher quality factor. This allows a larger frequency tuning range and lower power consumption for given phase noise. In the thesis it is described a new circuit solution of the frequency doubler. This solution exploits the injection locking technique, and it is based on a Pierce oscillator synchronized by a pair of transistors in push-push configuration. The results achieved are supported by two test chips realized in $65nm$ CMOS technology. In a first prototype the doubler is driven by an external source. The experimental results prove an operation bandwidth from $106GHz$ to $128GHz$ with a peak voltage swing on each output of $330mV$. In the second prototype the doubler is driven by an integrated LC-tank VCO, operating at half the output frequency. This has allowed to demonstrate an exceptional 13.1% frequency tuning range around $115GHz$. The tuning range is about 4 times higher than the state of the art.

A summary of each thesis chapter is reported below:
in **Chapter 1** a general overview of mm-Waves systems and applications will be discussed. Advantages of higher operation frequency are presented, along with mm-Wave channel propagation characteristics and the main challenges in mm-Waves CMOS design.

Chapter 2 deals with the frequency generation requirements, considering advantages and disadvantages coming from different receiver architectures. In this chapter an overview of state of the art mm-Waves receivers is also proposed.

In **Chapter 3** the issue of quadrature signals generation at 60GHz is faced. A new circuit topology will be presented and experimental results will be discussed to demonstrate the possibility to integrate into a complete direct conversion receiver the described QVCO. Compared to recently reported literature, the proposed solution demonstrates a very low $1/f^3$ corner frequency and an average improvement of $5dB$ in the phase noise figure of merit.

In **Chapter 4** the benefit of introduction of frequency doubler will be presented. Different frequency multiplier topologies operating at mm-Waves, available on the literature, are described. The new circuit solution improving the state of the art performances is than shown. Two different prototype versions of the doubler will be presented,. When driven by a half-frequency VCO, the complete frequency generation circuit demonstrates an outstanding 13.1% tuning range around $115GHz$.

At the end of the thesis, conclusions, review the presented scientific achievements and list the associated scientific publications.

Chapter 1

Millimeter Wave Applications

Millimeter waves are electromagnetic waves just like microwaves, radio waves, and visible and infrared light. Millimeter waves lie in the frequency region from $30 - 300GHz$ (wavelength: $1 - 10mm$) and receive their name because their wavelengths are of the millimeter order as shown in figure 1.1. In 1946, the most unique feature of mm-waves, oxygen absorption at $60GHz$, was reported by Becker [1], which results in the rapid attenuation of electromagnetic waves in the air. Although the oxygen absorption makes long-distance wireless communication difficult. Wireless communication, automotive radar, imaging system are highlights of a growing list of applications at mm-wave frequencies. The valuable functions represented by these applications are causing excitement in the engineering and business offices of companies involved in mm-wave components, assemblies and test equipment. As development continues and costs come down, mm-waves will become a well-used portion of the electromagnetic spectrum. In this chapter the main applications at millimeter waves are described, a special attention will be paid to the various frequency bands occupied by different applications.

1.1 Wireless Communication

The most promising mm-waves applications is very high data rate links and personal area networking [2]. Such a wide unlicensed bandwidth represents the ideal candidate to high bit-rate data transmission as demonstrated by the Shannon's theorem [3]:

$$C = BW \log_2(1 + SNR) \tag{1.1}$$

Equation (1.1) represents the maximum data-rate of a communication channel, known as channel capacity, C. It is related to the bandwidth

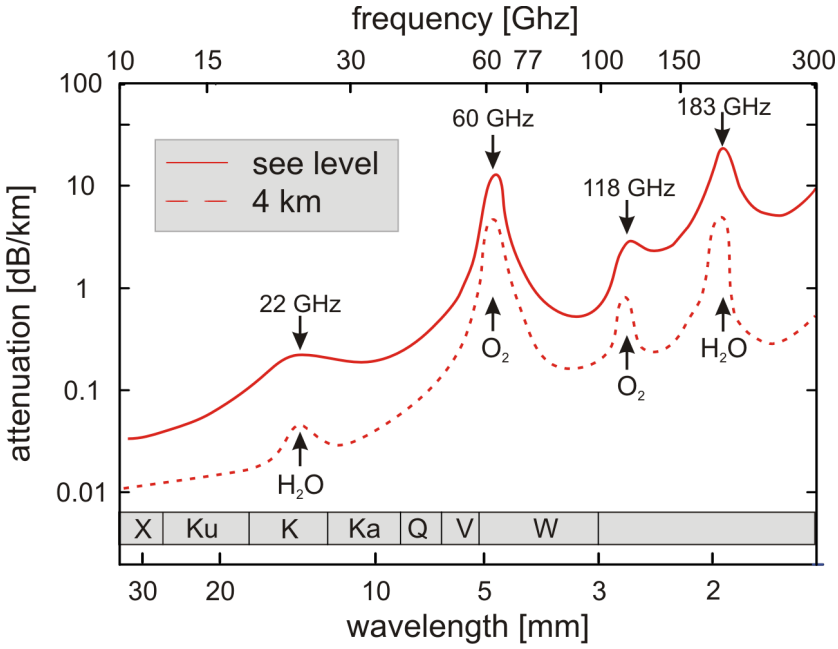

Figure 1.1: Features of millimeter waves band.

of the channel, BW, and the signal-to-noise ratio, SNR. The way to increase the communication data rate is to by using more bandwidth. $60GHz$ technology offers advantages over existing wireless communi-

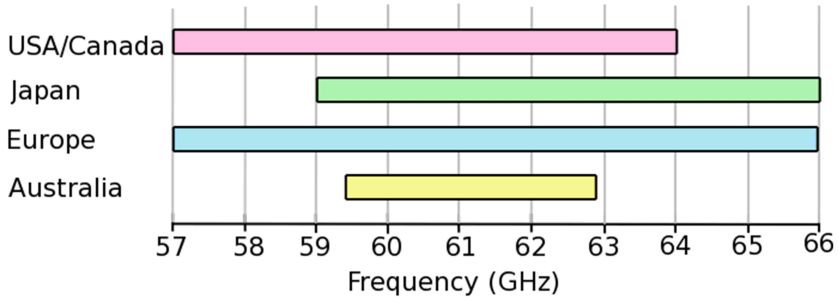

Figure 1.2: The spectrum allocation around the $60GHz$ band for some regions.

cations systems. This is not only true in some Region but also globally as shown in figure 1.2. There is thus great incentive to design wireless systems capable of exploiting this opportunity.

In July 2003, the IEEE $802.15.3$ working group for WPAN began in-

vestigating the use of the $7GHz$ of unlicensed spectrum around $60GHz$ as an alternate physical layer (PHY) to enable very high data-rate applications such as high-speed internet access, streaming content downloads, and wireless data bus for cable replacement. The targeted data-rate for these applications is greater than $2Gb/s$. Although the excessively high path loss at $60GHz$, due to oxygen absorption as shown in figure 1.1, precludes communications over distances greater than a few kms, short-range WPANs actually benefit from the attenuation, which provides extra spatial isolation and higher implicit security. Furthermore, due to the oxygen absorption, the FCC regulations allow for up to $40dBm$ Equivalent Isotropic Radiated Power (EIRP) transmit power, which is significantly higher than what is available for the other WLAN/WPAN standards. The wide bandwidth and high allowable transmit power at $60GHz$ enable multi-Gb/s wireless transmission over typical indoor distances ($\sim\ll 10m$). Moving to higher frequencies also reduces the form factor of the antennas.

Propagation challenges are greater at mm-waves, but are not a significant problem for point-to-point and short range systems. For point-to-point data communications, mm-waves offer an alternative to fiber optics for short-distance links, without the environmental limitations of laser links (rain, snow, fog and haze). The poor wall penetration of mm-waves requires a terminal (wireless transceiver) to be located in each room, but this also allows frequency reuse, or different data streams at each terminal. These special features are excellent starting points of a number of indoor applications, such as:

- cable replacement or uncompressed high definition (HD) video streaming that enables users to wirelessly display content to a remote screen with wired equivalent quality/experience;
- 'Sync and Go' file transfer that enables gigabytes of file transfer in a few seconds;
- wireless docking stations that allow multiple peripherals (including an external monitor) to be connected without the need for frequent plugging and unplugging;

- wireless gigabit Ethernet that permits bidirectional multi-gigabit Ethernet traffic;
- wireless gaming that ensures high-quality performance and low latency for exceptional user experience.

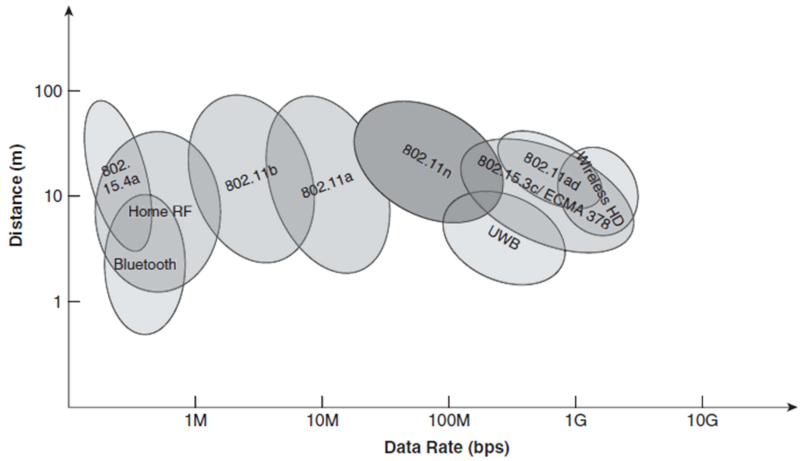

Figure 1.3: Rate versus range different standards.

Despite of the various advantages offered, $60GHz$ based communications suffer a number of critical problems that must be solved for example the standardization.

The figure 1.3 shows the data rates and range requirements for a number of WLAN and WPAN systems. Since there is a need to distinguish between different standards for broader market exploitation, the $60GHz$ related standards are positioned to provide gigabit rates and longer operating range than the UWB systems but shorter than that of IEEE 802.11n systems. Typically, $60GHz$ systems are designed to provide multigigabit data rates with operating range below $20m$ to support various applications. There are currently many standards for $60GHz$ wireless communication[4], including *IEEE 802.15.3c*, *IEEE802.11ad* (a high-speed WLAN network), the *ECMA-387* standard, *WirelessHD*, and the *WiGig* standard. Each standard is formed by a different community of potential users of the technology, such as consumer electronics companies (WirelessHD) versus the PC industry (WiGig). Most of

the standards are focusing on very high speed communication $(15Gb/s)$ to enable wireless HDMI replacement. Unfortunately the process of standardization is highly political and controversial, often to the detriment of the technology and ultimately to the consumers. This was certainly the case for UWB technology and may have contributed to the delay of products and to the eventual downfall of UWB. It is imperative that the same mistakes are not made with $60GHz$. Even though different standards are needed for different applications, interoperability between the standards is key. For instance, a simple single carrier low range link should be the fall-back mode for all the different 60-GHz radios. A single carrier is preferred, even though it may have a shorter range due to multipath effects, because it can be easily integrated into small low-power portable devices. This is in stark contrast to systems using OFDM, which require high power for the ADC and digital baseband processor (FFT operation).

1.2 Automotive Radar

The Federal Communications Commission has allocated two frequency bands, $22-29GHz$ and $76-77GHz$ for cruise control automotive radar applications [5, 6]. In 2004 and 2005, the ECC (Electronic Communications Committee) adopted decisions that regulate the temporary introduction of vehicular using $24GHz$ spectrum in Europe until 1 July 2013 and the unlimited allocation at $79GHz$. Currently, these radar systems are made using $III-V$ semiconductor technology and are only available on luxury cars. Considering the high mortality and injury rates as a result of car accidents using silicon technology to make these radar systems ubiquitous looks quite tempting. Between the frequencies 75 and $100GHz$ the atmospheric absorption by gases is minimal. Specifically at $77GHz$, the atmospheric attenuation is $0.4dB/km$ at sea level. In a typical automotive radar, an Electro-Magnetic impulse is transmitted toward potential targets. The reflected signal reveals information about the shape, distance and speed of the target, based on its shape and reflection time. A series of these radar sensors are embed-

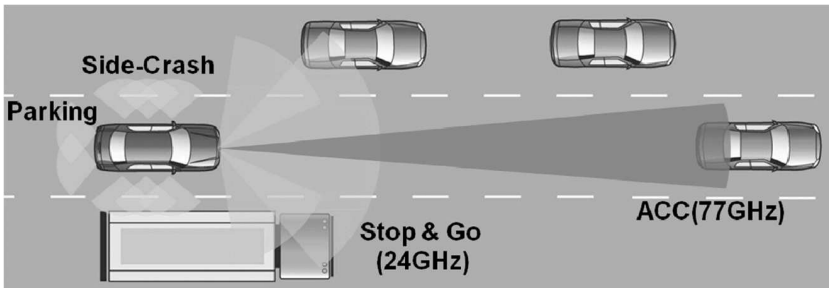

Figure 1.4: Automotive radar systems.

ded all around the vehicle to detect all potential obstacles and hazards. One potential difficulty with radar systems is the ability to discriminate between various signals, scattered from different objects back to the system. This requires sophisticated signal processing schemes and potentially introduces detection errors in the form of false alarm. The reliability of the automotive radar can dramatically increase by spatially scanning the visible field through antenna steering. The usual mechanical ways of steering the antenna is impractical for low cost systems. An alternative cheap solution is using electronic steering in the form of phase array systems [7, 8]. Phase array transmitters can form a narrow beam steered toward intended object in a narrow field of view. A phased array receiver is only sensitive to the reflected signals that arrive at a specific angle that can be electronically controlled. Therefore, phased arrays, also known as electronically scanned arrays or beam-forming arrays, reduce the undesired effect of multiple reflections and interference while allowing for a full spatial coverage. In addition, phased array receivers enhance the radar SNR and hence its range. RF phased arrays have been extensively used in military applications for high resolution ground- and ship-based as well as airborne radars.

1.3 Imaging at MillimeterWaves

Another potential application for mm-wave technology is passive and active imaging. The most attractive feature of millimeter waves, when

compared with optical, infrared, and terahertz waves, is their ability to penetrate obstacles[9]. A spatial resolution higher than that achievable with microwave imaging sensors is possible. Therefore, they can be used under low-visibility conditions such as in fog, rain, dust, or fire, where optical or infrared cameras cannot be used. In figure 1.5 we see the optical and mm-wave image seen from an airplane in good and bad visibility conditions. The mm-wave image is clearly able to penetrate through the fog and rain and provide a clear image. As the radiometric temperatures of an object are different depending on its metallic or dielectric properties (εr) and its temperature, these systems can detect concealed weapons or explosive materials. Consequently, these systems have undergone test installation for use in security cameras at the entrances of airports and buildings. In addition, these sensors are also useful for finding landmines, for offering all-weather vision, for detecting cracks in exterior walls, and for screening people for skin cancer. In security applications, passive (or active) mm-wave images of

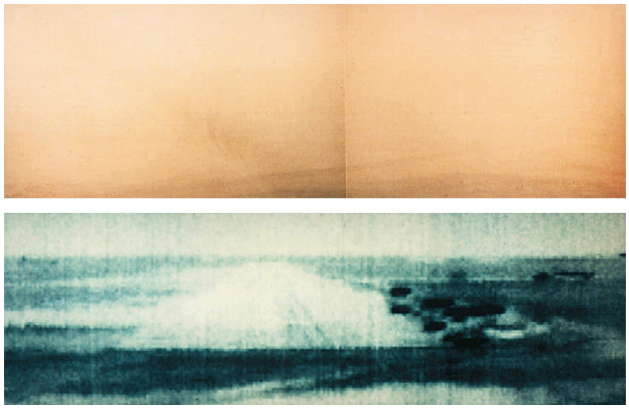

Figure 1.5: Figures show visible images in foggy weather and the corresponding PMMW image

a person can be used to find hidden weapons. The imaging of people in the mm-waves regime produces images that are somewhat eerie, especially when done outdoors. Mm-waves can easily penetrate clothing and hair. The detected mm-wave radiation is a combination of the natural emissions from the body and, what is reflected from the surround-

ings. In figure 1.6 we see that a hidden gun or knife is easily visible due

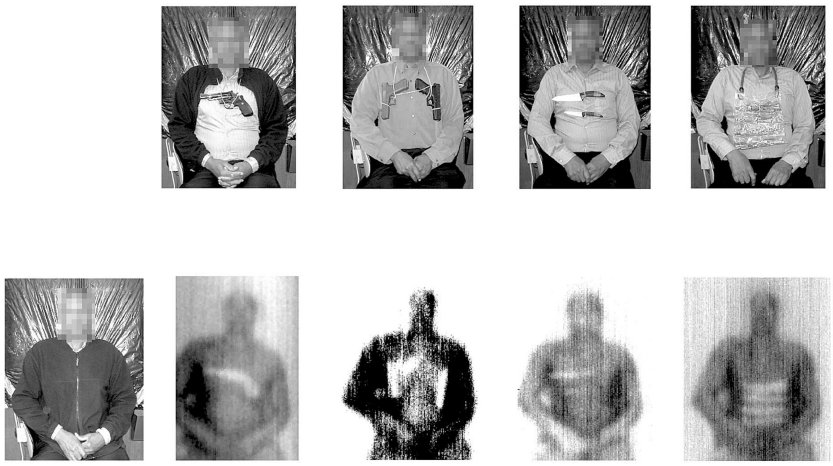

Figure 1.6: Visible (top row) and corresponding PMMW images of an individual with various weapons concealed by the sweatshirt shown in the visible picture at the start of the bottom row.

to the difference in emissivity of the body and the object. While metal objects are easy to detect by other means, non-metallic objects are also visible, which is a great advantage of the technology. Unlike X-ray based imaging systems, which can only be used with limited dosage with living organisms, passive mm-wave (PMMW) imaging does not use any additional radiation than what is naturally present. Even active imaging systems use radiations with milli-eV energies compared to $k - eV$ necessary for X-ray systems. Other emerging applications for mm-wave technology include medical imaging for tumor detection, temperature measurements, blood flow and water/oxygen content measurements.

The detection of objects based on mm-wave radiation or reflection/ absorption can be divided into three separate approaches as shown in figure 1.7 [10], each with a unique set of requirements placed on the mm-wave detector circuitry and its supporting optics. The first approach, commonly named transmissive imaging and depicted in figure 1.7a, is relatively straightforward when compared to other approaches. A target is placed between a transmitter and receiver. The attenuation

or blocking of the target at mm-wave frequencies is then measured at multiple points in space to construct an image. While this is the simplest type of imaging, it inherits a major disadvantage of requiring the system to surround the target for remote security screening and contraband detection. The second approach, shown in figure 1.7b, is to focus the source of mm-wave illumination (transmitter) into a narrow beam, then reflect the signal off the surface of a remote target and return it back to a receiver. This approach is commonly called backscatter or reflective imaging. The reflection coefficient information at different points in space is utilized to create an image. While this is conceptually simple, the signal must travel the path twice (forward and backward) in free-space and makes the link budget more difficult. The third

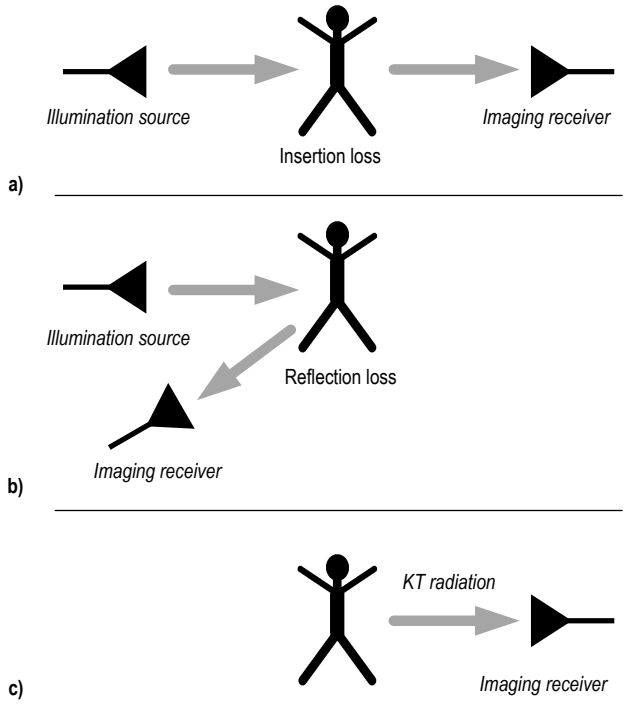

Figure 1.7: a) Transmissive mm-wave imaging system; b) reflective (backscattering) mm-wave imaging system; c) passive mm-wave imaging system.

approach, commonly called ”passive imaging,” is shown in figure 1.7c. It constructs imaging by detecting subjects own blackbody radiation,

without the need of mm-wave radiation sources or any compliance to FCC regulations. That can simplify the system and facilitate its wide applications. However, passive imaging is considered to be the most difficult approach in mm-wave imaging systems because it must detect the emitted thermal noise kT from the target, where k represents the Boltzmann constant and T represents the absolute temperature measured by Kelvin (or K). While the concept seems relatively simple, it is actually quite challenging as the temperature variation across a typical scene (contrast ratio) may vary only by a few K. Since scene content varies by such small temperatures a passive mm-wave imager requires $< 1K$ in temperature resolution to capture usable images for object detection. Imaging receivers can be partitioned into simple detection and pre-amplified detection. Figure 1.8 contains the block diagrams of both a simple detector (a) and a pre-amplified detector (b). The distinction between them where the first gain stage occurs. This is critical as it determines not only the noise performance, but the bandwidth and range of frequencies. Amplifiers at mm-wave frequencies are typically narrowband while nonlinear mixing elements can be quite broadband in nature. In the simple detector a nonlinear element first translates an

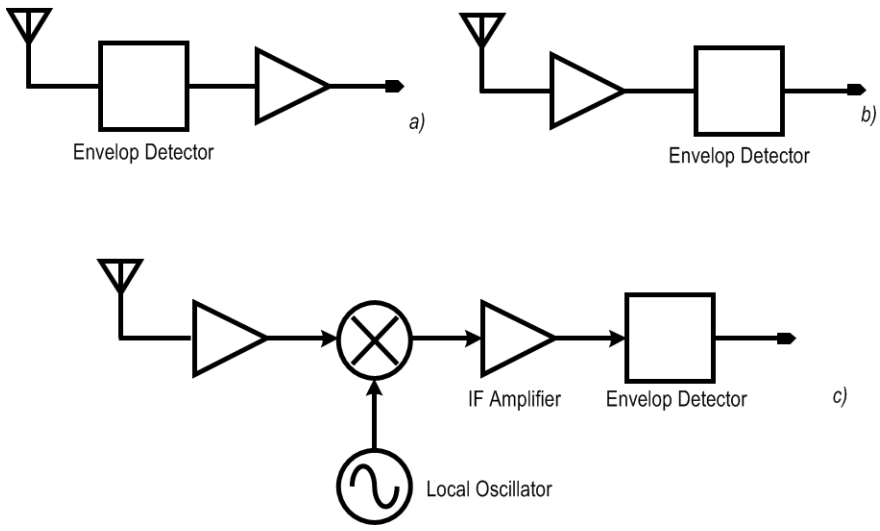

Figure 1.8: a)Simple detector. b) Pre-amplified detector block diagrams. c)Heterodyne receiver.

incoming signal to a very low frequency (near DC) voltage and subsequently amplifies it by a chain of low frequency amplifiers. As the detector has no pre-amplification, the noise equivalent power (NEP) of the detector is typically large. Pre-amplified detectors behave quite differently from simple detectors as their first stage is made of a low noise amplifier (LNA) allowing suppression of noise from following cascaded stages. For this reason, preamplified detectors can achieve much better NEP. In the figure 1.8c is shown an other receiver solution the heterodyne topology. This detection provides the highest sensitivity compared with the other receiver system. It use a mixer, which needs an local oscillator (LO). This system is more complicated because the LO generation presents many difficulties at mm-waves.

1.4 Why CMOS for Millimeter Wave Applications?

From a technology and performance perspective, silicon is not the obvious choice for millimeter-wave systems. Many non-silicon-based $III-V$ technology choices offer higher mobility and an insulating substrate (high Q passives) and, thus, high-frequency operation at moderately short channel lengths. Unfortunately, these technologies are expensive and have low manufacturing yields, thus they offer limited integration possibilities. Furthermore, these processes are not expected to scale in cost. If we assume mm-wave applications will became a high volume market then silicon would be the obvious choice. Moreover, in price-sensitive consumer applications, CMOS is the right choice. The CMOS technology is driven by a mass consumer market for high-speed digital microprocessors whereas specialized technologies are only needed in niche applications where the cost can be justified. For these reasons CMOS technology is a compelling choice, despite the added difficulties in doing mm-wave design in a digital process.

Continuous scaling of the transistor channel length has resulted in raw performance benefits, particularly in the transistor speed, whose f_t

has been pushed above $300GHz$ during last years [11] as shown in figure 1.9, making an all-CMOS solution at very high frequency at least in principle feasible. Nonetheless CMOS scaling poses several challenges to the analog design. First of all, the device output conductance g_0 reduces with scaling, leading to a lower and lower available gain ($g_m/g_0 \simeq 7$ in a $65nm$ technology)[12] as shown in figure 1.9. Moreover,

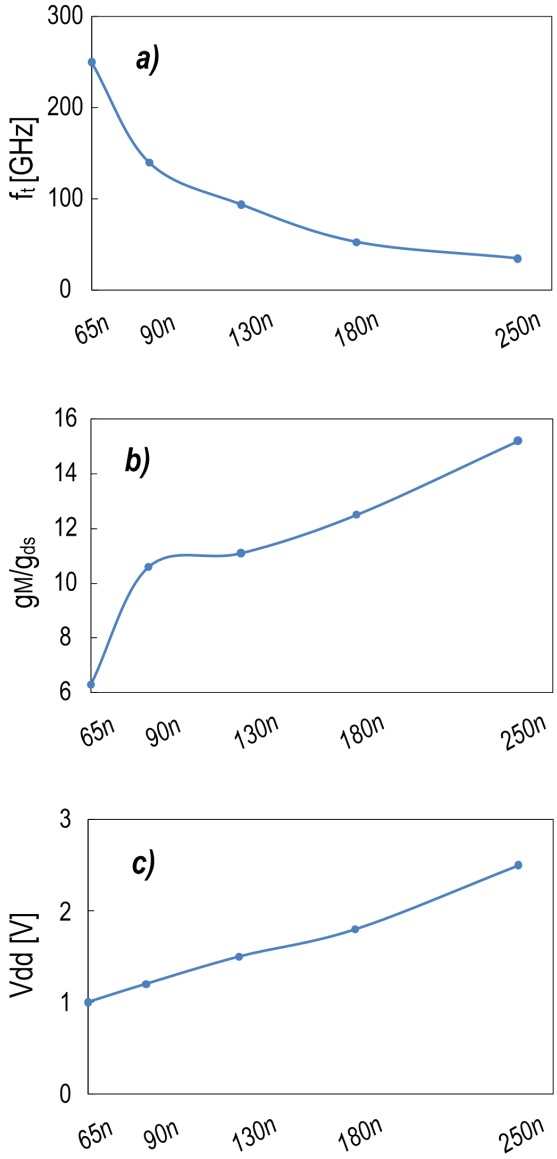

Figure 1.9: a)Scaling f_t, b)Scaling of ratio of g_m and g_{ds}, c)Scaling Vdd.

the continuous voltage supply reduction makes it difficult to stack more than two transistors and the achievable dynamic range of amplifiers is significantly limited. The low voltage supply translates also in a poor output power capability of Power Amplifiers (PA) and poor spectral purity of oscillators. Last but not least, passive components such as inductors and transmission lines are getting even worse with scaling, since there is a strong trend in lowering metal and oxide thicknesses, due to materials and processes constraints. The trend when moving from one CMOS node to the next is the vertical shrink of the BEOL together with the decrease of the metal and dielectric thicknesses and of the metal pitch in order to increase integration density. The increase of the integration scale imposes also the use of a larger number of metal levels and also implies some changes in the nature of the metallic materials used. One can observe that the total height of dielectric is diminishing from one technology node to another, thus increasing the influence of the substrate losses.

In conclusion, the continuous scaling of CMOS technology opens up the possibility of adopting it for emerging applications but seems to bring new and continuing challenges to analog designer in particular for RF and mm-wave systems.

Chapter 2

Transceiver Architecture and LO requirements

In this chapter an overview of the state of the art receiver architectures for mm-waves applications is reported to highlight advantages and disadvantages of different solutions. For millimeter-wave receiver systems, one of the most critical blocks is the frequency synthesizer. At very high frequency, the choice of the architecture becomes closely intertwined with the synthesizer design. For this reason, Local Oscillator (LO) requirements will be analyzed for each architecture. At the end of the chapter the state of art of LO will be dealt.

2.1 Direct-Conversion Receiver

The direct-conversion architecture converts the received RF signals into baseband without any intermediate stage. This architecture is widely used in some wireless applications due to its simplicity. Figure 2.1 shows a block diagram of a direct-conversion receiver. The band pass filter in front of the LNA removes out-of-band interferers and noise. In many cases it can be omitted thanks to the band pass characteristic of antenna and LNA [13]. After filtering and low-noise amplification the RF signal is splitted into two signals, which are directly down-converted to baseband with two RF mixers driven by quadrature LO. The following baseband low-pass filter (LPF) provides anti-aliasing for sampling and channel selection. This architecture is apparently simple and requires few components. In addition, it does not suffer from the image problems that always exist in multi-step frequency conversion architectures. Thus it is easier to have monolithic one-chip integration without the necessity for image reject and intermediate IF filters. This is particularly attractive in mobile applications

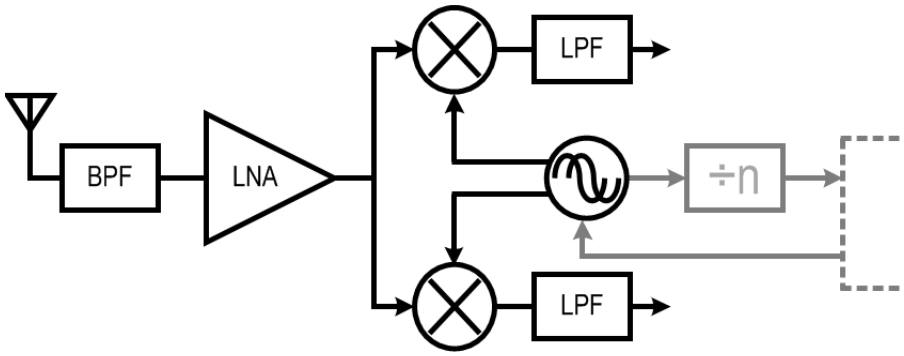

Figure 2.1: Direct-conversion architecture.

where low power consumption is the most critical figure-of-merit. The major drawback of direct-conversion receivers is higher dynamic range requirements in RF components including amplifiers and mixers since RF signals are directly converted into baseband and channel selection is done in baseband. LO self-mixing is serious. It results in DC offset and degraded receiver dynamic range. I/Q mismatch is another issue. It mainly comes from the existing layout tolerance of active and passive elements used in RF components, and becomes larger as operating frequency increases.

At millimeter-wave the direct conversion receivers pose different problems with respect to RF systems. The most challenging aspect is the design of the VCO and the first divider that must operate at very high frequencies while maintaining good power efficiency [14]. It is important to note that the VCO has to generate two different phases in quadrature (I/Q). At RF frequencies the generation of I and Q phases is achieved through a double-frequency oscillator followed by a divider by two. This solution is unfeasible at millimeter-wave. A possible alternative would be to design a quadrature oscillator at the same frequency of the input signal, realized by properly coupling two oscillators together. This configuration has several issues since quadrature operation typically degrades the phase noise considerably. A further issue of the direct conversion architecture is that the VCO and divider have to work at high frequency, the same of input signal. This leads to design diffi-

culties and very large power consumption since degradation of passive components increases with frequency. Another important problem is the LO distribution. The quadrature outputs of the VCO must travel a relatively long path to reach the I/Q mixer cores and to reach the divider core, thus experiencing significant loss and mismatch. With no buffer following the VCO, the loss of these interconnects also degrades the phase noise. One may wonder if these interconnects can be realized as low-loss Transmission lines having a controlled impedance and terminated properly at the destination. Since the characteristic impedance of on-chip T-lines hardly exceeds a few hundred ohms, such an approach would load the VCO with a low resistive component, drastically raising the noise floor or even prohibiting oscillation.

2.2 Super-Heterodyne Receiver

The super-heterodyne architecture, which Armstrong introduced in 1918, has long been a standard choice for wireless receivers due to its capability to provide high selectivity and sensitivity. Basically, it converts received RF signal energy into baseband through several steps, which makes it possible to optimize system parameters at each step. Figure

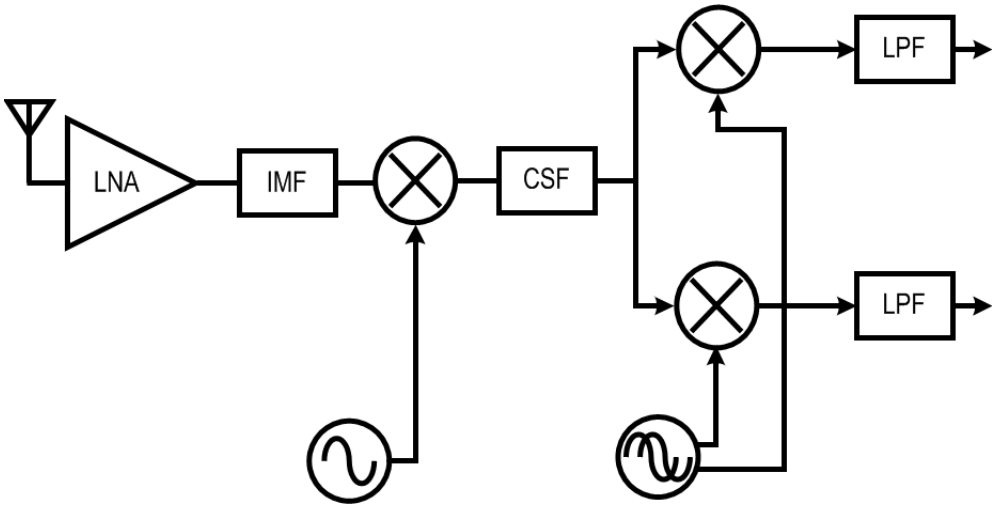

Figure 2.2: Super-Heterodyne architecture.

2.2 shows a block diagram. The filtered in-band signals are amplified by a low-noise amplifier (LNA) while keeping the system noise floor as low as possible. The filter after the LNA suppresses image signals which could be overlapped with wanted signals after mixing. The frequency down-conversion with the first LO moves RF signals down to the intermediate frequency (IF) band. Channel selection is done at the IF stage with the help of highly selective filters, which lessen the dynamic range requirement in the following stages. After splitting into two signals, the IF signals are down-converted into baseband with two mixers and the second quadrature LOs. Due to its superior performance, most millimeter-wave transceivers developed so far are based on the super-heterodyne architecture. Image rejection problems can be alleviated by incorporating high IF of more than a few gigahertz with the frequency selective responses of a Low Noise Amplifier (LNA) without integrating an external image rejection filter. The Local Oscillators of the architecture shown in figure 2.2, work at lower frequency than direct conversion receivers.

In this way generation and distribution of quadrature phases can be simplified. The main drawback of this option, compared to a standard direct conversion receiver, is the necessity of two frequency references. A possible solution to mitigate the receiver complexity and relax the oscillator requirements is the sliding-IF receiver. The block diagram is shown in figure 2.3 where two different LO generation schemes are illustrated. The first down-conversion is realized by a single phase LO signal at $2/3$ of the received frequencies while the second one is obtained by means of quadrature signals at $1/3$ of the receiver signal frequency. In the top block diagram the second quadrature LO is generated by frequency division by two of the high frequency VCO [14]. In the bottom block diagram the situation is symmetrical: the second down-conversion is realized by a quadrature VCO while the LO for the first mixer derives from the frequency doubling of the lower frequency quadrature LO signals [15].

In 2008, Ali Parsa proposed an alternative architecture [16] that is shown in figure 2.4. This configuration, like other superheterodyne

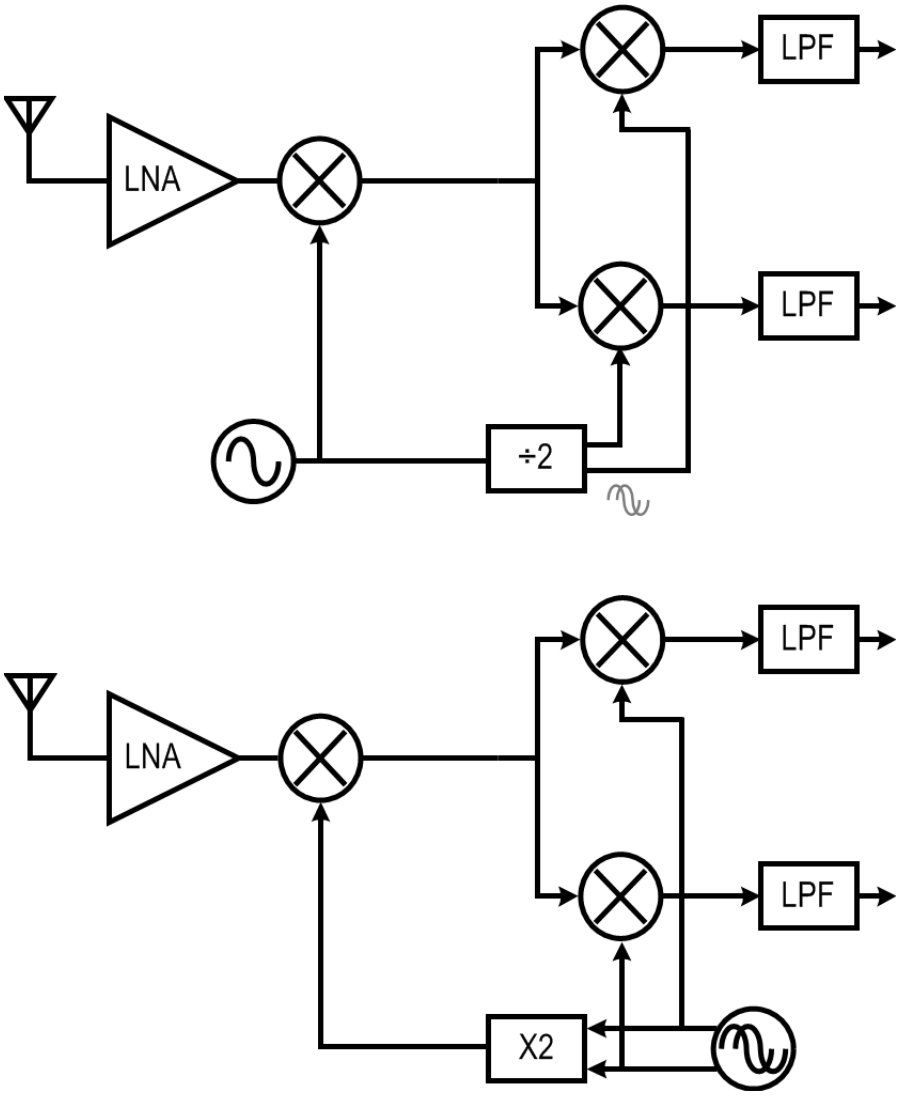

Figure 2.3: Sliding Conversion Receivers.

architectures, allows the frequency down conversion with a LO signal that presents a frequency lower than the input. In this new architecture the input is applied to a LNA. Following the LNA a phase shifter, realized with a polyphase filter, generate In-phase and Quadrature-phase (IQ) versions of the received signal which are then converted to base-band in two steps with a single phase LO at half input frequency. Quadrature LO is not required. With this architecture, the image falls

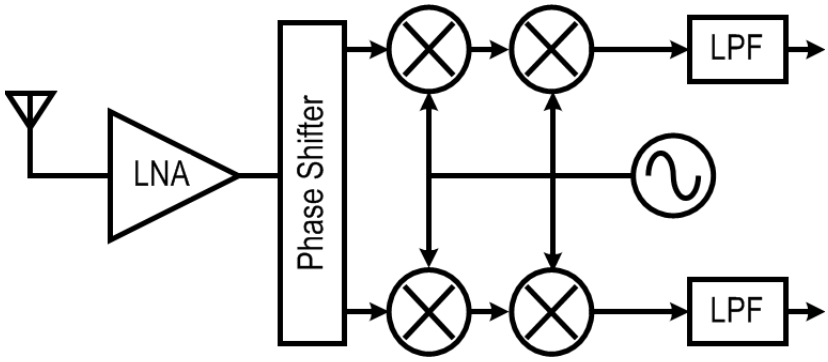

Figure 2.4: Half-RF heterodyne transceiver architecture.

to zero frequency and does not require filtering. The presence of the polyphase filter introduces attenuation (and therefore reduces the performance of noise) and it can introduce phase and amplitude error between the two paths of the receiver which is not negligible and difficult to calibrate, given the high operating frequency.

2.3 State of art of mmWave VCOs

The previous part of this chapter focused on the LO requirements for the receiver architectures operating at millimeter waves. Different architectures have been developed to simplify local oscillator specifications because, due to the very high operating frequency, it is one of the most critical components. This second part presents an overview of the state of the art for millimeter wave VCOs. The section will reports circuit topologies recently proposed in the literature, the performances and limitations.

Most of the architectures previously presented have been developed to avoid the need of a mm-Waves quadrature oscillator and require only a differential VCO. The circuit topology most widely used at RF is the CMOS differential LC-tank oscillator with both nMOS and pMOS cross-coupled pairs shown in figure 2.5. This topology presents in principle a superior phase noise performance [17], but is not adopted for mm-waves. The reason is the low cutoff frequency of p-channel MOSfets, approximately one third that of n-channel devices. The large parasitic capacitance introduced by pMOSfets reduces the tuning range while providing only a minor gain contribution. For this reason, pMOS are rarely employed to design oscillators at very high frequency. Cross

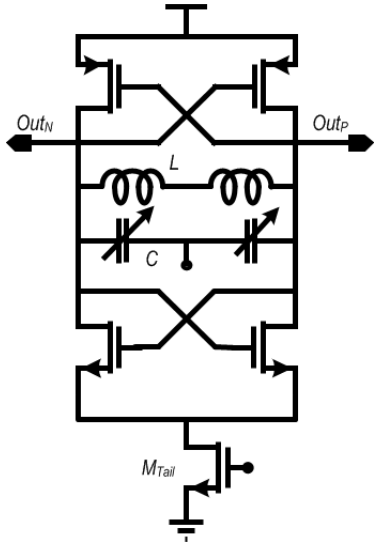

Figure 2.5: Simplified schematic view of the PN-VCO.

coupled VCOs with only nMOSfets are probably the most pervasive ones in high-speed systems, providing numerous merits to satisfy the requirements of different applications. Two different circuit schematics are reported in figure 2.6. These simple yet symmetric configurations facilitate high-speed operation and differential designs with large swing, reasonable tuning range, and low power consumption. The circuits also allow low-supply operation, even below $1V$.

The main differences between the two circuits are the common-

mode voltage of the resonator and maximum voltage swing. These two parameters play a key role in the tuning-range and phase noise performances of the VCOs. The ”bottom-biased” topology of figure 2.6a has the common-mode voltage of the resonator equal to the voltage supply (Vdd) and the biasing current is set by a nMOS current source. The maximum allowed voltage swing can be very high, close to two times the voltage supply, leading to a very good phase noise performance [18]. On the other hand the tuning range is limited if the variable capacitance (varactor) is realized with an accumulation-mode MOS (A-MOS). In fact, with this component, the tunig voltage must be larger than the supply to explore the maximum capacitance variation [19]. This solution is typically not feasible due to reliability issues. As an alternative, Bozzola [20] proposed to employ an inversion mode MOS (I-MOS) to realize the voltage controlled variable capacitor. With respect to the A-MOS, I-MOS allows exploiting the complete C-V characteristic with a tuning voltage within the supply of the VCO. This solution is very interesting even if the tuning range is slightly penalized by a lower capacitance change of I-MOS. Alternatively, in the ”top-biased” circuit topology of figure 2.6b, the biasing current source is connected from the supply to the center tap of the inductor reducing the resonator common-mode voltage to about half the supply [21, 22, 23]. In this case A-MOS varactors can be used maximizing the frequency tuning range. On the other hand the oscillation amplitude is reduced penalizing the phase noise. The previous circuit solutions are directly derived from realizations typical of RF system. A circuit topology specifically introduced for mm-waves is the push-push oscillator, shown in figure 2.7. This type of oscillator takes the $2nd$-order harmonic from the common-mode node of the oscillator, and amplifies it properly as an output [24]. Note that second harmonic is generated by the nonlinearity of the circuit, which manifests itself in large-signal operation. An example of circuit-level realization is proposed in [25, 26]. The $\lambda/4$ line reinforces the $2\omega_{osc}$ signal by providing an equivalent open at node P when looking into it and the output power could be quite large if proper matching is achieved. The main advantage is that the oscilla-

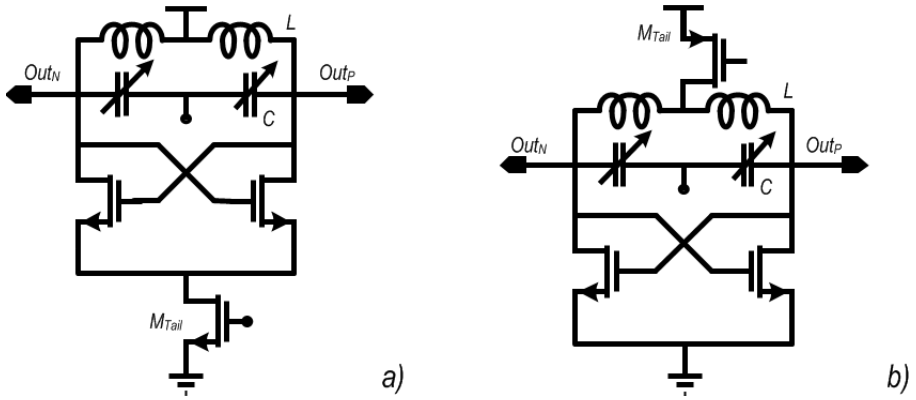

Figure 2.6: a) Simplified schematic view of the N-VCO ”bottom-biased” and b) ”top-biased”.

tor is designed at half frequency, so the tuning range and the phase noise are less penalized. On the other hand the push-push oscillator can only provide a single-ended output. In addition, tuning the fundamental frequency could result in a mismatch in the $\lambda/4$ line, potentially leading to large in band variations of the output power. Another

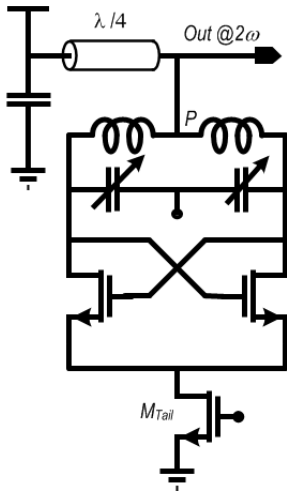

Figure 2.7: Push-push VCO based on cross-coupled.

characteristic VCO topology for high-speed operation relies on a distributed resonator and is named standing wave oscillator. This particular oscillator presents the resonator based on a transmission line. For

instance, a parallel resonance can be achieved using a short-circuited transmission line that has an electrical length of $\lambda/4$ at the desired oscillation frequency. The simplest topology where negative resistance is still realized with a cross coupled nMOS pair is shown in figure 2.8 and was proposed for instance by De Paola [27]. The distributed os-

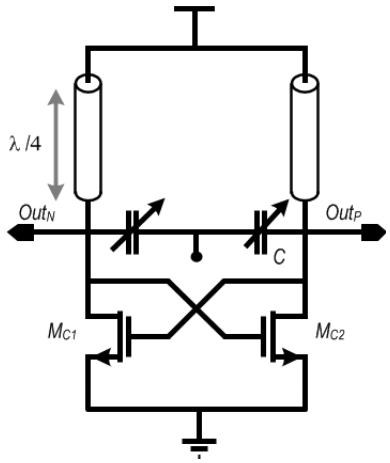

Figure 2.8: Schematic of Standing-Wave oscillator.

cillator proposed by Chien [28] with the simplified schematic reported in figure 2.9 has a transmission line with a variable length realized by introducing nMOS switches to short part of the line. This solution allows to achieve wider frequency tuning range. The distributed oscillators present several disadvantages. While looking attractive, they suffer from a number of drawbacks: area of the distributed resonator is larger than the lumped element counterpart, quality factor is typically lower leading to higher power dissipation, and the continuous frequency tuning provided by varactors is limited by the fixed capacitances distributed along the transmission lines. The switches introduced by Chen [28] to enlarge the tuning range by changing the line length introduce significant losses degrading phase noise. The most significant topologies of mm-waves oscillators have been summarized. The plots in figure 2.10 collect the tuning range and phase noise performances of the recently published VCOs operating from 20 to $120GHz$.

It is important to note that tuning range is drastically reduced with

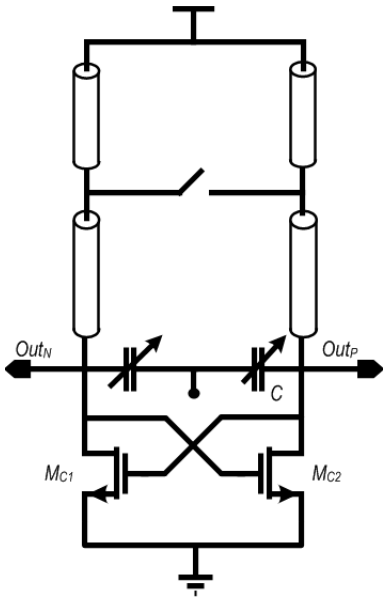

Figure 2.9: Simplified circuit of the Standing-Wave oscillator to illustrate the frequency tuning mechanism illustrated in [28].

the operation frequency. This is roughly independent from the topology and technology of the circuit. At frequency beyond $80GHz$ the tuning range in less than 5%. This value is not enough to compensate temperature and process variations and different circuit solutions need to be investigated. The phase noise performances present a similar trend that worsens as the frequency increases. These simple graphs confirm that as frequency increases, design of high performances VCOs is very troublesome. The reasons are easily attributable to the low quality factor of passive components, the low capacitance variation of varactors and parasitic capacitors introduced by active devices operating close to their cut-off frequency.

Even more difficult is the realization of a quadrature VCO [37]. Only few mm-waves implementations are present in the literature and are based on a pair of oscillators coupled together by active devices as shown in figure 2.11. Compared to a single oscillator, the circuit in figure 2.11 shows a lower tuning range caused by the large fixed capacitances loading directly the resonator, which are introduced by the

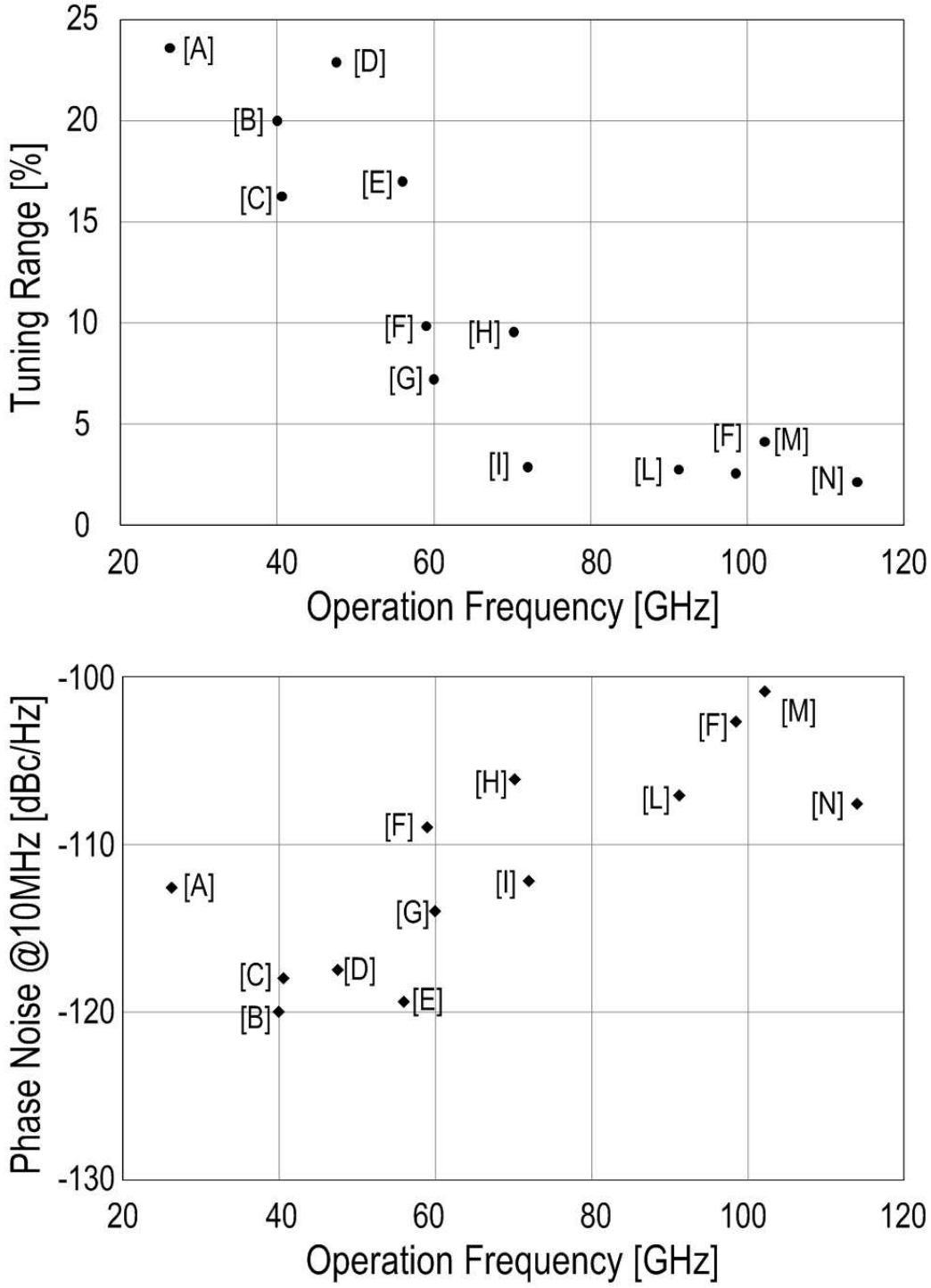

Figure 2.10: Tuning Range and Phase Noise performances of state of Art mm-waves VCOs. A [29], B [28], C [22],D [30],E [31],F[23],G[32],H [33],I [27], L [34],M [35],N [36].

parasitics of the coupling mosfets. It can also be proved that the oscillation frequency is dependent on device currents and not only by the resonance frequency of the tanks. As a results the low frequency noise (flicker) superimposed to the DC currents modulates the output signal frequency leading to large up-conversion of $1/f$ noise into $1/f^3$ phase noise. This aspect will be quantitatively discussed with more details in the next Chapter, where a new mm-waves quadrature oscillator will be proposed. To gain insight a phase noise simulation is reported in figure 2.12 showing a corner frequency close to $10MHz$.

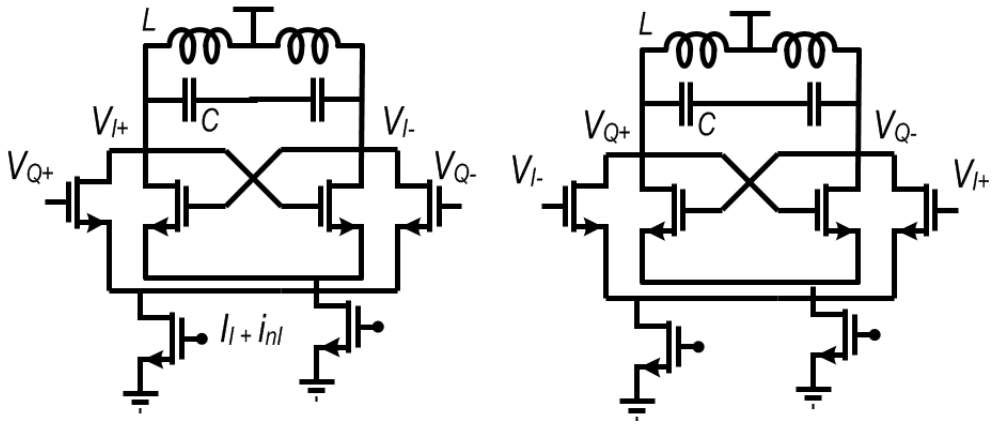

Figure 2.11: Quadrature Cross Coupled LC VCO schematic.

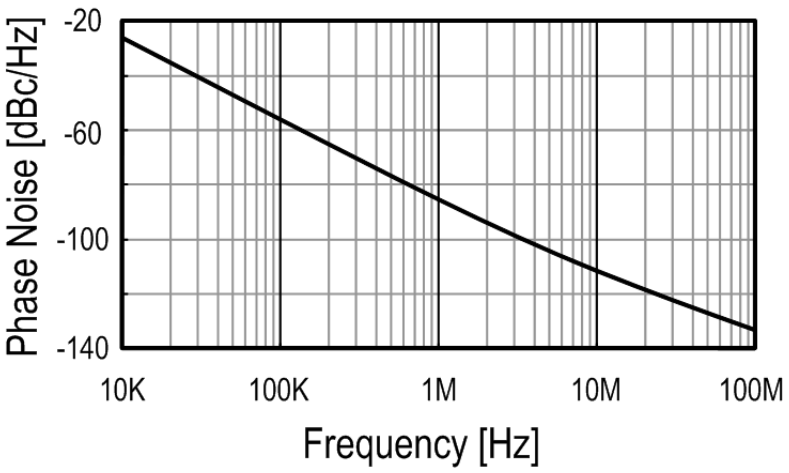

Figure 2.12: A simulation example of traditional quadrature VCO at $60GHz$.

Chapter 3

A Low-Noise Quadrature VCO Based on Magnetically Coupled Resonators

As discussed in the previous chapter, several heterodyne transceiver architectures have been investigated to circumvent peculiar problems such as generation of spectrally pure references with quadrature phases at received frequency. Nonetheless, the Intermediate Frequency (IF) stage itself is challenging due to wide-band requirements, complicates signal routing within the IC and is responsible for a significant power and area consumption. Low noise quadrature generators at mm-waves would enable direct conversion transceivers.

Double frequency oscillators followed by dividers by two represent a common technique for quadrature generation at RF, though disregarded at mm-waves where quality of passives degrades rapidly with increasing frequency and high speed frequency dividers are power hungry. Single phase VCOs followed by transmission lines or hybrids are suited for quadrature signal generation at high frequency [8], [38]. The drawback is a relatively large power consumed by the buffers interfacing VCOs to distributed passive components. Conventional cross-coupled LC VCOs constitute the most suitable topology borrowed by RF solutions [39]. But, the oscillation frequency dependence on the biasing current makes it susceptible to phase noise, close-in in particular [40]. The proposed solution[37] relies on a ring of two tuned VCOs, where the oscillation frequency depends on inter-stage passive components only, demonstrating low noise and accurate quadrature phases. Prototypes, realized in $65nm$ CMOS, show $56 - 60.4GHz$ tunable oscillation frequency, phase noise better than $-95dBc/Hz$ at $1MHz$ offset in the tuning range, 1.5^o maximum phase error while consuming $22mA$

from $1V$ supply

3.1 Quadrature VCO Based on Magnetically-Coupled Resonators

Coupled LC VCOs are the most attractive solution to generate high frequency quadrature signals at low power dissipation. As shown in figure 3.1a, a pair of harmonic VCOs are coupled by means of two additional differential pairs and forced to run in quadrature. The main drawback is the large phase noise degradation, close-in in particular, deriving from $1/f$ noise conversion into $1/f^3$ phase noise. The mechanisms can be revised looking at figure 3.1, where the circuit schematic is reported together with the phasor diagram of a tank voltage and current. The current I_B adds up I_I and I_Q, phase shifted by 90^o between each other, so that a phase difference Ψ_{Tank} between total tank current and voltage V_{Tank} is determined. The LC tank works off-resonance. From figure 3.1b $\Psi_{Tank}(\omega) = \arctan\dfrac{I_Q}{I_I}$, because the phase response of an LC resonator can be approximated, around resonance frequency ω_0, as $\Psi_{Tank}(\omega) \approx \arctan(2Q\frac{\omega-\omega_0}{\omega_0})$ where $\omega_0 = \dfrac{1}{\sqrt{LC}}$ and Q is the tank quality factor, the oscillation frequency ω_{osc} can be derived from:

$$\arctan(2Q\frac{\omega-\omega_0}{\omega_0}) = \arctan\frac{I_Q}{I_I} \tag{3.1}$$

leading to [41]: factor, the oscillation frequency ω_{osc} can be derived from:

$$\omega_{osc} = \omega_0\left(1 \pm \frac{I_Q}{I_I}\right) \tag{3.2}$$

Equation 3.2 reveals that amplitude noise in currents I_I and I_Q directly translates into phase noise, in contrast with mechanisms of classical single phase VCOs. This explains the gap in the phase noise figure of merit of single phase VCOs and transistor coupled quadrature VCOs. Moreover, implementations at mm-waves must use core devices of small dimensions and $1/f^3$ phase noise corners are encountered at

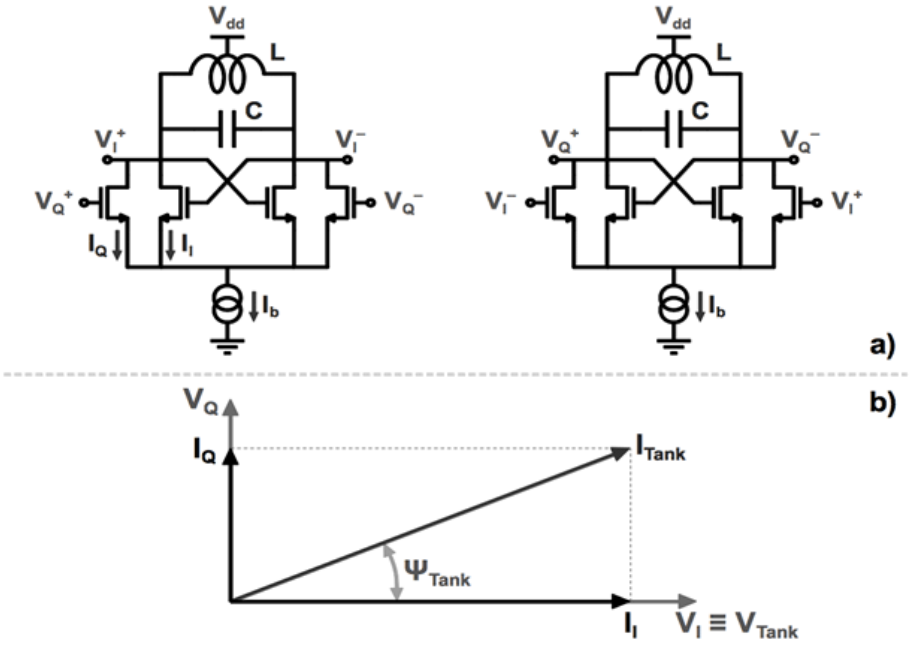

Figure 3.1: a) Cross Coupled LC VCO schematic. b) Phasor diagram.

several MHz [39, 42], too high for the applications of interest. The phase shift necessary to sustain the quadrature oscillation can be provided using passive components only. In this way the dependence of ω_{osc} from device current disappears avoiding direct up-conversion of flicker noise into phase noise. This happens in the two stage ring VCO of figure 3.2. Each stage is made of a transconductance gain block (g_m) and a reactive load coupled to the cascaded stage. To gain insight, let us characterize the two-ports passive inter-stage network by the admittance matrix Y:

$$[Y] = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} \tag{3.3}$$

By inspection, assuming for simplicity $R_{p1} = R_{p2} = R$, the following expressions are derived:

$$y_{11} = \frac{1}{R} + sC + \frac{1}{sL(1-k^2)} \tag{3.4}$$

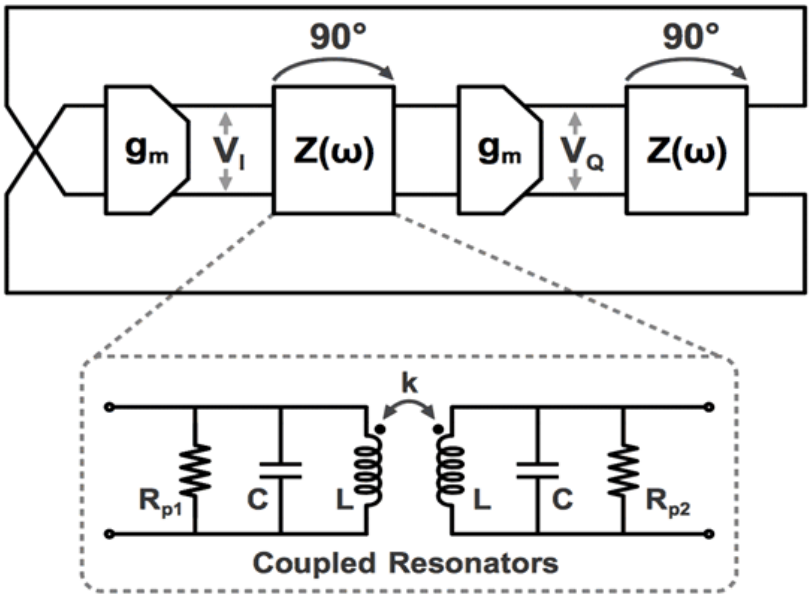

Figure 3.2: Ring of two magnetically coupled VCOs.

$$y_{22} = \frac{1}{R} + sC + \frac{1}{sL(1-k^2)} \tag{3.5}$$

$$y_{12} = \frac{k}{sL(1-k^2)} \tag{3.6}$$

$$y_{21} = \frac{k}{sL(1-k^2)} \tag{3.7}$$

From the admittance matrix, the expression for the trans-impedance Z_{12} for $s = j\omega$ follows:

$$z_{12} = -\frac{y_{12}}{y_{11}y_{22} - y_{12}y_{21}}$$

$$z_{12} = \frac{jk}{(1-k^2)L\omega\left(\left(\frac{k}{(1-k^2)\omega L}\right)^2 + \left(\frac{1}{R} + j\left(C\omega - \frac{1}{\omega L(1-k^2)}\right)\right)^2\right)} \tag{3.8}$$

The real part of $1/Z_{12}$ reduces to zero at resonance, i.e. the phase shift between the input current and the output voltage is $\pi/2$. The

two cascaded stages provide π radians of phase shift which, together with the cross-connection of the wires in the feedback path, lead to a total loop phase of 2π. The resonance frequency ω_0 of each inter-stage network of figure 3.2 is solution of :

$$Re\left[\frac{1}{Z_{12}}\right] = \frac{-2-2C(1+k^2)L\omega}{kR} = 0 \tag{3.9}$$

$$\omega_0 = \frac{1}{\sqrt{LC(1-k^2)}} \tag{3.10}$$

In order to start-up and sustain the oscillation, a loop gain greater than one must be provided, so the condition $(g_m \cdot Z_{21})^2 > 1$ must be satisfied. The magnitude of the transimpedance of the coupled resonators at ω_0 can be derived by substituting 3.10 into 3.8:

$$Z(\omega_0) = \frac{kRQ}{1+(kQ)^2} \tag{3.11}$$

where $Q = \omega_0 RC = R/(\omega_0 L(1-k))$. To gain insight, figure 3.3 shows magnitude and phase of Z_{12} versus frequency for different k values, with a Q of 5. The resonance frequency is set to $60GHz$ for $k = 0.08$, and varies according to 3.10. The trans-impedance magnitude has a maximum at ω_0 for $k = 0.2$ (i.e $kQ = 1$). This is valid in general, for any value of Q, and can be proved by finding the analytically the maximum of $|Z_{12}(\omega_0)|$. Moreover, k influences the phase variation versus frequency at resonance in a monotonic fashion, i.e. the lower k the higher the phase derivative. A large impedance amplitude together with a steep phase variation are desirable for the ring VCO to minimize phase noise and power consumption. The above considerations suggests therefore an optimum kQ value of 1. In order to prove the concept of the flicker noise reduction and to establish a quantitative comparison, the phase noise of the two circuits shown respectively in figure 3.1a and figure 3.2 have been simulated and the results are shown in figure 3.4. Both circuits draw $22mA$ from $1V$ supply, have the same Q of 5 for each LC tank, and have been sized to provide a maximum I/Q phase error of about 2 degrees. No varactors have been included in order to avoid

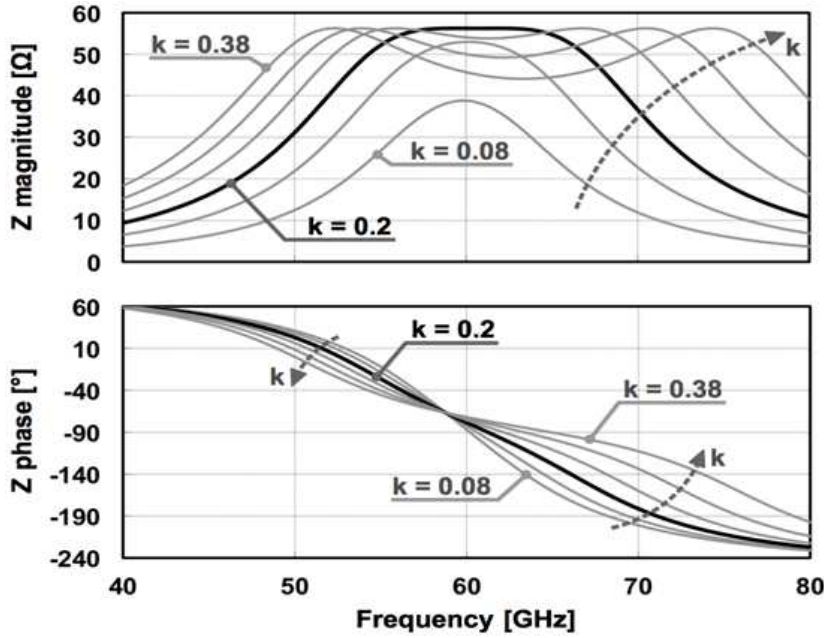

Figure 3.3: Trans-impedance phase and magnitude for magnetically coupled resonator vs frequency, for different k values.

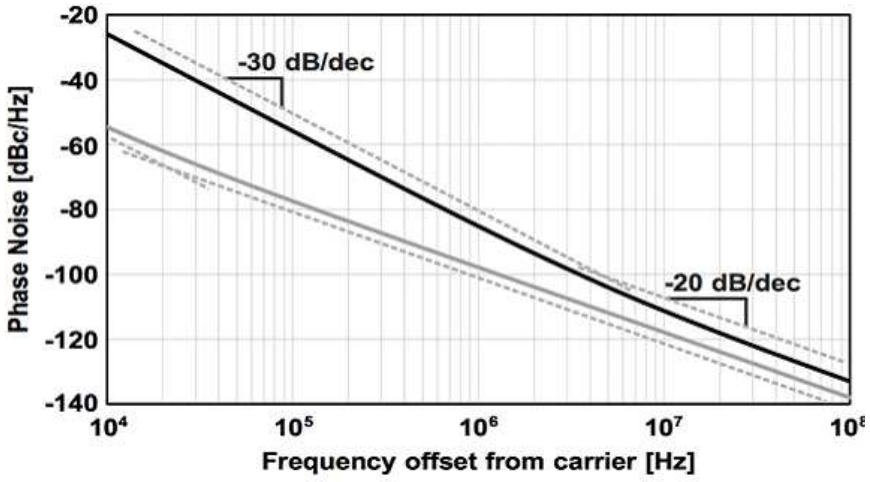

Figure 3.4: Phase Noise: comparison between theory (dashed line) and simulations for ideal transistor (continuous grey line) and for real transistor (continuous black line).

$1/f$ noise conversion into phase noise due to second-order effects like AM to PM conversion. The proposed solution shows a significant improvement since the $1/f$ noise corner is moved downward by almost two decades, from $\sim 10MHz$ to $\sim 20kHz$

3.2 Circuit implementation

Each pair of resonators in the proposed circuit can be coupled magnetically or capacitively [43]. It can be proved that the transfer function of the coupled resonators is the same. With capacitive coupling four separate inductors are needed, and they should be placed relatively far to each other in order to keep the magnetic coupling negligible and capacitive coupling as the main one. The magnetic version allows a $2\times$ area saving, with the additional benefit of the simplification of the routing of the quadrature signals out of the core. A $3D$ view of the implemented transformer with a simple lumped model is shown in figure 3.5. In order to realize a comparable inductance for the two interleaved windings, those should be very close to each other, thus leading to a high coupling factor, k_1. As derived in the previous section, the optimum coupling is rather small, about $1-2$ tenths for a Q of 5 of the overall resonator. A closed-loop shield has been introduced surrounding the outside inductor with the purpose of reducing the equivalent coupling coefficient between internal and external inductors. Intuitively, a current in L_{ext} induces a current in with opposite direction in L_{sh}. The magnetic fields induced on the internal inductor by the external one and by the shielding structure tend to cancel each other reducing the equivalent coupling coefficient between L_{int} and L_{ext}. By inspection of the equivalent circuit in figure 3.5, the coupling between the inner and outer inductors is:

$$k_{eq} = k_1 - k_2 k_3 \tag{3.12}$$

The shield has been realized with two turns, embedding the secondary winding in order to maximize k_3 and thus reducing k_{eq} down to the desired value of ~ 0.15. Accurate electromagnetic simulations have been

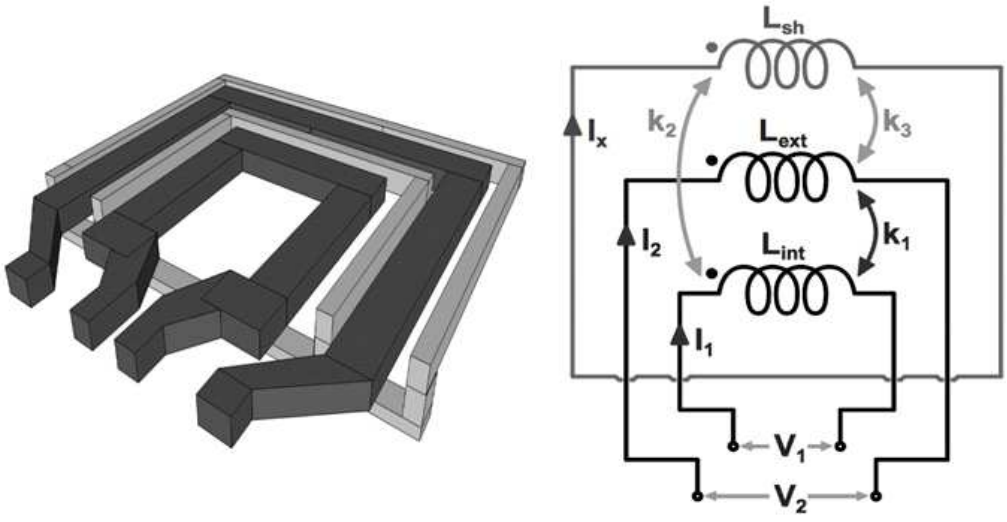

Figure 3.5: Low-k transformer: 3D view and simplified lumped model.

performed over the entire structure of the coupled resonator. Results are shown in figure 3.5. The internal inductance is $98pH$ with a Q of 19, while the external one is $113pH$ with a Q of 15. The shielding structure reduces the inductance L_{ext} and slightly lowers its Q, which would be equal to 18 without the shield. The former makes it easier to realize the two windings with comparable inductance, while the latter potentially degrades oscillator performance. However, because AMOS varactors present a quality factor around 7 at $60GHz$, the Q reduction has only a minor effect on the overall tank's losses, i.e., on the oscillator performances. The complete schematic of the implemented QVCO is depicted in figure 3.7. Three digitally controlled varactors implements the coarse tuning of each LC tank in eight different bands, with an AMOS varactor for fine analog tuning within the band. Since varactors are responsible for $1/f$ noise conversion into phase noise, the circuit has been biased by means of digitally controlled resistors R_{bias} minimizing the sources of flicker noise. Biasing resistors have been placed between the supply voltage and the center taps of the transformers, in order to nominally set the output nodes around $VDD/2$ and thus explore the tuning characteristic of the AMOS varactors in their region

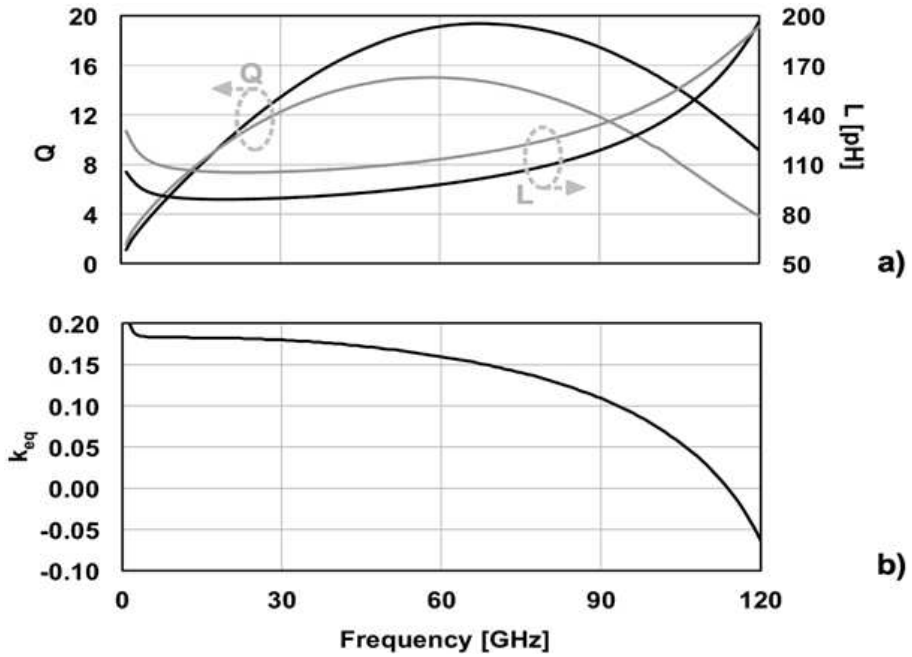

Figure 3.6: a) Low-k transformer: simulated inductance and quality factor values versus frequency for the internal (black lines) and the external (grey lines) winding. b) Simulated equivalent coupling coefficient k_{eq} for the transformer.

of steepest variation. Aspect ratio of transistors is $30\mu m/60nm$. They have been oversized with respect to the minimum required to start the oscillation, in order to ensure a wide margin on modeling errors of the transformers. The penalty is a limited tuning range, in this prototype, due to the large parasitic capacitance introduced by the transistors. Active devices work in a pseudodifferential way, increasing the risk of common mode oscillations. In fact, the Barkhausen condition on the phase holds true provided the coupled resonators result in a phase shift of 90^o, but also 0^0 and 180^0. The latter two cases lead to common mode oscillations and are to be avoided. R_{cm} are introduced to limit the loop gain for common-mode signals. Intuitively, resistors R_{cm} drastically reduce the quality factor of the resonator under common mode excitation while the loop gain is not affected when a differential signal propagates. The resistance has been set equal to $6k\Omega$, more than enough to avoid common mode oscillations in any possible process corner and over a wide temperature range. The simulated minimum oscillation amplitude is $300mV_{0-pk}$ single-ended.

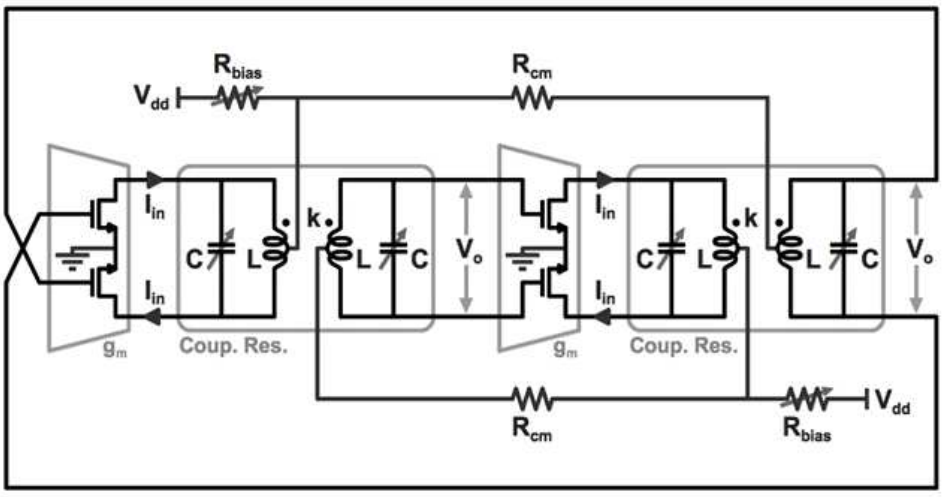

Figure 3.7: Complete schematic of the realized quadrature VCO.

3.3 Experimental Result

The quadrature oscillator of figure 3.7 has been realized in a standard $65nm$ CMOS bulk node from STMicroelectronics, featuring 7 Cu Metal layers plus an Al metal cover layer. Supply voltage is $1V$ and General Purpose transistors have been used. The chip micrograph is reported in figure 3.8. The VCO occupies an area of $0.075mm^2$ and draws $22mA$. The oscillator output signals can be tested directly at $60GHz$ or down-

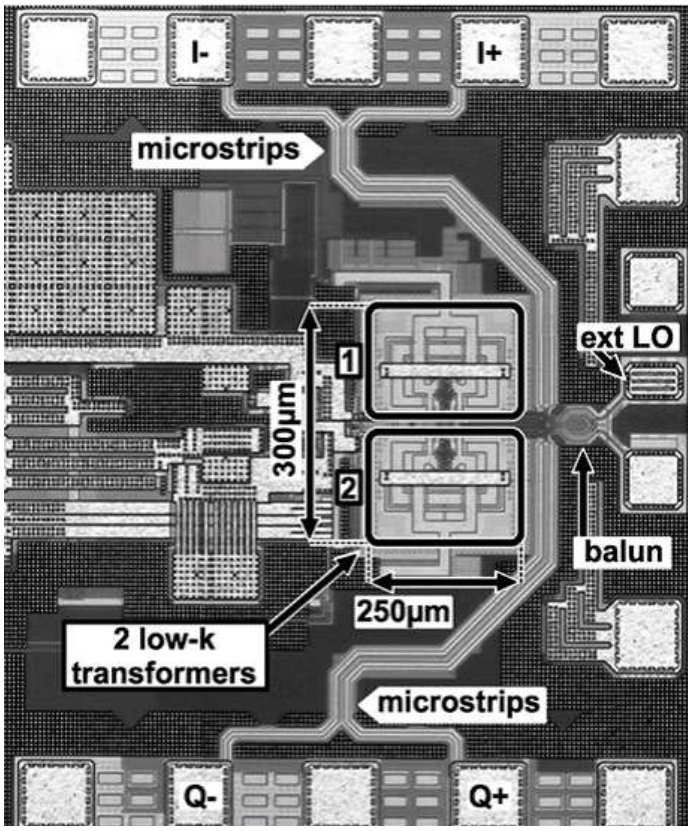

Figure 3.8: QVCO chip photomicrograph.

converted to a lower frequency by means of a quadrature mixer driven by an external frequency reference to better determine the phase accuracy. The mixer used for testing purposes is based on a conventional Gilbert cell. A bock diagram of the measurement setup is shown in figure 3.9 The VCO can be tuned between $56GHz$ and $60.4GHz$, in eight

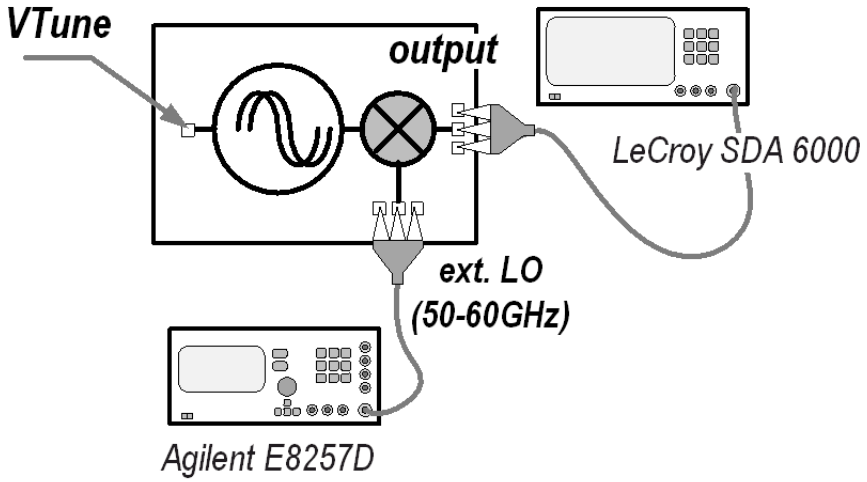

Figure 3.9: Experimental setup for testing the phase error of QVCO.

bands $500MHz$ wide. The 7.6% tuning range is mainly due to transistor oversizing to assure start-up with wide margin. From our estimations, halving the device dimensions would double the frequency tuning range, i.e. covering the application bandwidth, while still assuring oscillation start-up. The AMOS control voltage is varied between 0 and $1.2V$. The analog tuning allows $500MHz$ overlap between different bands. figure 3.10a shows measured phase noise for a $58.6GHz$ tone: corner frequency is less than $1MHz$, demonstrating a very low conversion of $1/f$ noise into phase noise and the spot value at $10MHz$ offset from carrier is $-117dBc/Hz$. Phase noise values at $1MHz$ offset from the carrier within the entire tuning range are reported in figure 3.10b, revealing a maximum variation of $2dB$. Phase accuracy measurements are reported in figure 3.11 where a scope screen-shot with quadrature signals down-converted at $200MHz$ is shown. The same measurement repeated at different VCO frequencies reveals a phase error always $< 1.5^o$ and an amplitude mismatch $< 1dB$. The oscillator performances are summarized in table and compared with state of the art mm-W QVCO. The phase noise figure of merit (FOM), defined as:

$$FOM = L(\Delta\omega) - 20\log\left(\frac{\omega_0}{\Delta\omega}\right) + 10\log\left(\frac{P_{diss}}{1mW}\right) \qquad (3.13)$$

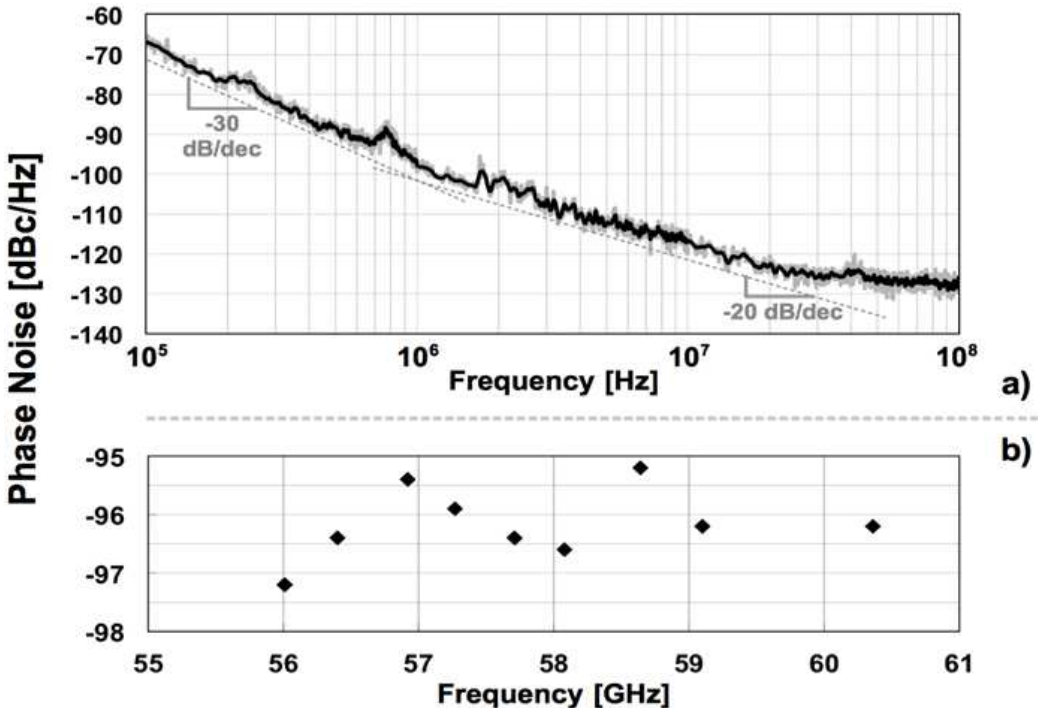

Figure 3.10: a) Measured phase noise for a $58.6GHz$ output frequency. b) Phase noise values at $1MHz$ offset from the carrier within the tuning range.

ranges from $-177dBc/Hz$ to $-179dBc/Hz$ (worst and best cases in band respectively) when calculated at $1MHz$ offset from the carrier, the best published today. The presented oscillator also shows good performances in terms of phase accuracy and occupies a relatively small area.

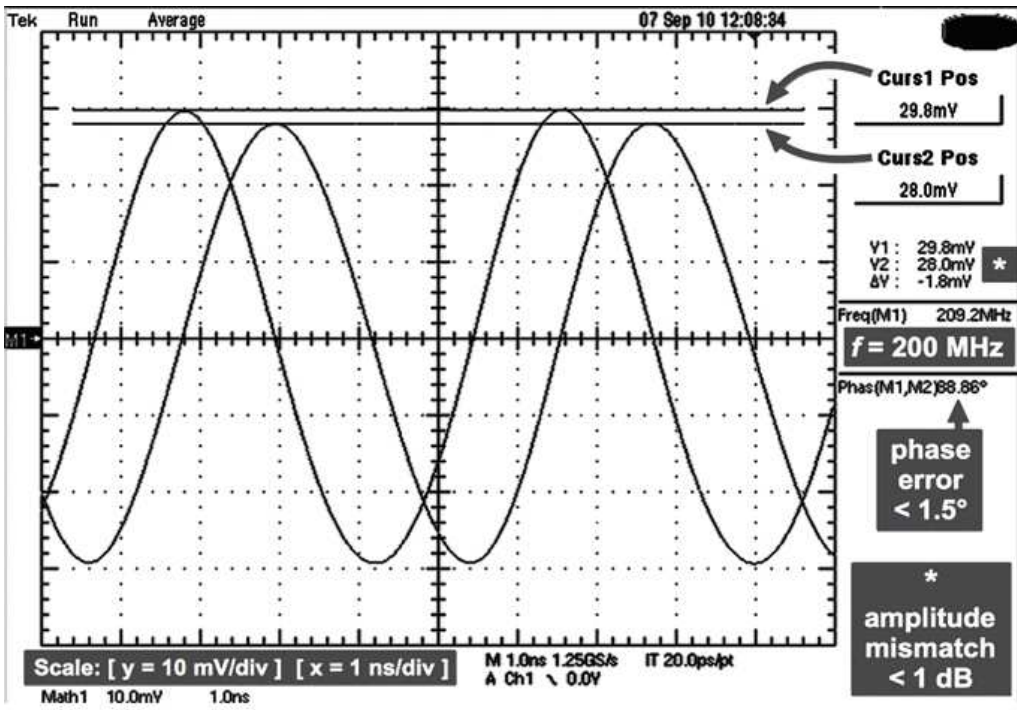

Figure 3.11: VCO quadrature output signals down-converted to $200MHz$.

Ref	Tech	Freq	T.R.	P.N.@1MHz	FOM	PhaseError	Area	Power
		[GHz]	[GHz]	[dBc/Hz]	[dBc/Hz]		[mm^2]	[mW]
[39]	90nm CMOS	48	8	-85	-165	n.a.	n.a.	22.7
[44]	65nm CMOS	93.1	4	-90	-172.7	n.a.	n.a.	43.2
[42]	45nm CMOS	61.6	9	-75	-156	n.a.	n.a.	28
This work	**65nm CMOS**	**58.2**	**4.35**	**-95 / -97**	**-177 /-179**	$< 1.5^o$	**0.075**	**22**

Chapter 4

Injection-Locked Frequency Doublers

4.1 Introduction

Several CMOS transceivers have been already demonstrated targeting high speed wireless communications in the $60GHz$ band [38, 14, 22] and [15]. Increasing the operating frequency near or above $100GHz$ for applications requiring a short wavelength, i.e. imaging and radars, is still extremely difficult. Fewer realizations have been reported requiring high power dissipation and displaying worst performances [45, 46]. Generation of the local oscillator is a major obstacle due to the degradation, with increasing frequency, of key passive components on silicon substrates. Adoption of Voltage Controlled Oscillators (VCOs) at fundamental frequency sets an increasingly severe trade-off between high spectral purity and frequency tuning range due to a dramatic reduction of varactors quality factor and the impact of large device parasitic capacitances. Several new receiver architectures, described in Chapter II, have been recently proposed to simplify local oscillator design requiring a reference frequency lower than input signal frequency. The penalty is a complication of the signal processing path, requiring in general many cascaded mixing stages and increased power dissipation. An alternative approach, usually pursued with compound semiconductor technologies, relies on a frequency multiplier driven by a VCO running at a lower frequency, as shown in the simplified PLL of figure 4.1. The most effective solution exploits the nonlinearity of active devices to generate harmonics of the input signal [47, 48] and [49]. When designed in CMOS, they suffer from low-conversion gain, or even loss, large input capacitance, and single-ended output. For these reasons the principle of frequency multiplication did not find extensive appli-

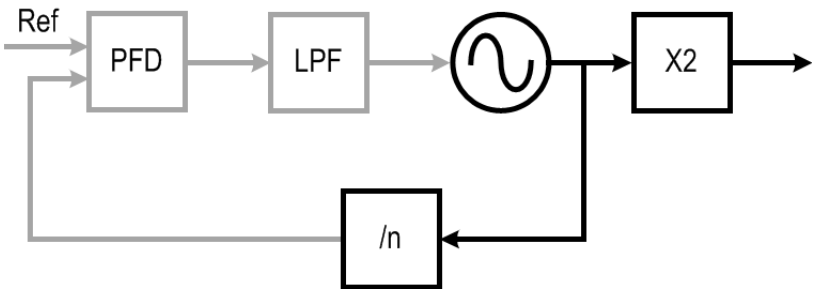

Figure 4.1: Phase locked loop followed by a frequency doubler.

cation to date. In this chapter, after a brief review of frequency multiplication techniques, a new topology of CMOS frequency multiplier by two, based on injection locking is presented. The proposed solution leads to a very low power dissipation, requires limited input signal swing and provides a differential output over a broad frequency range.

4.2 Review of Frequency Doubling Techniques

Frequency doubler circuits at microwaves and millimetre-waves can be categorized in two main groups:

1. Mixer based

2. Device non-linearity based

The principles of operation and the limits in CMOS technology are discussed in this section.

Figure 4.2 shows the conceptual diagram of a mixer based frequency doubler [50, 51, 52] and [53]. The RF and LO ports of a Gilbert-mixer are driven by the same input signal, generating an output component at twice the input frequency. The main advantage of this solution is the broad frequency range of operation. A state of the art realization, in a $200GHz$ f_T BiCMOS technology, displays a very large operation bandwidth, spanning from $36GHz$ to $80GHz$ output frequency, a peak output power of $1.4dBm$ at $66GHz$, although with a large power dissipation of $43mA$ from $3.3V$ supply [53]. As a drawback, a DC offset large

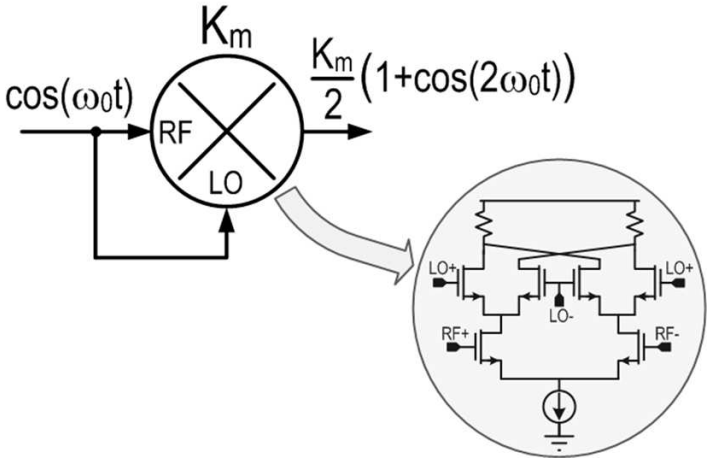

Figure 4.2: Frequency multiplier based on a Gilbert-Cell mixer (K_m is the mixer conversion gain)

at least as the desired double frequency signal appears at the output. It may saturate the mixer limiting the conversion gain. A 90^o phase shifter can be introduced at either mixer input port to minimize output DC offset. But, phase shifters are narrow-band and introduce losses. In order to suppress the fundamental component, fully balanced mixer topologies are employed, with the drawback of large capacitance at the input ports and significant power dissipation. Maximum operation frequency is also limited by the parasitic capacitance at the sources of the switching quad. Moreover, requiring multiple stacked devices, this topology does not lend itself to implementation in scaled CMOS technologies, biased at low supply voltage. A widely adopted alternative approach relies on selection of the harmonic component generated by a non-linear active device [54, 55, 56, 57, 58, 59] and [60].

The simplest schematic diagram is shown in figure 4.3a. If the MOS transistor is driven into compression, the drain current is rich of harmonic components of the input signal. A resonant load selects the desired one (e.g. $2nd$ harmonic for frequency doublers) and suppresses the fundamental. For maximum conversion efficiency the device conduction angle must be low i.e. it must be biased to operate in class-B or class-C. The amplitude of the fundamental is nevertheless much larger

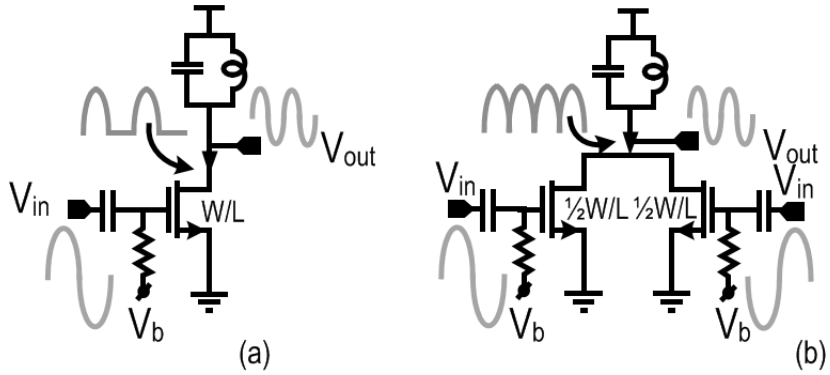

Figure 4.3: (a) Frequency Multiplier based on device non-linearity (b) and Push-push configuration to suppress the fundamental component and odd harmonics)

than its harmonics and achieving adequate suppression by means of integrated LC filters, showing a moderate quality factor, is troublesome. As a numerical example, assuming a resonator quality factor of 10, simulations of a frequency doubler based on the circuit of figure 4.3a in a $65nm$ CMOS technology reveals a fundamental rejection, with respect to the desired component, of only about $15dB$. A simple circuit technique to cancel out the fundamental frequency at the output, commonly known as push-push pair, is shown in figure 4.3b. Compared to figure 4.3a, the MOS device is split in two transistors of half size with the drain and sources in parallel and the gates driven by signals in opposite phase. Provided the inputs are perfectly balanced, the fundamental component of the total drain current is at twice the input signal frequency. To gain insight in the performances of this circuit at millimetre waves, figure 4.4 shows the input-output power curve of a design example in a $65nm$ CMOS technology, tuned for $120GHz$ output frequency. Size of the two devices is $40um/65nm$, showing a capacitance of about $50fF$ on each single ended input. A fixed capacitance of $20fF$ is placed at the output to simulate the loading effect of a buffer stage. The inductor is a single spiral of $100pH$ with a quality factor of 15. The drain currents, when the input differential signal is $600mV$ $0-pk$ (i.e. $6dBm$ in a 50Ω system), are shown in figure 4.5. The de-

vices work in class B (i.e. with a conduction angle of about π radians). Current consumption is $7mA$ and the double frequency component is $4.5mA$. A better performance is achieved in III-V and bipolar technologies, compared to CMOS, because they are less affected by non-ideal effects, like sub-threshold current and channel-length modulation, and they are characterized by a steeper non-linearity of the I-V curve. From figure 4.4, the output voltage swing is $200mV$ (i.e. $-4dBm$ in a 50Ω system) and the circuit features a voltage conversion loss of $10dB$. To

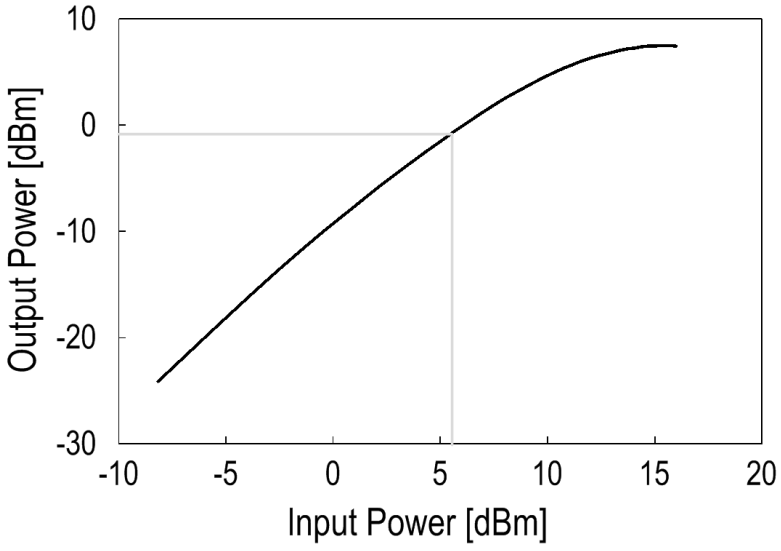

Figure 4.4: Simulated input-output power of a push-push frequency doubler tuned at 120GHz output frequency.

reduce conversion loss, the amplitude of the double frequency current can be further increased, for fixed power consumption, increasing the device size and reducing the conduction angle. On the other hand, the input capacitance rises very quickly. As an example, the gray curve in figure 4.5 reports the devices current when the conduction angle is reduced to about $3/4\pi$. The harmonic current is doubled but device size is eight times larger. The equivalent input capacitance is around $400fF$, excessively large to be driven on-chip at mm-waves. A further drawback of this circuit configuration is that, while the input is differential, the output is single-ended, not suited in general to drive high perfor-

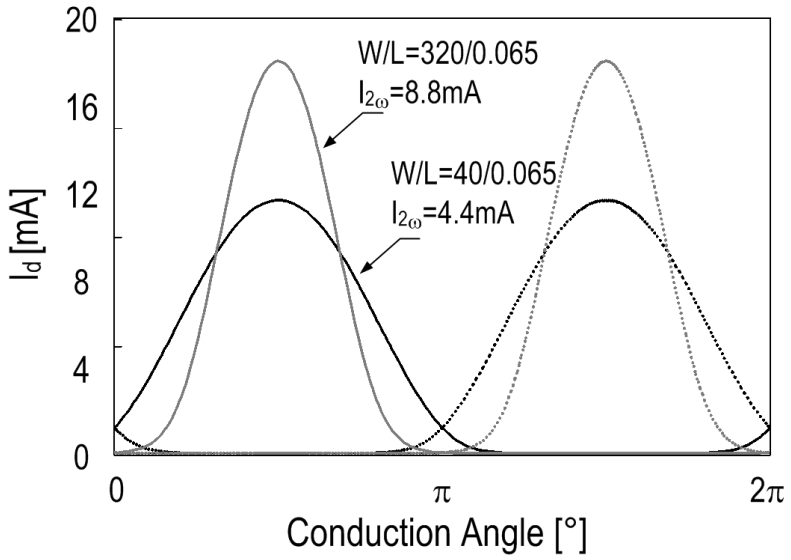

Figure 4.5: Drain currents of the push-push frequency doubler for two different device sizing and biasing.

mance mixers. At such high frequencies, differential signals are also desirable to avoid the need of accurate modeling of current return paths [61]. The load inductor in figure 4.3 can be in principle replaced by a transformer, providing a differential output on the secondary winding. On the other hand the weak spiral coupling and further parasitic capacitors introduced by the secondary further penalize the conversion gain.

4.3 Injection Locking Frequency Doubler

The proposed solution is based on the injection locking technique. It has been studied the use of a push-push pair to injection lock an oscillator running close to twice the input signal frequency[62, 63]. CMOS Injection locked oscillators topologies for millimeter waves multipliers have been recently introduced but display a limited operation bandwidth [64, 65]. The conceptual block diagram of the proposed solution is shown in figure 4.6 Compared to a simple push-push multiplier, a differential output can be easily obtained by selecting a differential

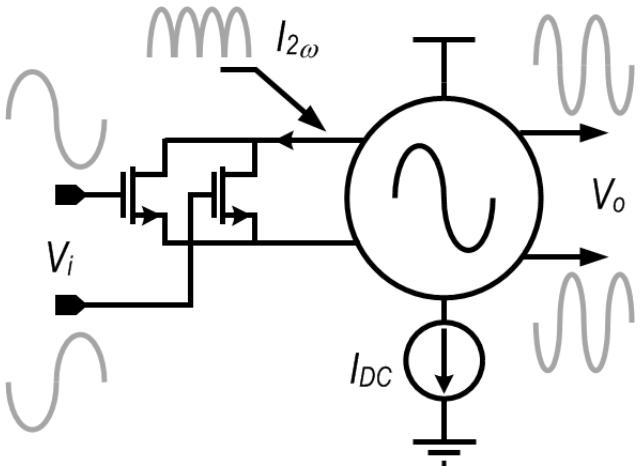

Figure 4.6: Operation principle of the proposed frequency doublers.

oscillator topology and the trade-off between device size and output swing is mitigated, being the amplitude of the output signal primarily determined by the DC biasing current of the oscillator instead of the $2nd$ harmonic component of the driving push-push pair. The output swing is also at first order independent of the input signal swing. Compared to previously reported injection locked multipliers, the relatively large second harmonic current injected by the push-push pair leads to a wider frequency locking range. The circuit schematic of the proposed injection-locked frequency doubler is shown in figure 4.7. The $C-L-C$ π-network and transistor M_1 form a Pierce oscillator [66]. The free running frequency is set by capacitance C and the inductance L according with to the equation:

$$\omega = \sqrt{\frac{2}{LC}} \tag{4.1}$$

Transistors $M2-2'$, connected in push-push configuration, inject a current in the resonator node V_1 at twice the input signal frequency to lock the oscillator. The core transistors are biased at a constant DC current, set by the two current mirrors M_b, while capacitors C_b are large enough to behave as AC shorts. The supply to the circuit is provided through a choke inductor (L_{ck}) to the center tap of the resonator. This solution makes the circuit suitable for technologies with low supply

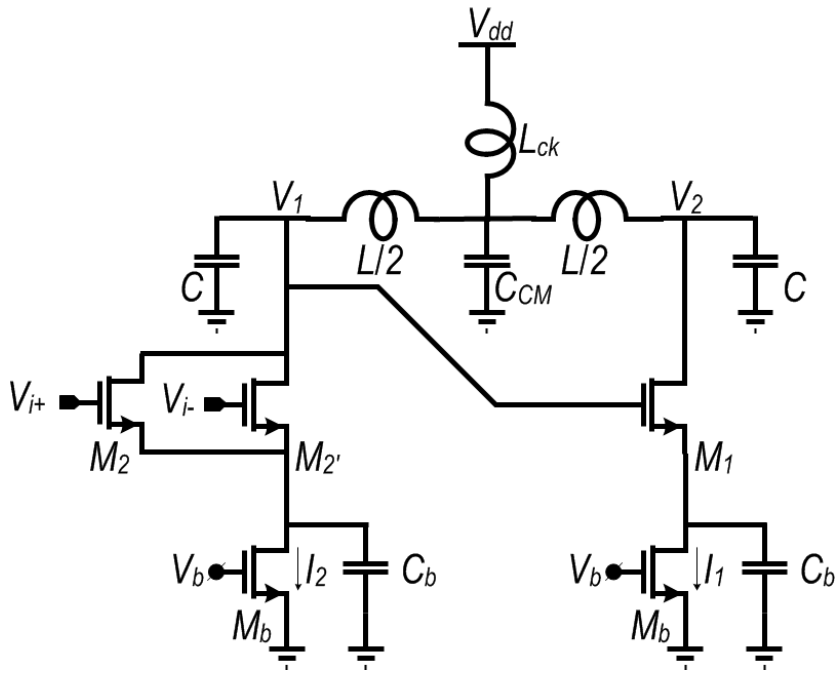

Figure 4.7: Schematic of the frequency doubler.

voltages where it is difficult to stack more than two mosfets. Moreover notice that grounded capacitors are explicitly required in each node for proper operation and absorb all device parasitics, making the circuit particularly suited for very high operation frequency. Capacitor C_{CM} is introduced to balance the two output voltages, V_1 and V_2. In fact, even if transistor M1 sets 180^o between V_1 and the current injected in the resonator node V_2, the two ports of the π-network are not driven symmetrically and the outputs are not balanced. Capacitor C_{CM} (of capacitance $2C$) suppresses the output common mode voltage V_{CM}. As an intuitive view, V_{CM} is shorted to ground by the low impedance provided by the series resonator formed by C_{CM} and the $L/2$ branches. To gain insight in the circuit operation, let's focus on the simplified equivalent circuit shown in figure 4.8. The two ports resonator is modeled by the $2X2$ impedance matrix reported in the figure. Being the network passive and symmetric, $Z_{11} = Z_{22} = Z$ while $Z_{12} = Z_{21} = Z_T$. Resistors R represent losses near resonance frequency. The independent left cur-

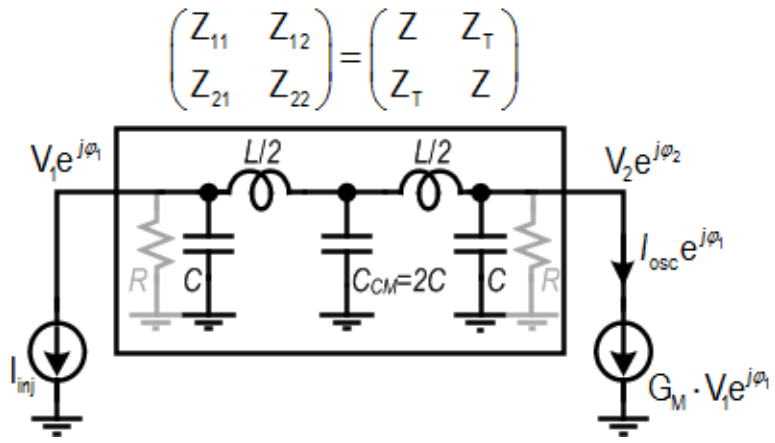

Figure 4.8: Simplified equivalent circuit of the frequency doubler.

rent generator represents the locking current from the push-push pair while the controlled current source on the right models the feedback transistor M_1. The fundamental component of its output current (I_{osc}) is aligned in phase with the driving voltage (V_1). Furthermore I_{inj} is assumed with zero phase, as a reference, while the phases of the two output voltages are φ_1 and φ_2 respectively. The two output voltages are solutions of the following system of equations:

$$\begin{cases} V_1 e^{j\varphi_1} = Z_T I_{osc} e^{j\varphi_1} - Z I_{inj} \\ V_2 e^{j\varphi_2} = Z I_{osc} e^{j\varphi_1} - Z_T I_{inj} \end{cases} \tag{4.2}$$

V_1 and V_2 are balanced (e.g. $|V1| = |V2|$ and $V_1 = V_2 \pm \pi$) only if $Z_T = -Z$. Simulated magnitude and phase of the two impedances in the absence of capacitor C_{CM} are shown in figure 4.9), with dotted lines, for a design example ($L = 80pH$, $C = 64fF$, $R = 110\Omega$). The impedance magnitudes are significantly different and the two phases deviate from 180^o by more than 20^o. Simulations with capacitor C_{CM} are shown with continuous lines in figure 4.9. In this case, the impedance magnitudes differ less than $1dB$ over a fractional bandwidth of 20% around resonance frequency while the phases are almost perfectly 180^o apart. In presence of C_{CM}, inspection of the resonator leads to the following simplified

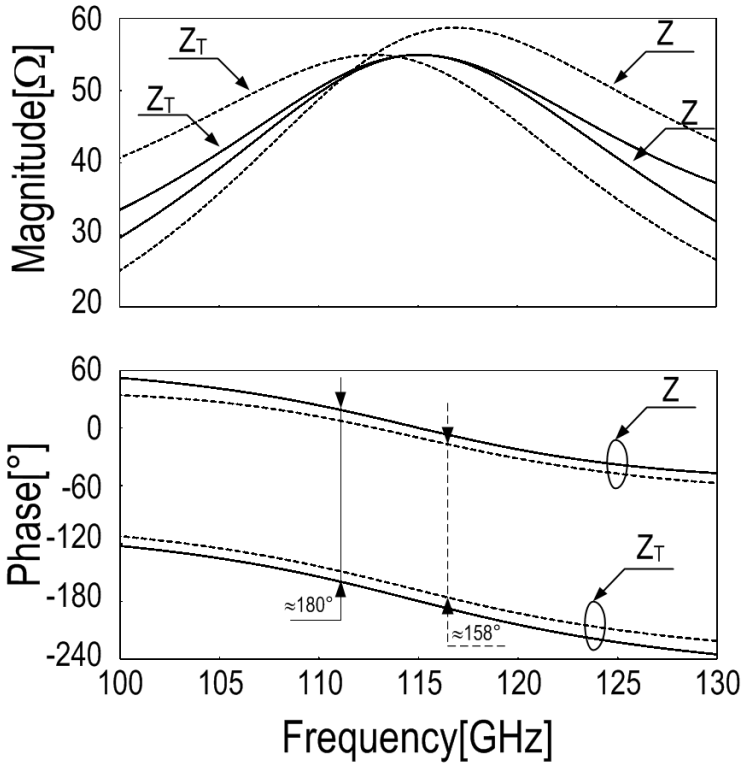

Figure 4.9: Simulated impedance magnitude (a) and phase (b)of the two ports resonator in figure 4.8, without capacitor C_{CM} (dotted lines) and with capacitor C_{CM} (black solid lines).

expressions for Z and Z_T near resonance frequency ω_0:

$$Z(\omega) = \frac{R}{2}\frac{1}{1+2jQ\frac{\Delta\omega}{\omega_0}} \tag{4.3}$$

$$Z_T(\omega) \approx -Z_T(\omega) \tag{4.4}$$

$$\omega_0 = \sqrt{\frac{2}{LC}} \tag{4.5}$$

Simplifications are valid down to moderately low quality factors. For comparison, equations (4.3) are plotted against the simulation example in 4.9, where $Q = 5 (Q = \omega_0 RC)$. Using (4.3) and (4.4) the system of equations (4.2) becomes:

$$\begin{cases} V_1 e^{j\varphi_1} = \dfrac{R}{2}\dfrac{I_{osc}e^{j\varphi_1} - ZI_{inj} + I_{inj}}{1+2jQ\frac{\Delta\omega}{\omega_0}} \\ V_2 e^{-j\varphi_1} = V_1 e^{j\varphi_1} \end{cases} \tag{4.6}$$

From 4.6b, the two output voltages are balanced. Solution of 4.6a following the approach of [67] gives the (single-sided) frequency locking range:

$$\Delta\omega\omega_0 = \frac{1}{2Q}\frac{I_{inj}}{I_{osc}}\frac{1}{\sqrt{1-\left(\frac{I_{inj}}{I_{osc}}\right)^2}} \tag{4.7}$$

Given the tank quality factor, the locking range is increased by increasing I_{inj}/I_{osc}. Considering that I_{inj} is usually smaller than I_{osc}, the latter primarily determines the oscillation amplitude, i.e. I_{inj} should be maximized for maximum locking range. Referring to 4.7, this is achieved either maximizing the driving amplitude V_{in}, the biasing current I_2 or the device width of push-push locking pair, $M2' - 2''$.

The equation number 4.7 is compared against the simulation results of a design example where $Q = 5$. A good agreement between simulations and prediction is achieved as shown in figure 4.10. As expected the frequency locking range increases with the amplitude of the input signal. A locking range on the order of 20% is obtained with a relatively low input power of $0dBm$.

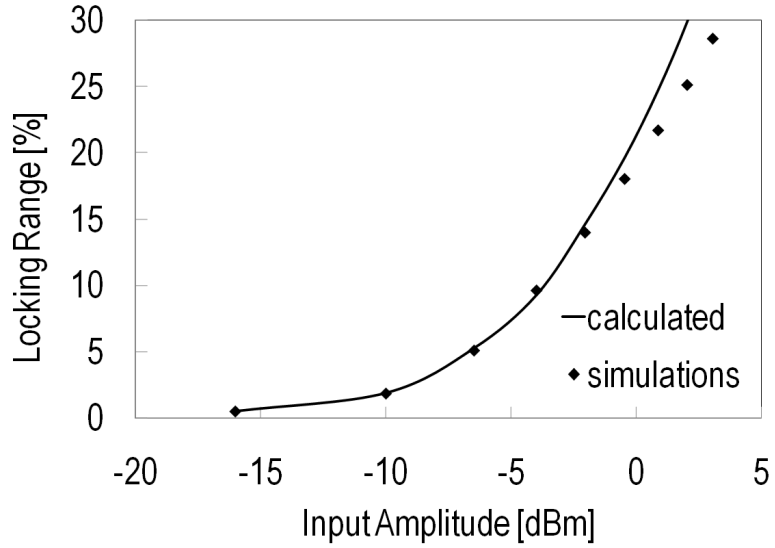

Figure 4.10: Calculated (line) and simulated (dots) one-side locking range.

4.4 Circuit design

The doubler has been designed for a target output frequency of $115GHz$ in a $65nm$ CMOS technology provided by STMicroelectronics. Resonator capacitors are device parasitics only. The center capacitor is also implemented with the gate capacitance of a dummy nMOS device. The loaded quality factor is relatively low (~ 4). Losses are primarily determined by parasitic device resistors (gate and bulk resistances) and output conductances. The resonator inductor has been maximized, for maximum output amplitude at given power consumption. It is a $80pH$ single turn spiral of $2.6\mu m$ width trace, realized shorting together the two top-most Cu metal layers. Estimated quality factor is 15. For maximum series impedance and self resonance frequency, the choke inductor, which provides the supply to the circuit, is realized as a $15um$ diameter 3.5 turns spiral of a thin $0.4\mu m$ width trace in the topmost metal only. From electromagnetic simulations, the self resonant frequency of the two inductors is close to $200GHz$. $M1$ is $20\mu m/65nm$ while $M2, 2'$ are $10\mu m/65nm$ each one. Transistor sizes are relatively

small leading to a low capacitance ($\sim 15fF$ on each input) loading the half-frequency signal source. The two biasing currents have been set equal to $3mA$ and supply voltage is $1V$. From simulations, assuming $300mV$ swing at $57.5GHz$ on each push-push transistor, the frequency locking range is 18% while the single-ended peak output swing, when driving the measurements buffer shown in figure 4.11, is $340mV$. The

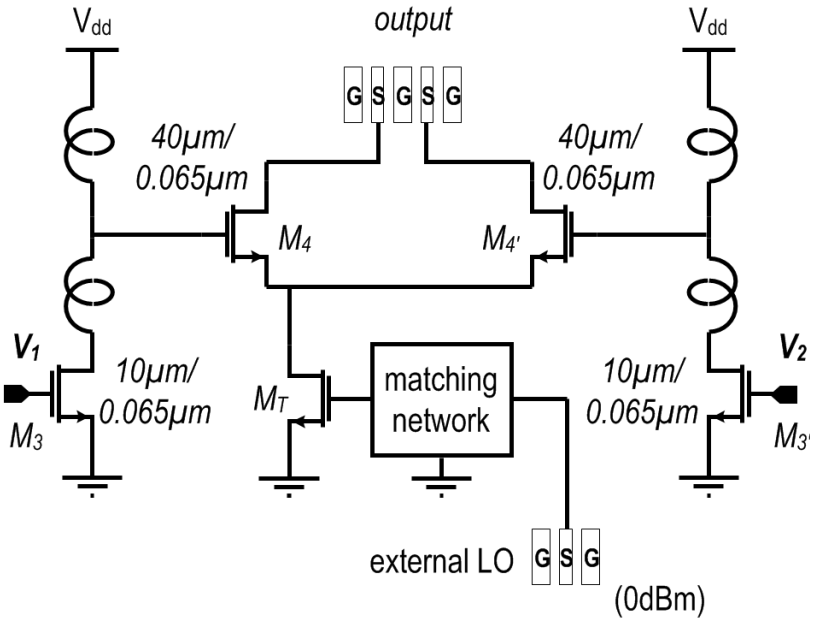

Figure 4.11: Buffer stage of the doubler.

first stage is a differential common-source pair ($M3-3'$) with inductive loads while the second is a differential pair ($M4-4'$), supplied off-chip with bias-tees, driving the 50Ω load of the measurement setup. If an off-chip local oscillator (LO) signal is superimposed to the bias voltage of the tail transistor (M_T), it works as a down-conversion mixer translating the multiplier output signals at a lower frequency. The complete buffer draws $17mA$ from $1V$ supply. The circuit displays a simulated loss of $3dB$ and $16dB$ when the second stage works as a standard differential pair and down-conversion mixer respectively. Two different chip versions have been realized. In the first, the multiplier is locked by an off-chip half frequency reference. A transformer balun has been

integrated to make the input signal differential. Schematic of the input network is shown in figure 4.12a. The $r_g - C_{gs}$ circuits (in gray) represent the input impedance of the push-push pair. C_{gs} and C_1 resonate with the secondary winding of the transformer leading to an equivalent parallel resistance seen from the primary winding of 200Ω. Resistor R_1 reduces the input impedance to 50Ω to terminate the input signal. The voltage gain from the primary to the secondary is ~ 1.5. The bias voltage of the push-push pair is provided through the center-tap of the secondary. In a second chip version, the multiplier is locked by an on-chip half-frequency VCO . The schematic is shown in figure figure 4.12b. It is a standard nMOS differential pair LC-tank oscillator tuned with accumulation-mode MOS varactors and two switchted poly-well capacitors to lower the tuning gain. Supplied from $750mV$, it dissipates $6mW$.

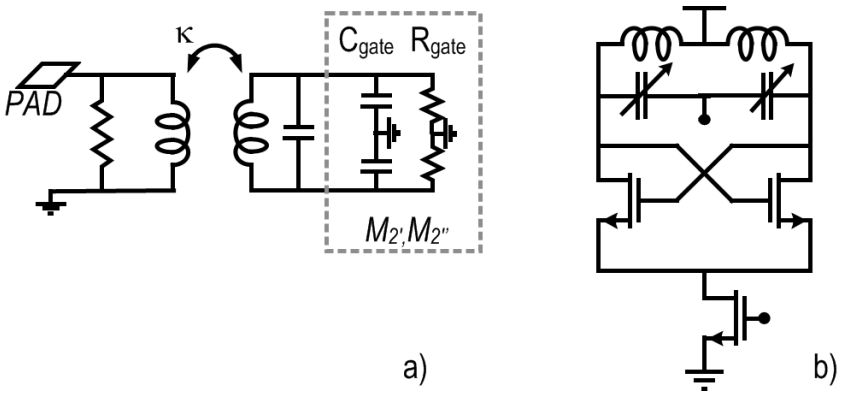

Figure 4.12: (a) Input network for the doubler driven off-chip and (b) half frequency VCO.

4.5 Experimental Result

Photomicrographs of the realized test chips are shown in figure 4.13. The left photo shows the prototype with balun while the right figure shows the test chip with the doubler driven by the VCO. Active area is $120\mu mX120\mu m$ for the doublers. Dies have been glued on PCB for exper-

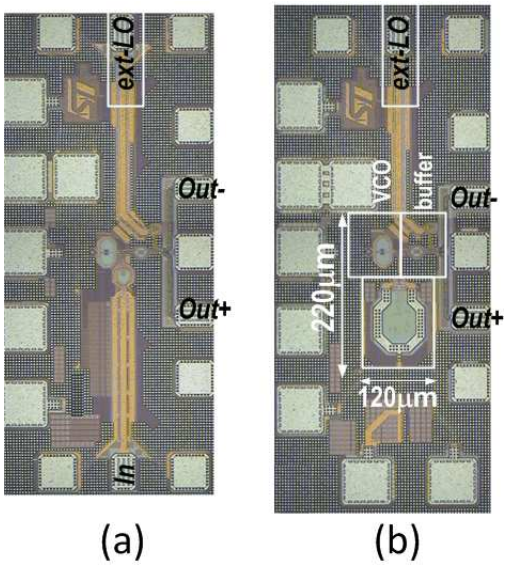

Figure 4.13: Photomicrographs of the realized test-chips. (a) doubler with on-chip balun; (b) doubler with on-chip VCO.

imental characterization. Supply and DC biasing are provided through bond-wires while the high frequency input and output signals are provided through micro-probes as shown in figure 4.14. Two alternative

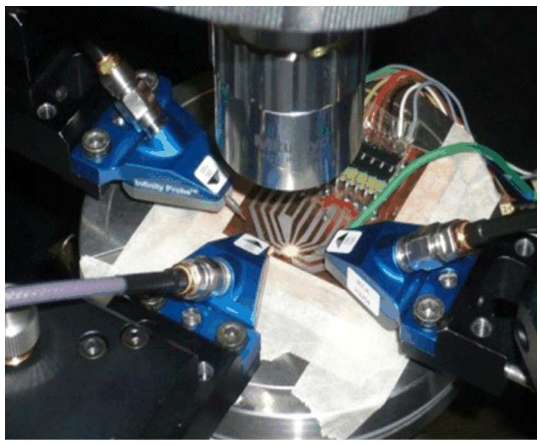

Figure 4.14: Photo of detail of measurement setups, the micro-probes and the board with chip.

experiments have been set-up for the characterization of the doubler.

They are shown in figure 4.15a. When the second buffer stage is operated as a down-conversion mixer, two signal sources provide the input signal and the LO, as shown in figure 4.15a. The output is measured by means of a Spectrum Analyzer, extended to V-band ($50 - 75GHz$) through a compatible external harmonic mixer. The doubler has been tested also as shown in figure 4.15b, without translating on-chip the outputs to a lower frequency. In this case W-band ($75 - 110GHz$) waveguide probe and harmonic mixer have been employed. Measurements are carried out up to $125GHz$ frequency, as previously reported in [68], beyond the nominal bandwidth of the waveguides. Estimated in-band losses have been linearly extrapolated up to the measured frequency [68]. Figure 4.16 shows the measured output power versus the doubler output frequency with a constant input power of $0dBm$. The top curve corresponds to the setup of 4.15b. Maximum output power at center frequency is $-2.6dBm$. Being the simulated buffer loss equal to $3dB$, the single ended zero-peak voltage swing at the doubler outputs is estimated to be $330mV$, and the voltage conversion gain is $0dB$, in good agreement with simulations. The lowest curve in figure 4.16 is referred to the setup of figure 4.15a, where the output signal is first down-converted on-chip. The LO frequency was set to $55GHz$ leading to an intermediate frequency spanning from 56 to $73GHz$. Being the simulated conversion loss of the buffer $13dB$ larger, when it is configured as a mixer, the two measurement setups give consistent results. Due to the lack of differential probes and waveguide baluns, the two outputs of the frequency doubler have been tested single-ended. Measured amplitude difference between the two outputs, shown in figure 4.17, is always less $1dB$, i.e. within the measurement inaccuracy of the setup. Test of the phase noise degradation at the output is shown in figure 4.18. The lowest curve is the phase noise of the input source. The top curve is the phase noise at the output. At low offset frequency, the output phase noise is $6dB$ higher than at the input, as expected [69]. The measured output phase noise above $300kHz$ offset is bounded by the setup noise floor which is relatively high ($\sim -110dBc/Hz$), determined by the large conversion losses of the harmonic mixer and probe.

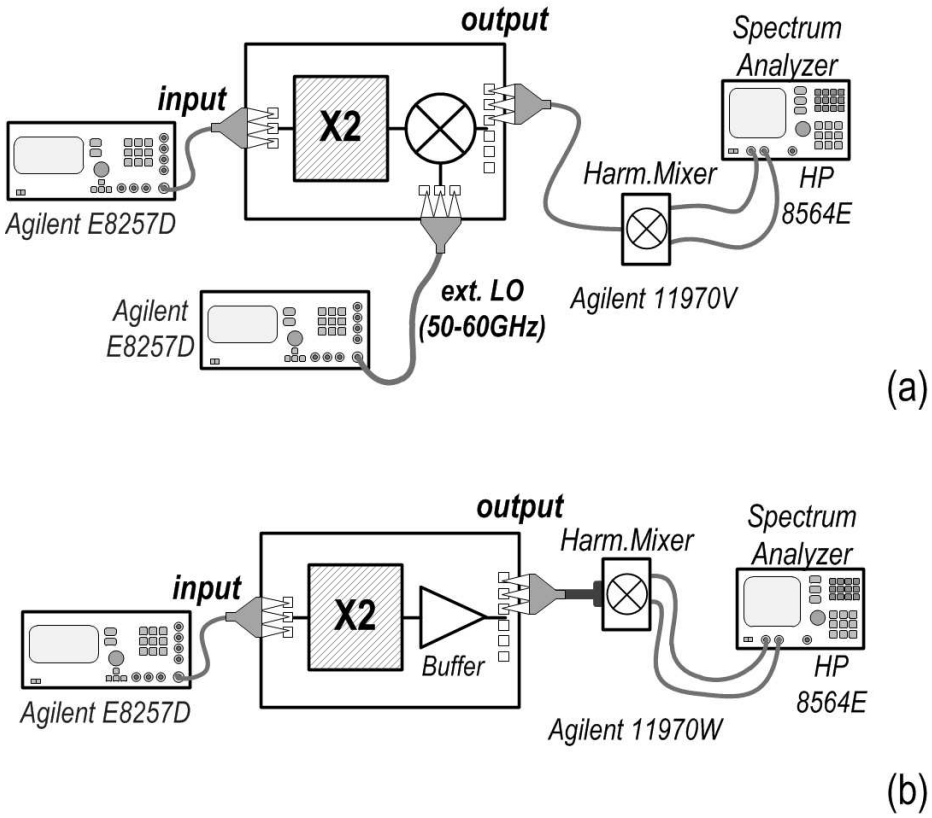

Figure 4.15: Experimental setup for testing the doubler. Characterization with on-chip down-conversion to V-band (a) and at the actual output frequency (b).

Finally the experimental performances of the circuit are summarized in table 4.5 and compared against recently reported CMOS frequency doublers for millimeter-waves applications.

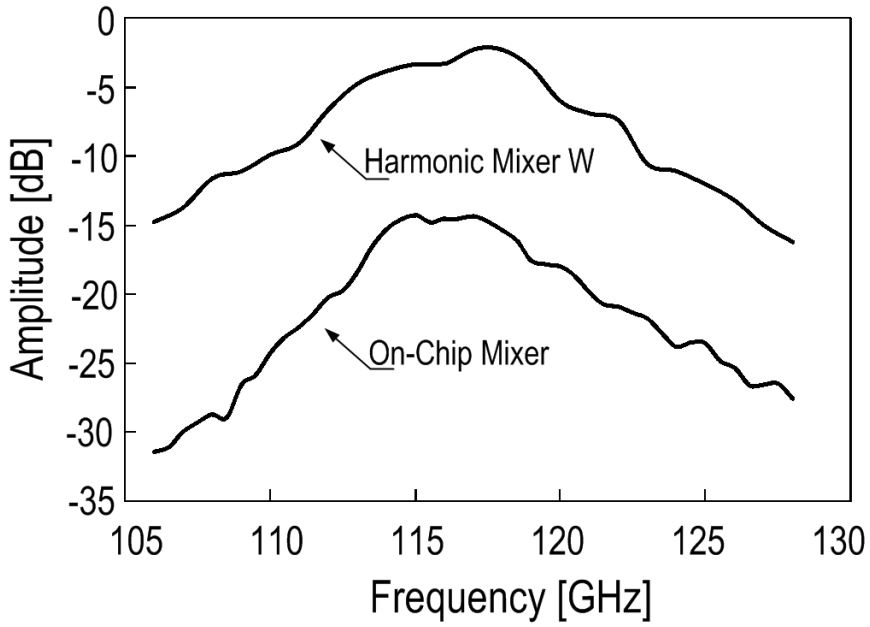

Figure 4.16: Measured power versus multiplier output frequency.

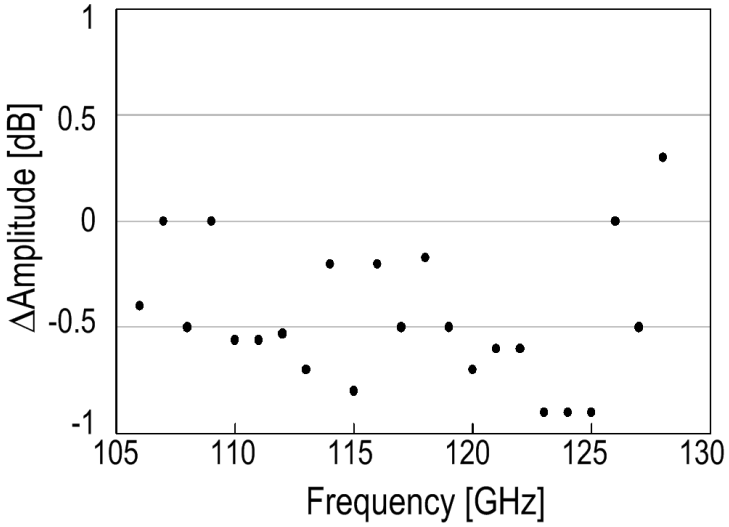

Figure 4.17: Measured amplitude difference between the two outputs of the frequency doubler.

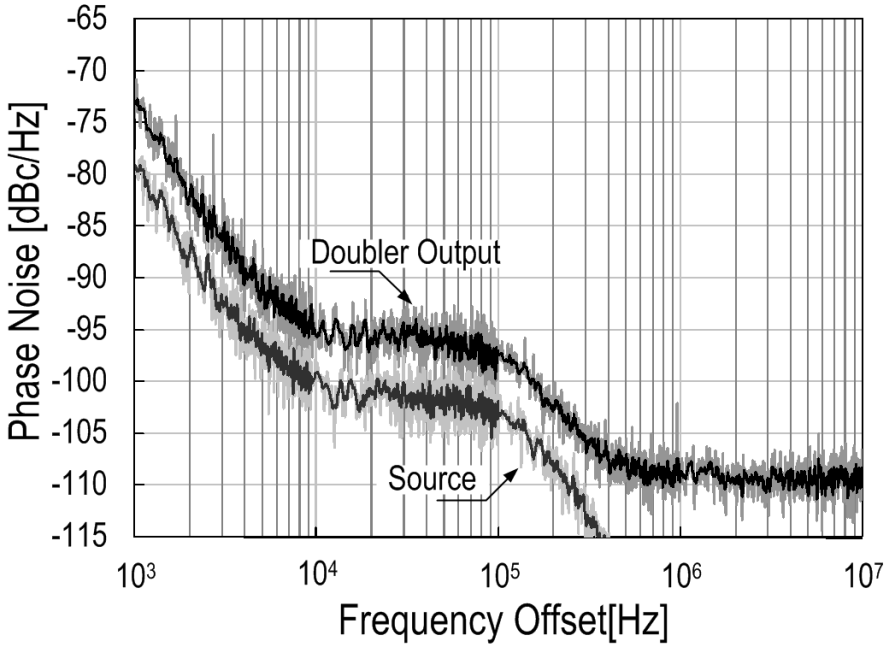

Figure 4.18: Phase noise of the input source and at the output of the F-band frequency doubler.

Ref	f_{out}	Conv. Gain	P.diss (core+buffer)	Out
	[GHz]	[dB]	[mW]	s.e/diff
[54]	27	1.5	10	s.e.
[70]	40	-15.8	4	s.e.
[70]	60	-15.3	4	s.e.
[58]	54	-0.45	9 (4+5)	s.e.
This Work	*115*	*6*	**23 (6+17)**	*diff.*

Finally the doubler with on-chip half frequency VCO has been tested [63]. The complete SubTHz frequency generator displays a 13.1% frequency tuning range around $115GHz$. When locked by the VCO, the measured phase noise profile is shown in figure 4.19 and, at $10MHz$ offset, it is reduced to $-107dBc/Hz$ with a total power dissipation (VCO and doubler) of $12mW$. The performances of the VCO and multiplier combination, proposed in this work, are summarized and compared against stand-alone fundamental frequency VCOs in the table reported below. In the last column, the FOM_T normalizes frequency 4.8, power dissipation, phase noise and tuning range [71]. The proposed solution shows more than $10dB$ improvement against state of the art.

$$FOM_T = L(\Delta\omega) - 20\log\left(\left(\frac{\omega_0}{\Delta\omega}\right)\left(\frac{FTR}{10}\right)\right) + 10\log\left(\frac{P_{diss}}{1mW}\right) \tag{4.8}$$

Ref	f_0	P.N.@10MHz	T.R.	Power	FOM_T
	[GHz]	[dBc/Hz]	%	[mW]	[dB]
[23]	98.0	-102.7	2.55	7	-162.20
[23]	105.2	-97.5	0.19	7.2	-134.94
[72]	114.0	-107.6	2.10	8.4	-165.94
[21]	109.2	-105.2	2.24	9.6	-163.15
[21]	122.8	-100.2	1.30	9.6	-154.44
[21]	139.6	-93.0	0.86	9.6	-144.76
[71]	102.2	-100.9	4.12	7.6	-164.58
This Work	**115**	**-107**	**13.1**	**12**	**-179.8**

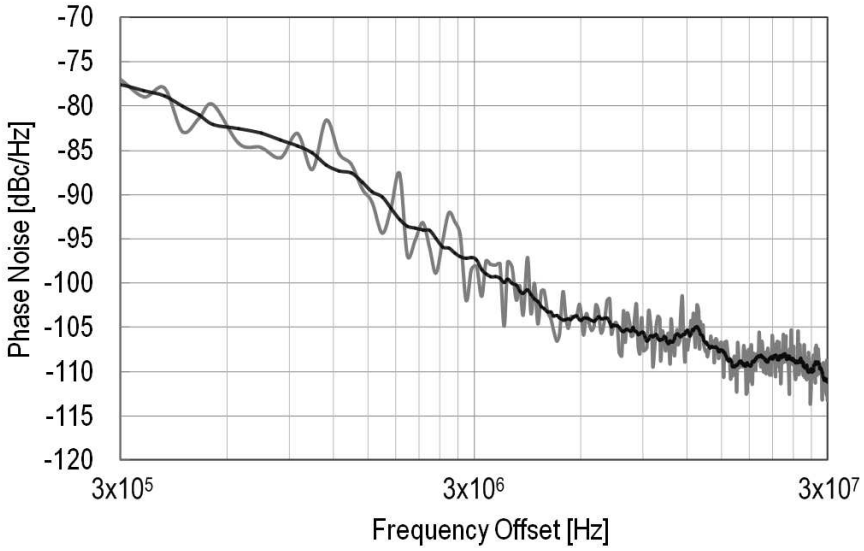

Figure 4.19: Phase noise at the multiplier output when driven by the on-chip half-frequency VCO.

Chapter 5

Conclusion

The PhD. thesis focused on issues related to the generation of local oscillators at mm-Waves. Two new circuit solutions have been proposed concerning the frequency generation: a $60GHz$ quadrature VCO and a $120GHz$ frequency doubler.

The quadrature VCO, based on inter-stage passive coupling, is proposed to greatly reduce the conversion of flicker noise into phase noise. Measured performances of prototypes realized in $65nm$ CMOS demonstrate a remarkable advantage compared to state of the art. The solution is suitable for direct conversion architectures and may enable compact low-power phased array systems.

The new frequency doubler is based on a differential LC oscillator locked by the 2^{nd} harmonic generated by a pair of transistors arranged in push-push configuration. Compared to a simple push-push pair driving a tuned load, widely proposed in the literature, the presented technique leads to smaller input capacitance, higher conversion gain and provide a differential output at low power dissipation. Performances have been proven experimentally on two different configuration of the test-chip in $65nm$ CMOS technology.

Publications

Journals

- E. Monaco, M. Pozzoni, F. Svelto, A. Mazzanti, Injection-locked CMOS frequency doublers for u-wave and mm-wave applications, *IEEE Journal of Solid-State Circuits*, August 2010, VOL. 45, NO. 8, pp. 1565 1574

- Decanis, U., Ghilioni, A., E. Monaco, Mazzanti, A., Svelto, F, A Low-Noise Quadrature VCO Based on Magnetically Coupled Resonators and a Wideband Frequency Divider at Millimeter Waves, *IEEE Journal of Solid-State Circuits*, December 2011 , VOL. 46, NO. 12, pp. 2943 - 2955

Conferences

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