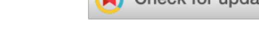

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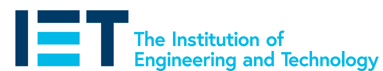

Computational-Efficient IGBT and Diode Thermal Modelling Methodology With High Accuracy

Ciro Alosa[1] | Abraham M. Alcaide[2] | Alejandro Stowhas-Villa[3] | Jhonattan G. Berger[4] | Fabio Immovilli[1] | Christian A. Rojas[3] | Ricardo Lizana F[5] | Giampaolo Buticchi[6] | Samir Kouro[3] | Jose I. Leon[2,7]

[1]DISMI - Department of Sciences and Methods for Engineering, University of Modena and Reggio Emilia, Reggio Emilia, Italy | [2]Electronic Engineering Department and with ENGREEN Lab. of Engineering for Energy and Environmental Sustainability, Universidad de Sevilla, Seville, Spain | [3]Electronics Department, Universidad Técnica Federico Santa María, Valparaíso, Chile | [4]Laboratory for Mechatronics and Renewable Energy Systems (LMRES), HM Munich University of Applied Sciences, Munich, Germany | [5]Energy Center of Universidad Catolica de la Santisima Concepcion, Concepcion, Chile | [6]Faculty of Science and Engineering, University of Nottingham Ningbo China, Ningbo, China | [7]School of Astronautics, Harbin Institute of Technology, Harbin, China

Correspondence: Giampaolo Buticchi (buticchi@ieee.org)

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ABSTRACT

In an industrial context where high reliability is an increasingly important requirement, thermal modelling of power semiconductors becomes necessary for diagnostics and prognostics. This paper proposes a simulation-based methodology that can estimate junction temperatures in insulated gate bipolar transistors and diodes much faster than conventional methods with an improved accuracy. The approach is based on a combination of conventional steady state simulation techniques with a post-processing stage. The analysis is carried out by first calculating the conduction and switching losses and then obtaining the junction temperature by using the device thermal network. The obtained results (including both simulations and experiments) are compared to state-of-the-art methods, highlighting the accuracy of the proposed method.

1 | Introduction

Power electronic systems have been the enablers of the energy transition and are at the cornerstone of power generation, transmission, and utilization. As an example, and taking into account all power converters present in the technical literature, the silicon-based insulated gate bipolar transistor (IGBT) two-level voltage source inverter (2L-VSI) is the mainstream solution in many industrial applications. This power converter structure is shown in Figure 1 in a grid-connected application. In this context, currently IGBTs and diodes are critical components in power systems. They are widely used in multiple industrial applications, such as electric vehicles and renewable energy systems. The reliability and performance of these components depend on the variation in junction temperature, which can significantly affect their operating characteristics and service life. Therefore, accurate estimation of junction temperatures is crucial in the design and optimization of power electronic systems.

Modern power electronics require an accurate prediction of their remaining useful lifetime (RUL) to schedule an active maintenance plan to reduce the operating cost [1–3]. Among the critical components of a power converter, semiconductors and capacitors are the most fragile ones [4, 5].

In recent years, the concept of digital twin has gained significant attention in various industries, including power electronics. A digital twin is a virtual replica of a physical system that can be used to simulate its behaviour and performance in a digital environment. Several possibilities are offered by the digital twin paradigm [6], which can be summarized in providing accurate and reliable predictions of the system behaviour and

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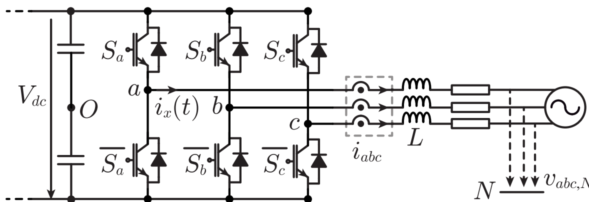

FIGURE 1 | Two-level insulated gate bipolar transistor (IGBT)-based voltage source inverter (2L-VSI) in grid connection application example

performance, enabling engineers to optimize its design and operation. Additional features, such as estimation of parasitic parameters, can be added to increase the accuracy [7, 8]. Digital twin can also be updated to estimate the thermal impedance of the power semiconductors [9]. This has been implemented for fault detection and health assessment for applications such as electric vehicles [10] or renewable energy systems [11].

For digital twin purposes or for reliability estimation, there is the need for accurate but also fast thermal models. In this regards, several techniques are available to engineers, from finite elements simulations (FEM), to circuit simulators, to simplified and analytical models. As an example, [12] presents physics-based electrothermal models for high-power semiconductors like GTOs and diodes, which are implemented in PSpice to enable transient temperature simulation and show excellent agreement with experimental measurements. Unlike simpler behavioural models, these models use fundamental semiconductor equations to ensure accuracy across a wide range of operating conditions.

In [13] a Fourier series-based thermal model that enables fast and accurate electrothermal simulation of power semiconductor devices, outperforming traditional RC network methods by more accurately predicting transient junction temperatures.

In [14] a frequency-based thermal modelling is proposed, where the low-pass and high-frequency components of the generated heat are separated, so that the case temperature and high-frequency variations can be more efficiently calculated. This has been expanded in [15], where a higher-order low-pass filter is adopted for higher accuracy.

In [16, 17] a detailed analytical model for IGBT devices taking into account the instantaneous loss waveform and the consequent temperature fluctuation is presented. This model relies on the discretization of the conduction losses curve of an IGBT when the inverter is driven with a sinusoidal PWM (SPWM) strategy, leading to very accurate results for the calculation of the temperature ripple by exploiting an equivalent foster network, at the expense of a high computational cost. In this paper, the original contribution is to propose an averaged model-based methodology that can predict junction temperatures in IGBTs and diodes much faster than conventional methods with similar accuracy. The proposed approach is based on a combination of conventional averaged-model calculation technique in steady state with a post-processing stage. This tool can handle complex power electronic applications and systems, potentially allowing for the implementation of digital twin into the microcontrollers on-board the power electronics to be executed in real time. Another application is the possibility to generate quickly thermal data of complex systems to be used in ANN training.

The rest of the paper is organized as follows: Section 2 summarizes the power loss calculations for IGBT and diodes. Section 3 presents the proposed thermal estimation procedure of the IGBT with diode. Section 4 analysed the accuracy of the proposed method by several numerical simulations whereas Section 5 demonstrates its accuracy in the experimental rig. Finally, in Section 6 some conclusions are drawn.

1.1 | Novelty and Contribution

This paper proposes a novel simulation-based methodology for estimating junction temperatures in IGBTs and diodes. The key contributions which are present at the same time are:

- **Computational efficiency with high accuracy**: The proposed method decouples the problem into an average temperature simulation and a post-processing ripple calculation. This structure achieves a significant reduction in computational time compared to conventional transient simulation tools while maintaining accuracy comparable to these detailed models, as shown in Sections 4 and 5.
- **Harmonic-based thermal ripple post-processing**: A novel frequency-domain post-processing technique is introduced to calculate the temperature ripple. By applying the Fourier transform to the loss waveform and the device's thermal impedance, the method efficiently reconstructs the junction temperature ripple caused by the fundamental load frequency, avoiding the need for simulating the entire high-frequency switching period.
- **Enhanced conduction loss model**: Unlike simplified models that use constant parameters and consider the simple sinusoidal modulation, the proposed methodology incorporates a piecewise-linear discretization of the semiconductor's forward characteristics (v_{on}–i_{on} curves). This model, detailed in Section 2.1, accounts for their nonlinear dependence on both current and temperature, directly improving accuracy.
- **Application-oriented design**: The computational efficiency of the approach is not an end in itself but is designed to enable practical applications that are infeasible with slower models. This includes real-time digital twin implementations on embedded microcontrollers and the rapid generation of large datasets for training artificial neural networks (ANNs) for health monitoring and prognostics.

2 | Average Power Loss Modelling of an IGBT With the Free-Wheeling Diode

In this section, the average loss calculation procedure for an IGBT (Q) and its anti-parallel diode (D) in the conventional 2L-VSI Figure 2 is presented, where the upper switch is named H while lower switch is L. The calculation of the total loss for each device (Q or D) is given by the sum of its conduction losses P_c and its switching losses P_{sw}. Both, conduction and switching loss, depend on the modulation strategy adopted to operate the power

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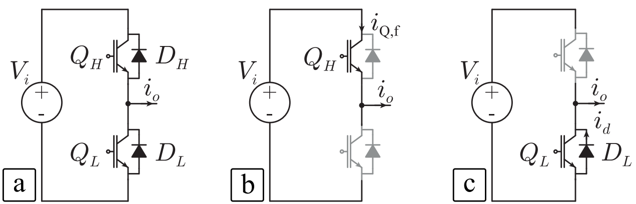

FIGURE 2 | (a) Half-bridge corresponding to a phase of a three-phase inverter. (b) Forward conduction state for a half-bridge converter. (c) Reverse conduction state for a half-bridge.

converter. Despite all the modulation techniques available in the technical literature, SPWM and SPWM with a third harmonic injection (THI-SPWM) are the most popular so far [18]. This work is focused on the THI-SPWM technique since it allows to extend the modulation index range by 15.47%. In any case, other continuous modulation alternatives could be considered in a similar manner.

2.1 | Average Conduction Loss

In a conventional operation applying the THI-SPWM method, the DC/AC power converter output currents can be approximated by a sinusoidal waveform composed by a sum of fundamental frequency plus a third harmonic injection (f_1, f_3). It is important to note that the output current waveforms generate a variation in the conduction loss which leads to a junction temperature (T_j) fluctuation in power devices. Therefore, this phenomenon should be introduced in the thermal analysis of the power device for a better estimation of the T_j of the power devices and their RUL.

The average conduction loss per fundamental period of a power semiconductor device (P_c) is obtained from the instantaneous conduction loss (p_c), which is expressed as:

$$p_c(\alpha) = m(\alpha) v_{on} i_{on} \tag{1}$$

where $m(\alpha)$ is defined in the interval $0 < \alpha \leq 2\pi$ and represent the duty-cycle applied to the device. Parameters v_{on} and i_{on} are the on-voltage and on-current of the power device during the conduction phase, respectively. In addition, v_{on} is also a function of the current during the on-state (i_{on}) as well as the junction temperature of the power device (T_j). In the following, the conduction loss expression is particularized for an IGBT and a diode.

For each power device (sub-index x is referred to the power device, Q or D), the on-voltage of the device is defined as:

$$v_{x,\mathrm{on}} = R_{x,\mathrm{on}} i_{x,\mathrm{on}} + V_{x,0} \tag{2}$$

where $R_{x,\mathrm{on}}$ is the on-resistance, which also depends on the junction temperature ($T_{j,x}$) and the on-current ($i_{x,\mathrm{on}}$). The term $V_{x,0}$ is the no-load voltage of the device which depends on $T_{j,x}$ as well.

Considering the half-bridge architecture shown in Figure 2, the instantaneous conduction loss of the upper switch (switch means IGBT plus its free-wheeling diode) can be expressed as follows.

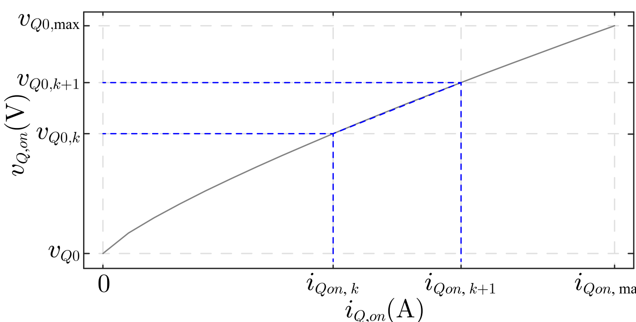

FIGURE 3 | IGBT forward characteristic v_{Qon}–i_{Qon} for a T_{jQ}

$$p_c(\alpha) = p_{c,Q}(\alpha) + p_{c,D}(\alpha) \tag{3a}$$

$$= d_H(\alpha) v_{Q,\mathrm{on}} i_o + d(\alpha) v_{D,\mathrm{on}}(-i_o) \tag{3b}$$

where $i_{Q,\mathrm{on}} = i_o$ and $i_{D,\mathrm{on}} = -i_o$. Moreover, d_H is the duty ratio applied to the upper switching device shown in Figure 2. Then, the average value in a fundamental period of the conduction loss in the upper switch can be calculated as:

$$P_{c,Q} = \frac{1}{2\pi} \int_0^{\pi} p_{c,Q}(\alpha) \mathrm{d}\alpha \tag{4a}$$

$$P_{c,D} = \frac{1}{2\pi} \int_{\pi}^{2\pi} p_{c,D}(\alpha) \mathrm{d}\alpha \tag{4b}$$

where $\alpha \in [0, \pi]$ is the forward conduction phase in the IGBT, while $\alpha \in [\pi, 2\pi]$ is the reverse conduction phase produced in the diode.

As shown in Figure 3, a non-linear relationship exists between $v_{\mathrm{Q,on}}$ and $i_{\mathrm{Q,on}}$. To enhance modelling accuracy, the forward characteristic v_{on}–i_{on} is partitioned into K sub-intervals, where the corresponding on-voltage (for Q and D) is expressed as:

$$v_{x,\mathrm{on}} = \mathrm{R}_{x,\mathrm{on}}|_k \left(i_{x,\mathrm{on}} - \mathrm{I}_{x,\mathrm{on}}|_k\right) + \mathrm{V}_{x0}|_k \tag{5}$$

It should be emphasized that the K sub-intervals may be either uniformly or non-uniformly distributed, depending on the degree of non-linearity, in order to achieve a more accurate representation.

Accordingly, i_{Qon} and i_{Don} belong to the kth interval, defined as:

$$i_{x,\mathrm{on}} \in \left(\mathrm{I}_{x,\mathrm{on}}|_k, \mathrm{I}_{x,\mathrm{on}}|_{k+1}\right) \tag{6}$$

Similarly, the coefficients $\mathrm{R}_{\mathrm{Qon}}|_k$ and $\mathrm{R}_{\mathrm{Don}}|_k$ of the kth interval can be obtained as:

$$\mathrm{R}_{x,\mathrm{on}}|_k = \frac{\mathrm{V}_{x0}|_{k+1} - \mathrm{V}_{x0}|_k}{\mathrm{I}_{x,\mathrm{on}}|_{k+1} - \mathrm{I}_{x,\mathrm{on}}|_k} \tag{7}$$

By introducing Equation (5) into Equation (3b), instantaneous conduction loss can be rewritten as:

$$p_{c,x}(\alpha) = d_H(\alpha)\left(\mathrm{R}_{x,\mathrm{on}}|_k \left(i_{\mathrm{on}} - \mathrm{I}_{x,\mathrm{on}}|_k\right) + \mathrm{V}_{x,0}|_k\right) i_{x,\mathrm{on}}$$
$$= \mathrm{R}_{x,\mathrm{on}}|_k d_H(\alpha) i_{x,\mathrm{on}}^2 \tag{8a}$$

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$$+ \left(\mathrm{V}_{x,0}|_k - \mathrm{R}_{x,\mathrm{on}}|_k \mathrm{I}_{x,\mathrm{on}}|_k\right) d_{\mathrm{H}}(\alpha) i_{x,\mathrm{on}} \tag{8b}$$

It is important to remark that all these parameters belong to the kth sub-interval, and they are functions of $i_{x,\mathrm{on}}$ and the $T_{j,x}$. In this sense, the proposed model takes into account the variation of the Q and D forward characteristic to provide a more accurate calculation of the resulting conduction losses.

Finally, after some mathematical manipulation, the conduction loss in a complete fundamental period is given by:

$$P_{c,x} = \mathrm{R}_{x,\mathrm{on}}|_k I_{x,\mathrm{rms}}^2 + \left(\mathrm{V}_{x,0}|_k - \mathrm{R}_{x,\mathrm{on}}|_k \mathrm{I}_{x,\mathrm{on}}|_k\right) I_{x,\mathrm{avg}} \tag{9}$$

showing the definition:

$$I_{x,\mathrm{avg}} = \frac{I_{\mathrm{p}}}{2\pi} \int_a^b d_{\mathrm{H}}(\alpha) \sin(\alpha) \mathrm{d}\alpha \tag{10}$$

$$I_{x,\mathrm{rms}}^2 = \frac{I_{\mathrm{p}}^2}{2\pi} \int_a^b d_{\mathrm{H}}(\alpha) \sin^2(\alpha) \mathrm{d}\alpha \tag{11}$$

where I_{p} is the phase current peak value fulfilling that $i_{\mathrm{o}}(\alpha) = I_{\mathrm{p}} \sin(\alpha)$. $\mathrm{R}_{x,\mathrm{on}}$ and $\upsilon_{x,\mathrm{on}}$ presented in Equations (5) and (7) are calculated as a function of the peak phase current I_{p}.

The expressions (10) and (11) should be evaluated in the correct interval of the fundamental period, that is $\alpha \in [0, \pi]$ for Q and $\alpha \in [\pi, 2\pi]$ for D. In addition, these expressions should be particularized for the specific modulation technique used to operate the converter; the conventional THI-SPWM in the case under study for this work. In this sense, the duty-cycle applied to the upper switch is described as:

$$d_{\mathrm{H}}^{\mathrm{THI-SPWM}}(\alpha) = d_{\mathrm{H}}^{f_1}(\alpha) + d_{\mathrm{H}}^{f_3}(\alpha) \tag{12a}$$

$$d_{\mathrm{H}}^{f_1}(\alpha) = \frac{1}{2}[1 + M_a \sin(\alpha + \varphi)] \tag{12b}$$

$$d_{\mathrm{H}}^{f_3}(\alpha) = \frac{1}{12} M_a \sin(3\alpha + 3\varphi) \tag{12c}$$

where the parameter $M_a \in [0, 1]$ is the modulation index, and φ is the power factor of the load connected to the half-bridge.

By introducing expression (12a) into Equation (9), the average conduction power loss considering the fundamental component for Q and D is obtained as:

$$P_{\mathrm{c},x}^{f_1} = \mathrm{R}_{x,\mathrm{on}}|_k I_p^2 \left[\frac{1}{8} + a \frac{M_a \cos(\varphi)}{3\pi}\right] + \left(\mathrm{V}_{x,0}|_k - [\mathrm{R}_{x,\mathrm{on}} \mathrm{I}_{x,\mathrm{on}}]|_k\right) I_p \left[\frac{1}{2\pi} + a \frac{M_a \cos(\varphi)}{8}\right] \tag{13}$$

where the parameter a takes the value 1 for Q and -1 for D. In a similar manner, the conduction loss associated with the third harmonic component is derived as follows:

$$P_{\mathrm{c},x}^{f_3} = -a \mathrm{R}_{x,\mathrm{on}}|_k I_p^2 \frac{M_a \cos(3\varphi)}{90\pi} \tag{14}$$

Finally, the total average conduction loss for Q and D considering the conventional THI-SPWM technique is given by:

$$P_{\mathrm{c},x}^{\mathrm{THI-SPWM}} = P_{\mathrm{c},x}^{f_1} + P_{\mathrm{c},x}^{f_3} \tag{15}$$

2.2 | Average Switching Loss

The calculation of the switching loss is carried out considering the switching energies of the devices E_{sw} that are commonly provided in the manufacturer's data sheet. These energy losses depend on the output current i_{o}, the gate resistance R_{g}, the input voltage V_{i} as well as the junction temperature T_{j}. For this reason, the switching energies can be obtained by using a multi-dimensional look-up-table defined by $E_{\mathrm{sw}} = f(i_{\mathrm{o}}, T_{\mathrm{j}}, R_{\mathrm{g}}, V_{\mathrm{i}})$.

The switching losses of Q are caused by the turn-on and the turn-off of the device, whereas in the D, the losses are only produced by the reverse recovery effect. In the case of the Schottky-type diode, the reverse recovery losses can also be neglected.

For a sinusoidal output current, $i_{\mathrm{o}} = I_{\mathrm{p}} \sin(\alpha)$, the switching losses can be expressed as a function of the switching energy as:

$$p_{\mathrm{sw}}(\alpha) = f_{\mathrm{sw}} E_{\mathrm{sw}} \tag{16}$$

During the forward conduction phase (i.e. $i_{\mathrm{o}} > 0$), the $\mathrm{Q_H}$ device works in hard-switching mode because the $\upsilon_{\mathrm{Q,on}}$ voltage is equal to the input voltage V_{i}. On the other hand, the Q_L device works in zero voltage switching (ZVS) since the $\upsilon_{\mathrm{Q,on}}$ voltage is equal to the diode no-load voltage $V_{\mathrm{D},0}$. Conversely, during the reverse conduction phase (i.e. $i_{\mathrm{o}} < 0$), the $\mathrm{Q_H}$ device works in ZVS, whereas $\mathrm{Q_L}$ device works in hard-switching. In both cases, the reverse recovery losses are given by the opposite diode with respect to the IGBT working in hard-switching. Considering the conventional half-bridge architecture shown in Figure 2a, the average switching loss of Q and D per fundamental period can be calculated as:

$$P_{\mathrm{sw},x} = \frac{f_{\mathrm{sw}}}{2\pi} \int_a^b e_{\mathrm{sw},x}(\alpha) \mathrm{d}\alpha \tag{17}$$

where $e_{\mathrm{sw},x}(\alpha)$ is the instantaneous switching energy curve for the corresponding device. The integral should be calculated in the corresponding region, that is, in $\mathrm{Q_H}$ when $0 \leq \alpha \leq \pi$, while they are present in $\mathrm{D_H}$ when $\pi \leq \alpha \leq 2\pi$. An analogous phenomenon occurs for the lower switch. The integral expressions in Equation (17) can be calculated by the discretization of these switching energy curves into K intervals by trapezoidal integration method (similarly, the selection of the integration method can be adjusted by the most appropriated technique), as shown in Figure 4.

$$P_{\mathrm{sw},x} = \frac{f_{\mathrm{sw}}}{2K} \sum_{k=1}^{K} E_{\mathrm{sw},x}(I_x|_k) \tag{18}$$

where $I_x|_k$ is defined as:

$$I_{\mathrm{Q}}|_k = I_{\mathrm{p}} \sin(k\Delta\alpha)$$
$$I_{\mathrm{D}}|_k = I_{\mathrm{p}} |\sin(k\Delta\alpha + \pi)|$$
$$\Delta\alpha = \frac{\pi}{K} = \alpha_{k+1} - \alpha_k \tag{19}$$

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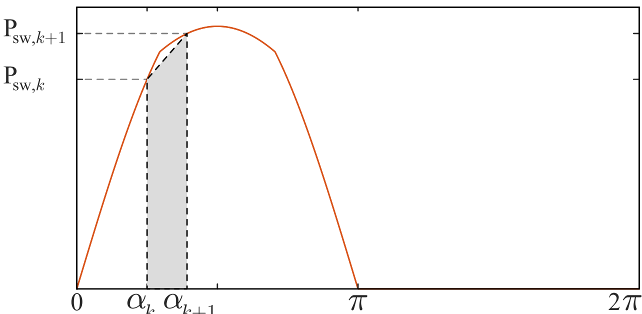

FIGURE 4 | Example of a trapezoidal discretization for the Q switching loss curve.

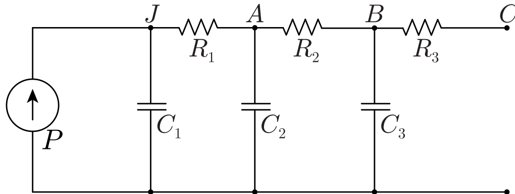

FIGURE 5 | Generic Cauer thermal network of a power electronic device, without heatsink.

Then, for a given operational condition (i.e. R_g, T_j, V_i), the average switching loss of Q and D can be calculated as:

$$P_{\text{sw,Q}} = \frac{f_{\text{sw}}}{2K} \sum_{k=1}^{K} \left[E_{\text{Q,on}} + E_{\text{Q,off}}\right] \tag{20a}$$

$$P_{\text{sw,D}} = \frac{f_{\text{sw}}}{2K} \sum_{k=1}^{K} E_{\text{D,rr}} \tag{20b}$$

where $E_{\text{Q,on}}$ and $E_{\text{Q,off}}$ are the Q on-energy and off-energy whereas and $E_{\text{D,rr}}$ is the diode reverse recovery energy. It is important to point out that the reverse recovery of the opposite diode causes the increment of the transistor turn-on energy, which is usually already taken into account in the manufacturer's datasheet [19].

3 | Thermal Estimation of the IGBT and Diode

In order to develop an accurate thermal model, the thermal network of a power electronic device can be represented by its Cauer thermal network. A generic Cauer network is represented in Figure 5 where the nodes represent the most notable part of the device. Normally, a three-stage Cauer thermal network presents a good response for the thermal behaviour of the device. The Cauer thermal network of a device can be directly provided by the manufacturer, or it can be obtained from the single pulse thermal response of the device by experimental fitting.

Each element of the thermal network has a physical meaning, where each node represents a real connection point of the device. To obtain the temperature variation, the loss P in the thermal model is represented as a heat generator connected to the device junction node J. The node C represents the case connection, where the heatsink impedance should be added. It is worth to notice that, since the device thermal capacitance is much smaller than the heatsink thermal capacitance, the transient response of the device temperature can be very well approximated by considering only the internal impedance of the device, thus neglecting the connection to the heatsink and the influence of the nearby devices.

The flow chart of the temperature estimation proposed in this work is illustrated in Figure 6. The calculation procedure for the temperature estimation of the Q and D devices is split into two different sub-processes: average temperature and thermal cycle calculation.

3.1 | Average Temperature Calculation

As a first step, a numerical simulation provides the average temperature profile according to the imposed mission power profile. This power profile varies according to load fluctuations and other external factors, such as ambient temperature. To this end, the power converter is numerically modelled using the average loss expressions previously presented.

Then, the parameters involved on the calculation of the conduction loss (see Section 2.1 should be calculated every simulation step since these coefficients depend not only on the peak value of the phase current, but also on the different parameters of the Q and D devices discussed previously.

The average conduction and switching power loss values ($P_{\text{c},x}$ and $P_{\text{sw},x}$) of the Q and D devices are obtained by using the expressions introduced in Section 2.

After obtaining $P_{\text{c},x}$ and $P_{\text{sw},x}$, the corresponding average junction temperature $T_{\text{j},x}$ is obtained considering the total power loss in the corresponding Cauer network. This Cauer network can be as complex as required to consider different physical aspects such as their relative location in the power module or the location on the heatsink, to mention a few. Please, note that the obtained $T_{\text{j},x}$ is used as a feedback for the calculations of the evolution of the parameters in consecutive simulation steps used in Section 2.1.

3.2 | Thermal Cycle Calculation

After performing the average numerical simulation for the estimation of the average junction temperature $T_{\text{j},x}$ for each device under study, a post-processing numerical method calculates the periodic temperature ripple caused by the operating conditions at the fundamental frequency, neglecting the high-frequency harmonic components. This temperature ripple will be superimposed on the previously calculated average $T_{\text{j},x}$. Please note that $P_{\text{c},x}$ and $P_{\text{sw},x}$ are calculated based on operating conditions and data from the power devices for each fundamental cycle according to the modulation technique using the previous expressions. This post-processing numerical method to calculate the temperature ripple is as follows:

1. The data obtained from the average numerical simulation is divided into a certain number of intervals, which depend on the fundamental frequency f_1 of the system and the total length of the simulated scenario under study. Note that f_1 can vary during the operation of the converter, so

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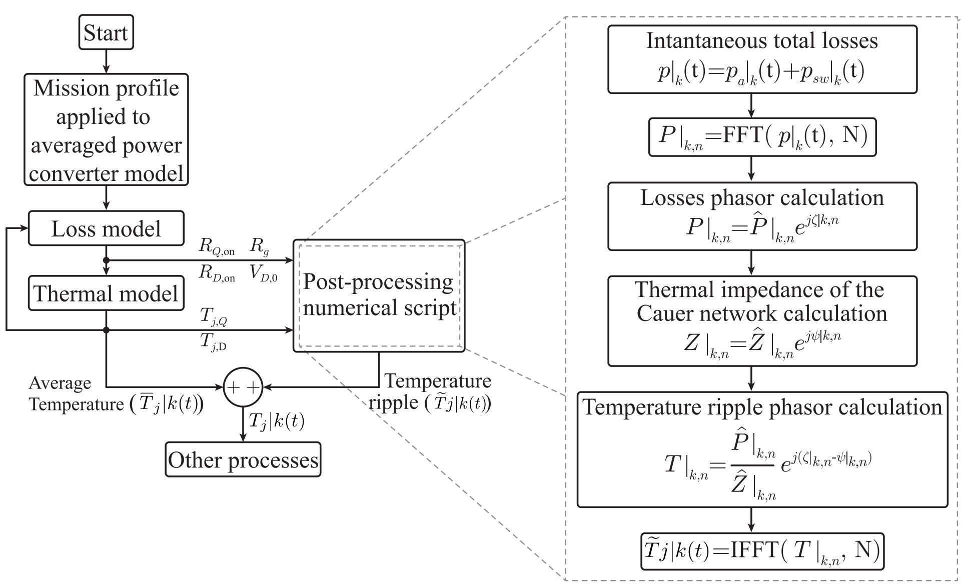

FIGURE 6 | Flowchart of the proposed method to calculate the power device temperature based on the average conduction loss and the periodic profile at the fundamental frequency.

this procedure is not valid only for frequency-fixed power systems. For example, for a total simulation time equals to $t_{\max}$ and considering that the fundamental frequency changes during the operation, for each fundamental frequency $f_1|_k$, the number of intervals considered for that frequency is equal to $\Delta t|_k f_1|_k$, where $\Delta t|_k$ is the kth time interval corresponding to the fundamental frequency $f_1|_k$ and $\sum_k \Delta t_k = t_{\max}$.

2. Each interval $\Delta t|_k = t_{k+1} - t_k$ is split-off into Z parts, where $\delta t|_z = \frac{\Delta t|_k}{Z}$ is the sub-interval of each kth time interval. For each sub-interval, and according to the adopted modulation strategy, the duty-cycle applied for each power device under study is calculated. Then the following procedure is applied:
   a. The instantaneous conduction and switching loss curves are calculated, and the total loss curve $p|_k(t) = p_c|_k(t) + p_{sw}|_k(t)$ is obtained;
   b. The Fourier transform is performed on the total loss curve $p|_k(t)$ and N harmonics are obtained (the dc value is excluded since only the ripple is evaluated);
   c. For each nth harmonic, a loss phasor $\boldsymbol{P}|_{\boldsymbol{k,n}} = \hat{P}|_{k,n}e^{j\zeta|_{k,n}}$ is calculated;
   d. The nth thermal impedance of the Cauer network $\boldsymbol{Z}|_{\boldsymbol{k,n}} = \hat{Z}|_{k,n}e^{j\psi|_{k,n}}$ is evaluated at each harmonic frequency $f_n = nf_1$;
   e. The temperature ripple phasors are calculated by dividing the loss phasors by the thermal impedance:

$$\widetilde{\boldsymbol{\Theta}}_{\mathrm{J}}|_{\boldsymbol{k,n}} = \hat{\Theta}_{\mathrm{J}}|_{k,n}e^{j(\zeta|_{k,n}-\psi|_{k,n})} \tag{21}$$

$$\hat{\Theta}_{\mathrm{J}}|_{k,n} = \frac{\hat{P}|_{k,n}}{\hat{Z}|_{k,n}} \tag{22}$$

   f. Finally, the time-variant signal is reconstructed from the N phasors, and thus the temperature ripple profile is obtained:

$$\widetilde{\Theta}_{\mathrm{J}}|_k = 2\sum_{n=1}^{N}\hat{\Theta}_{\mathrm{J}}|_{k,n}\cos\left(n\omega_1 t + \zeta|_{k,n} - \psi|_{k,n}\right), \tag{23}$$

where $\omega_1 = 2\pi f_1$ and $t \in (t_k, t_{k+1})$.

It is worth noting that the process can be speed up if the balanced operation of a three-phase converter is considered. In this case, only one power switch (composed by a Q and D) can be considered. In any case, for unbalanced power converter operation, the method remains still valid considering all legs of the power converter separately.

Finally, the temperature profile of the power devices is achieved by superimposing both average temperature ($\overline{\Theta}_J|_k(t)$) and the ripple temperature profile ($\widetilde{\Theta}_J|_k(t)$):

$$\Theta_J|_k(t) = \overline{\Theta}_J|_k(t) + \widetilde{\Theta}_J|_k(t), \qquad t \in (t_k, t_{k+1}) \tag{24}$$

4 | Numerical Simulations

Several numerical simulations have been carried out to validate the analytical loss models. In this sense, the proposed analytical model structure follows the flowchart diagram shown in Figure 6 being executed in Matlab environment, whereas the temporal simulations were carried out in Simulink in combination with the PLECS blockset simulation environment.

Please note that, several simulation platforms can be employed for this type of study, including Matlab/Simulink, Matlab/PLECS, PSpice, or Typhoon. Even custom implementations in interpreted languages (e.g. Python, Java) or compiled languages (e.g. C) could be considered.

Finally, both strategies were executed on the same computer, so the results could be fairly compared. Workstation specifications are summarized in Table 1. Indeed, execution time may vary depending on factors such as the programming language (e.g. Matlab vs. standard C), memory allocation, or matrix handling routines, but such implementation-specific aspects fall outside the intended scope of this contribution. It is important to note

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TABLE 1 | Workstation specifications used for the comparison.

Parameter	Value
CPU	AMD Ryzen 7 5800H 3.2 GHz
GPU	NVIDIA GeForce RTX 3080 Laptop GPU
Storage	SAMSUNG MZVLB1T0HBLR-000L2
Motherboard	Lenovo LNVNB161216
Memory	Kingston 32GB (2×16 GB) 2666MHz DDR4 CL15
Operating system	Windows 11 Pro

TABLE 2 | Operational conditions for thermal comparison and thermal description of IGBT and diode from Infineon datasheet.

Parameter	Value	Parameter	Value
DC bus voltage (v_{DC})	900 V	Power device	FZ400R12KE4
Switching freq. (f_{sw})	10 kHz	R_g	1.8 Ω
Fund. freq. (f_1)	50 Hz	R_{Qon}	1.8 mΩ
Amb. temp. (Θ_{amb})	40 °C	V_{Q0}	0.766 V
Output load ($\hat{Z}_o$)	1 Ω	R_{Don}	1.5 mΩ
		V_{D0}	0.796 V

that the proposed methodology is not intended to replace high-fidelity simulation tools like PLECS, but rather to serve as a complementary approach for scenarios where computational speed is the primary constraint.

The aim of the simulation evaluation is to compare the temperature profile obtained with the proposed method, with that obtained with the conventional approach based on numerical simulations, considering the same working points and ambient temperature [16, 17]. It is worth mentioning that PLECS blockset is taken as a reference for the simulations because of its wide adoption in industry an academia. The thermal analysis carried out has followed the procedure described in Section 3, and shown in Figure 6.

A three-phase 2L-VSI operated with THI-SPWM strategy and connected to a passive and balanced RL load is considered as the power converter to be evaluated. A sinusoidal phase current with constant fundamental frequency f_1 equal to 50 Hz is considered. The power module case is connected directly to a fixed ambient temperature source to maintain the same boundary conditions. The device under test is an Infineon 400 A, 1200 V IGBT power module because the PLECS thermal model is already available on the manufacturer's website, therefore avoiding the risk of bad device characterization. In addition, for a fair comparison, the same lookup tables used for the PLECS simulation have been used to build the analytical model of the devices. Table 2 summarizes the common input data used for all simulations.

The PLECS calculations in the thermal domain are carried out considering the lookup tables of the device forward characteristic

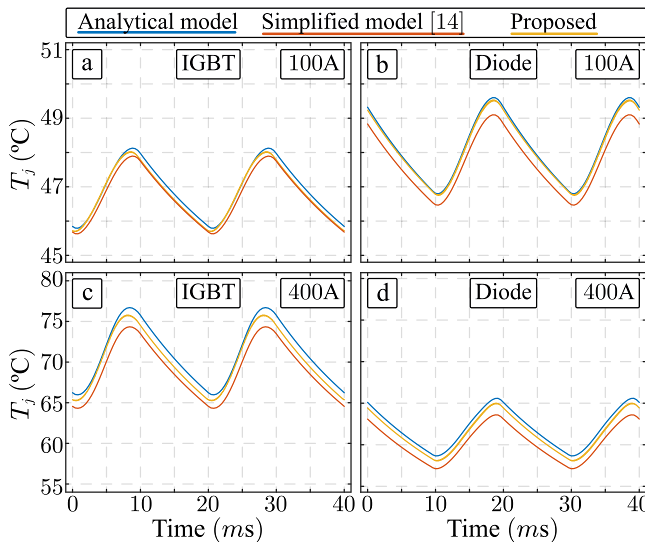

FIGURE 7 | Comparison of IGBT and diode junction temperature waveforms applying the THI-SPWM method @ $\cos(\varphi) = 0.9$.

(for the conduction power loss) and the switching energies (for the switching power loss).

On the other hand, the analytical model does not take into account the variation of the IGBT and diode parameters (on-resistances and no-load voltages) with respect to the phase current peak, but only the junction temperature. However, a modification of the conduction power loss was presented in Section 2, where the IGBT and diode forward characteristic are divided into sub-intervals and for each of them the on-resistance and the no-load voltage are calculated by considering the current in that interval.

In the following analysis, the numerical results will be compared to two different analytical models: the first one is the modified model, the second one is a simple model [16], where constant parameters are used. In Figure 7, the junction temperature waveforms of the IGBT and the diode for two different phase current peak values considering a power factor equal to 0.9 are shown. It can be observed that the proposed method fits closely with the waveforms provided by the PLECS simulation environment. In addition, there is also a noticeable difference between the simplified model [16] and the proposed method, which is in good agreement with the numerical model.

This study has been extended considering a wide current range. In Figure 8, the average and the (peak-to-peak) junction temperature ripple trend with respect to the phase current peak value with two different power factors are shown. As highlighted before, the difference between the proposed and the simplified model is important, especially when considering the diode junction temperature. On the other hand, the numerical and the proposed analytical models are in very good agreement, in particular when considering the junction temperature ripple. For better comprehension, the mean and maximum error of the achieved Tj and ΔTj for simple model [16] and the proposed method respect to the analytical model is reported in Table 3. As shown, the proposed method present a better performance.

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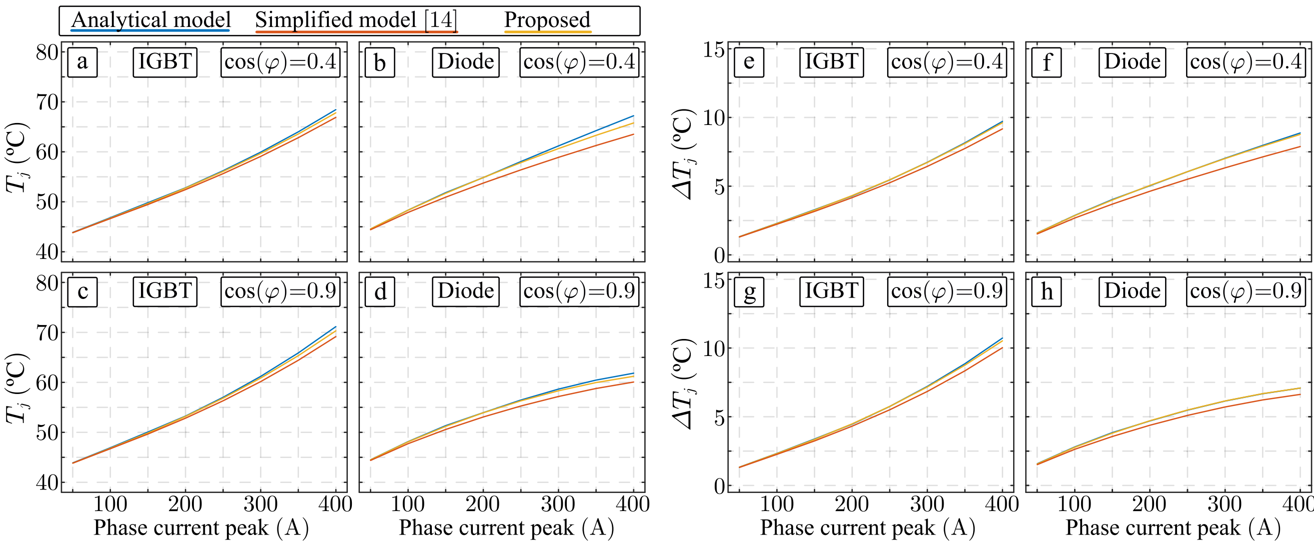

FIGURE 8 | Comparison of IGBT and diode junction temperatures. (a–d) average temperature. (e–h) Peak-to-peak temperature ripple.

TABLE 3 | Calculated error metrics for data obtained in Figure 8 comparing proposed method with the simplified method.

			Simplified		**Proposed**	
			$\cos(\varphi) = 0.4$	$\cos(\varphi) = 0.9$	$\cos(\varphi) = 0.4$	$\cos(\varphi) = 0.9$
IGBT	T_j	Mean (°C) [%]	0.67 [1.15%]	0.80 [1.35%]	0.26 [0.46%]	0.30 [0.51%]
		Max (°C) [%]	1.55 [2.27%]	1.98 [2.79%]	0.63 [0.92%]	0.84 [1.18%]
	ΔT_j	Mean (°C) [%]	0.25 [4.44%]	0.29 [4.86%]	0.05 [0.77%]	0.06 [1.31%]
		Max (°C) [%]	0.55 [6.08%]	0.69 [6.52%]	0.13 [1.89%]	0.19 [3.98%]
Diode	T_j	Mean (°C) [%]	0.67 [1.15%]	1.08 [1.93%]	0.26 [0.46%]	0.25 [0.45%]
		Max (°C) [%]	1.55 [2.27%]	1.77 [2.87%]	0.63 [0.92%]	0.61 [1.00%]
	ΔT_j	Mean (°C) [%]	0.25 [4.44%]	0.34 [7.23%]	0.05 [0.77%]	0.02 [0.82%]
		Max (°C) [%]	0.55 [6.08%]	0.46 [8.12%]	0.13 [1.89%]	0.07 [2.82%]

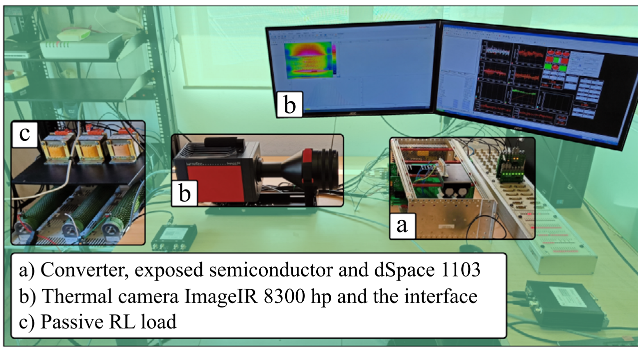

FIGURE 9 | Experimental setup.

TABLE 4 | Summary of the experimental rig.

Parameter	Value	Parameter	Value
DC bus voltage (v_{DC})	250 V	Power device	SK25GH12T4
Switching freq. (f_{sw})	10 kHz	Fund. freq. (f_1)	1 Hz
Load Resistor ($\hat{Z}_o$)	10 Ω	Load inductance	15 mH
Amb. temp. (Θ_{amb})	25 °	Thermal acquisition	200 Hz
		Sampling time (S_t)	5 ms

5 | Experimental Validation

To validate the previous results, a brief experimental test has been carried out in the down scaled laboratory prototype shown in Figure 9. This experimental rig is composed by a two-level IGBT-based inverter feeding a balanced RL load. IGBT and diode devices are the SK25GH12T4 [20] model from the Semikron manufacturer. The system is operated in closed-loop form following the conventional synchronous dq-frame with a PWM modulation with sinusoidal carrier by using a DSP1103 control platform from dSPACE. The rest of passive elements and operating parameters are summarized in Table 4.

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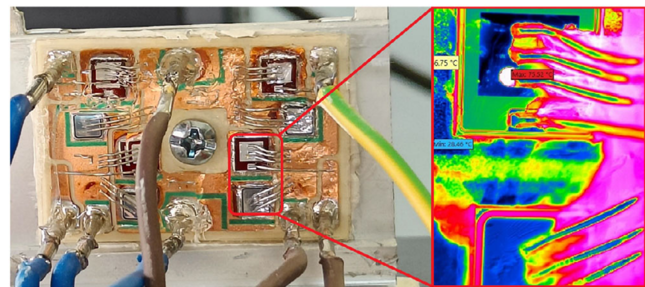

FIGURE 10 | Exposed Semikron power device for thermal measurement.

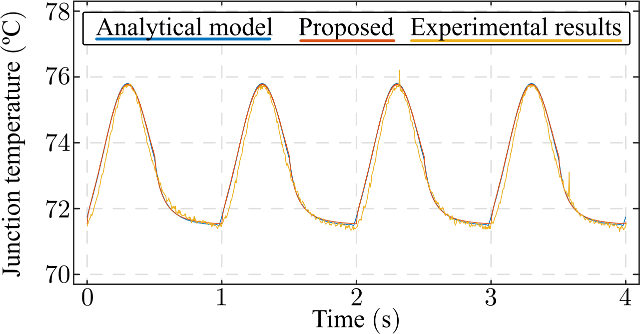

FIGURE 11 | Comparison between simulation data, proposed modelling and thermal acquisition in the experimental rig.

For temperature acquisition, a high performance infrared ImageIR 8300-hp camera and the WD300 microscope lens have been used from Infratec manufacturer, which has an accuracy of 1 C. For measuring purposes, one power module has been opened and its protector gel has been carefully removed, except for a thin layer which ensures a uniform emissivity for increased accuracy. A zoom image of the module is shown in Figure 10. It is important to note that a small heatsink has been chosen to facilitate the thermal ripple acquisition. The experiments were carried out in a room with controlled ambient temperature (25 °). Measurements have been captured after reaching a thermal steady state operation.

In Figure 11, a comparative image of the thermal acquisition between the simulation environment (in blue), the proposed technique (in red) and the experimental result (in yellow) is shown. It can be observed that the experimental thermal measurement of the IGBT junction temperature closely fits with the results obtained by the conventional and the proposed model (with de same semiconductor and diode). It has to be noticed that a small thermal deviation on the dynamics on rise and fall slopes is presented, but it is important to highlight that the average value as well as the peak-to-peak junction temperature values are consistent. In fact, the predicted T_j temperature presents a mean error of 0.17 °C which represents a 0.28% with a maximum error of 0.72 °C representing a 1.01% demonstrating the effectiveness of the proposal.

6 | Conclusions

This study introduces an advanced methodology for accurately estimating the junction temperatures of IGBTs and diodes, achieving superior precision compared to conventional strategies. The proposed approach is validated through a combination of simulations and experimental testing on a two-level IGBT-based voltage source inverter. The empirical results demonstrate that the temperature estimation of individual semiconductor devices within the converter can be achieved with high resolution and robustness.

A key technical advantage of the proposed methodology, confirmed by the obtained results, lies in its integration of averaged modelling techniques with detailed characterization of operating points and the dynamic behaviour of semiconductor's datasheet-based characteristic curves. This hybrid approach, which combines analytical modelling and post-processing for temperature estimation under nominal operating conditions at the fundamental frequency, significantly enhances the scalability and applicability of the methodology. It can be extended to a wide spectrum of semiconductor technologies and more complex converter topologies with increased device counts. Furthermore, the ability to perform accurate temperature estimations enables the implementation of RUL analysis techniques, facilitating predictive maintenance strategies that optimize operational reliability and reduce overall lifecycle costs.

Author Contributions

Ciro Alosa: conceptualization, investigation, methodology, writing – original draft, writing – review & editing. **Abraham Marquez Alcaide:** conceptualization, formal analysis, project administration, supervision, writing – original draft, writing – review and Editing. **Alejandro Stowhas-Villa:** conceptualization, methodology, writing – original draft, writing – review & editing. **Jhonattan Berger**: conceptualization, methodology, writing – review & editing. **Fabio Immovilli**: conceptualization, investigation, supervision, writing – review & editing. **Christian A. Rojas**: conceptualization, investigation, writing – original draft, writing – review & editing **Ricardo Lizana F**: conceptualization, methodology, supervision, writing – original draft, writing – review & editing. **Giampaolo Buticchi**: funding acquisition, methodology, writing – original draft, writing – review & editing. **Samir Kouro**: conceptualization, project administration, supervision, writing – original draft, writing – review & editing. **Jose Leon**: conceptualization, funding acquisition, project administration, supervision, writing – original draft, writing – review & editing.

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Conflicts of Interest

The authors declare no conflicts of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author, upon reasonable request.

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