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Assessment of dual-oxide options for LDMOS transistors in FinFET technology☆

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ABSTRACT

We present a comparison of three LDMOS transistor designs in ≃16 nm FinFET technology with different gate stack configurations: thick ITL oxide, thin ITL oxide, and a combination of both (dual ITL oxide thickness). We analyze by simulation how the gate oxide stack influences the main performance and time-zero degradation rate indicators.

The simulations suggest that, for the same doping profile and gate length (L_G), the dual-oxide configuration has transition frequency (f_T) and on-resistance ($R_{DS,on}$) within ≈16% and 6% of those of thick and thin-oxide devices, respectively, while the maximum substrate and gate currents are ≈35% and 43% smaller than for a fully thin-oxide device, respectively. Consequently, the dual-oxide configuration enables L_G scaling and improvements in f_T and $R_{DS,on}$ while keeping degradation monitors under control.

1. Introduction

The laterally double-diffused MOS (LDMOS) is the transistor of choice for high-power applications, power management integrated circuits (ICs), automotive and radio-frequency (RF) communication systems [1,2]. It can handle high electric fields owing to the drift region, a resistive extension where the voltage drop between the drain and the channel is uniformly distributed. The planar LDMOS is a key component of RF power amplifiers (PA), DC-DC converters, and power switches.

FinFETs are the technology of choice for low-power digital applications. Compared to planar realizations, FinFETs demonstrate lower RF performance due to larger gate–source and gate-drain capacitances [3]. Furthermore, reliability is limited at the shortest FinFET nodes, because high voltages dramatically increase hot carrier injection (HCI) [4], thus jeopardizing the device lifetime. Thus, the realization of LDMOS FinFETs at N16 appears a sensible choice to balance good RF performance with adequate reliability in the next generation of RF mixed-signal designs for Systems-on-Chip (SoCs) [5,6]. However, as of today, the FinFET LDMOS is addressed in very few studies [4,7,8].

The FET RF and switching performance is typically evaluated by the cut-off frequency (f_T) and the on-resistance ($R_{DS,on}$) metrics. It is well known that these figures improve when scaling gate length (L_G) and the equivalent oxide thickness (EOT) [9]. However, when shortening the L_G, HCI deteriorates, as monitored by the substrate and gate tunneling currents (I_B and I_G, respectively), thus jeopardizing the device reliability [10].

A dual-oxide configuration where the thin SiO_2 inter-layer is thickened above the drift region could embody an effective compromise [11]. Thinning the oxide above the p-channel enables gate length scaling, while thickening the one above the drift region mitigates the gate tunneling leakage and the maximum electric field; hence, the breakdown voltage [9,11].

In this context, we present a simulation study comparing three performance metrics, f_T, $R_{DS,on}$, and breakdown voltage, V_{BD}, and two degradation metrics, I_B and I_G of LDMOS FinFETs. We analyze three gate stack configurations having different SiO_2 ITL thickness, hereafter denoted thick-oxide (TO), thin-oxide (tO), and dual-oxide (DO) for L_G = 500 nm, L_{eff}≈150 nm devices. Then, we consider scaled DO devices down to L_G = 250 nm, L_{eff}≈21 nm.

The paper is organized as follows: Section 2 describes the simulated device architecture, the simulation setup, and the model calibration. Section 3 shows the simulation results of the three configurations at L_G = 500 nm, while Section 4 discusses the scaling perspectives of DO LDMOS FinFETs. Finally, Section 5 draws the conclusions.

2. Device architecture and simulation setup

We simulated a FinFET LDMOS device with 2 fins/1 finger and L_G = 500 nm, targeting V_{DD} = 3.3 V. Fig. 1 presents the TCAD structure

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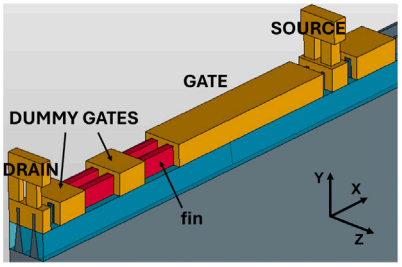

Fig. 1. Schematic view of the simulation domain.

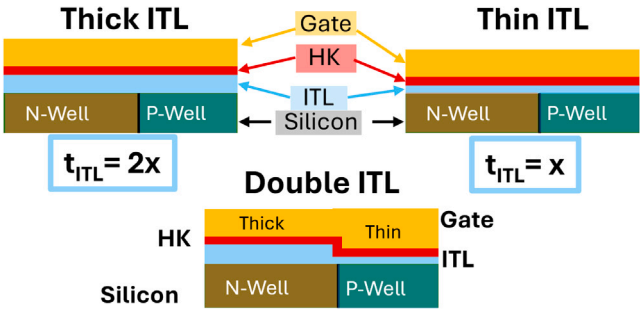

Fig. 2. Schematic view of the gate stack in the region above the p-well/n-well junction of the LDMOS in this work. The change in oxide thickness occurs above the p-channel/n-drift region junction. No significant change in the lateral component of the electric field is visible in simulations.

where we see two dummy (i.e., electrically floating) gates above the drift region. These dummies, imposed by the lithography rules, are useful to move the current flux away from the surface where the electric field is high, thus reducing the impact ionization generation rate.

The simulation domain contains two fins. Reflective boundary conditions at a distance of half fin-pitch from the center of the two fins allow us to replicate the behavior of large transistors composed of the repetition of multiple fins, fingers, and channels in a large array. We adopt an isothermal drift–diffusion transport model, neglecting electrothermal coupling, which results in a worst-case scenario slight overestimation of the hot carrier currents.

Firstly, we consider an L_G = 500 nm device and three different configurations of the interfacial SiO_2 oxide (ITL): thick-oxide (TO), thin-oxide (tO), and dual-oxide (DO), as shown in Fig. 2. The ITL of the TO sample is about twice as thick as in the tO one. Both ITLs have uniform thickness (thick or thin) under the dummy gates and the main gate. The DO sample, instead, has a thick ITL above the drift region and a thin ITL above the channel. The high-κ oxide thickness is uniform and the same in all structures. This solution appears more fabrication-friendly than changing the high-κ layer thickness for the same target EOTs because the regrowth of SiO_2 layers is a well-developed and highly reliable process, while the regrowth of a thicker high-κ layer can significantly degrade the high-κ to ITL interface quality. The ITL thickness impacts the C_{ox}, which in turn affects the c_{gg}, the g_m, and consequently the f_T and the $R_{DS,on}$ but also affects the degradation rate indicators I_B and I_G.

The model of the TO device has been calibrated on DC and AC measurements of LDMOS FinFETs fabricated in the same ≃16 nm digital technology of [12]. Lacking reliable process simulations, the calibration started with the fin/finger dimensions (i.e., W_{fin} = 8 nm, H_{fin}≃40 nm) and the dopings in [12]. Then we added the series resistances and the drift region doping in the area delimited by the dedicated mask. By fine-tuning the drift-region vertical and lateral doping, and by adjusting the mobility and velocity parameters (due to unknown quantum confinement and strain levels), we achieved good agreement with measurements.

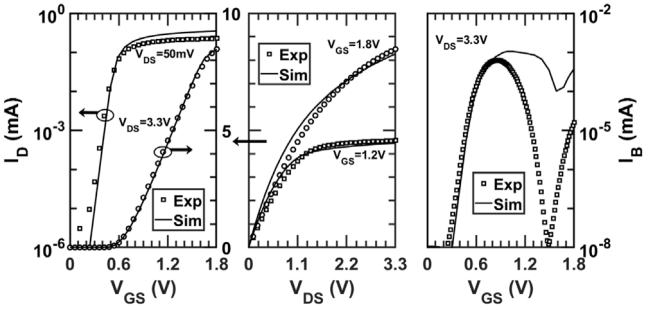

Fig. 3. DC calibration of the TCAD model on ≈16 nm LDMOS FinFET data. TO device. L_G=500 nm. The overestimated I_B at large V_{GS} is likely due to carrier confinement in the fin and residual inaccuracy of the local impact ionization model at low electric field.

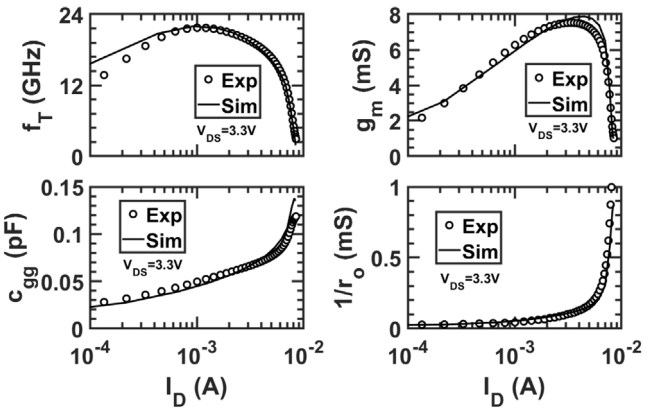

Fig. 4. AC calibration of the TCAD model on LDMOS FinFET experimental data. TO device. L_G = 500 nm, f = 10 GHz.

Fig. 3 shows that the TCAD model well represents the experimental DC curves. The electron ionization rate (α_n) of the TCAD local model for impact ionization [13] has been slightly adjusted to match the measured I_B peak at low V_{GS}. The I_B at large V_{GS} departs from the experiments, likely due to non-local dark space, hot carrier effects and carrier confinement in the fin. AC analyses (Fig. 4), conducted at the same extraction frequency f = 10 GHz used in measurements, also led to a good agreement with experiments.

3. Simulation results

The successful design of LDMOS FinFETs for the next generation of RF mixed-signal SoCs targets significant RF performance improvements without worsening the reliability. This TCAD study addresses the three LDMOS designs introduced in Section 2 to understand how the gate stack impacts their performance and degradation rate indicators.

Figs. 5, 6 compare the $R_{DS,on}$ and f_T among the three device configurations at L_G = 500 nm. The tO and DO samples show similar $R_{DS,on}$ and f_T at every V_{GS} and I_D, respectively, proving that these two designs behave comparably in the active channel. The TO LDMOS has thick-oxide everywhere, thus the C_{ox} is the lowest. The other configurations have a lower $R_{DS,on}$, but also smaller f_T than the TO case as reported in Table 1. Simulations show that in the V_{GS} range of maximum f_T accumulation of the gate/drift overlap region affects g_m and c_{GG}. Compared to the DO device, the tO one has a bit larger g_m and the same c_{GG}, while the TO one has lower g_m but even lower c_{GG}, thus yielding slightly better f_T than the DO LDMOS.

Considering now the degradation rate indicators, we see in Fig. 8 that the I_B vs V_{GS} curves have a secondary hump at V_{GS} close to 1.8 V

Table 1
Comparison of the main performance and degradation metrics of thick (TO), thin (tO), dual (DO), and scaled dual-oxide devices. The percentage variations are computed w.r.t. the tO configuration.

	Thick	Thin (ref)	Dual	Dual350	Dual250	var. Dual	var. Dual350	var. Dual250
$R_{DS,on,V_{GS}=1.8V}$ (mΩ mm^2)	1.80	1.66	1.70	1.47	1.32	+2.41%	−11.4%	−20.5%
$f_{T,max}$ (GHz)	22.0	19.6	18.5	28.3	38.4	−5.61%	+44.4%	+95.9%
$I_{B,V_{GS}\ first-peak}$ (μA)	0.967	1.68	1.11	2.62	2.98	−34.9%	+55.9%	+77.4%
$I_{B,V_{GS}=1.8V}$ (μA)	0.324	1.46	0.734	0.788	0.614	−49.7%	−46.0%	−57.9%
$I_{G,V_{GS}=1.8V}$ (pA)	$< 10^{-3}$	29.1	16.5	9.62	3.75	−43.3%	−66.9%	−87.1%
V_{BD} (V) @V_{GS} = 1.8 V	11	7.1	7.9	7.6	7.7	+11.3%	+7.04%	+8.45%
L_G (nm)	500	500	500	350	250	/	/	/

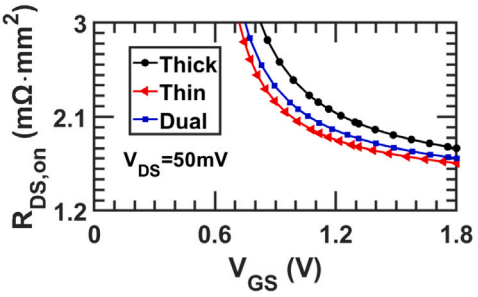

Fig. 5. Simulated $R_{DS,on}$ of thick-oxide, thin-oxide and dual-oxide configurations. All the devices feature L_G = 500 nm.

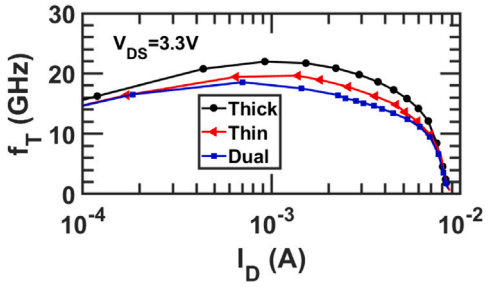

Fig. 6. Simulated f_T of thick-oxide, thin-oxide and dual-oxide configurations. All the devices feature L_G = 500 nm.

in all configurations. This is due to the shift of the peak electric field toward the region next to the drain at high V_{GS}. The uniform tO device has the largest I_B at both peaks because of the stronger inversion of the surface, indicating strong hot-carrier effects and poor reliability. The DO one, instead, shows an I_B comparable to that of the TO LDMOS, suggesting that the TO and the DO devices behave similarly almost most of the drift region where the bulk current is mainly generated.

Fig. 7 shows the electron ionization coefficient (α_n), the electron current density (J_n), and the impact ionization generation rate ($G_{II} = \alpha_n|J_n|/q$), for all configurations at the bias of peak I_B (V_{DS} = 3.3 V; V_{GS} = 0.9 V). The cut along the *x* direction intersects the region of maximum G_{II}, located slightly below the end of the gated part of the fin. The TO device exhibits the highest α_n but also the lowest J_n, resulting in a low G_{II} value. The tO configuration has a higher J_n than the TO one, and even if α_n is smaller, G_{II} is larger by ≈ 2×.

The DO configuration, instead, combines a high J_n with an α_n value smaller than for the TO device, resulting in a G_{II} peak comparable to the TO device. This is reflected in the I_B curves of Fig. 8. Therefore, the dual-oxide configuration achieves similar I_D as the tO structure but with a lower I_B.

Finally, the breakdown voltage of the 500 nm DO device at V_{GS} = 1.8 V, Table 1), is between those of the tO and TO LDMOS, but anyway more than 2× larger than V_{DD} = 3.3 V.

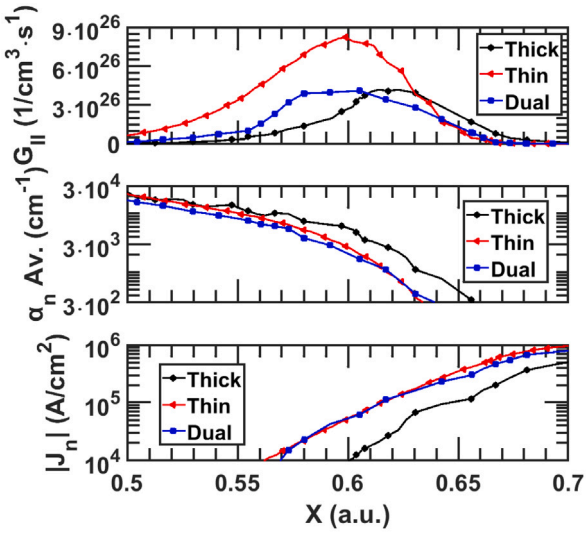

Fig. 7. Generation rate (G_{II}), electron alpha avalanche (α_n) and electron current density (J_n) along the drift region at the y-depth where the maximum G_{II} is located (L_G = 500 nm; V_{DS} = 3.3 V; V_{GS} = 0.9 V). X = 0 is located at the drain edge of simulation domain.

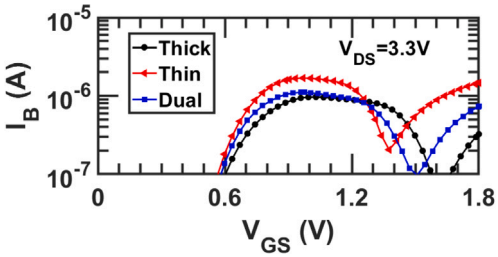

Fig. 8. Simulated I_B of thick-oxide, thin-oxide, and dual-oxide configurations. All the devices feature L_G = 500 nm.

4. Dual-oxide LDMOS FinFET scaling

The scaling in LDMOS FinFET is constrained by L_G and gate oxide thickness. The tO structure could scale well, but has significantly higher I_B than the other configurations. Since I_B of the DO device is not so deteriorated, it offers larger margins for L_G reduction. In the following, the DO LDMOS scaling has been investigated keeping the profile of each dopant and the physical model parameters the same while decreasing L_G down to 250 nm (L_{eff}≃21 nm). Due to lateral overlap, the net doping is slightly reduced below the gate and at the start of the drift region.

Fig. 9 shows the performance metrics of the scaled DO devices compared to the L_G = 500 nm DO one. The shortest LDMOS (Dual250) has the lowest $R_{DS,on}$ and the highest f_T, as expected, thus improving the RF performance and the power efficiency of the circuits. This improvement comes at the price of a higher I_B peak at $V_{GS} \approx V_{DS}/2$

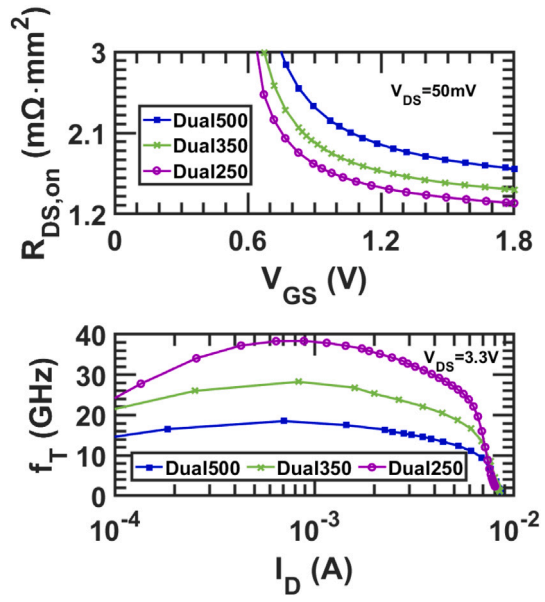

Fig. 9. Comparison of the $R_{DS,on}$ and f_T for three DO devices with scaled L_G = 500, 350, and 250 nm.

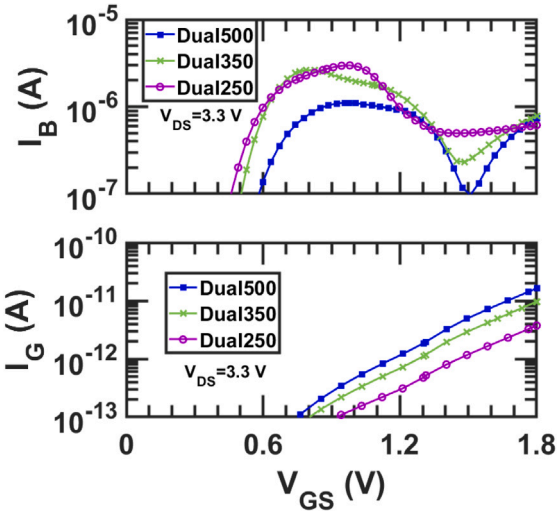

Fig. 10. Same as Fig. 9 for the I_B (top) and I_G (bottom) for three DO devices.

compared to the longer DO structure, but similar to that of the Dual350 LDMOS (Fig. 10 and Table 1). The I_B value at high V_{GS}, instead, is similar for all the DO transistors. The promising scaling of DO devices is also evident in the gate tunneling current plots (Fig. 10), where I_G decreases as the L_G is reduced, mainly due to the smaller tunneling area. At last, notice that the Dual350 and Dual250 LDMOS feature similar V_{BD}, which is comparable to that of the 500 nm DO device, thus better than for the tO LDMOS (Table 1).

These results suggest that by scaling DO LDMOS finFET down to L_G = 250 nm while keeping the same doping profiles, we can achieve better performance metrics than its long-channel counterpart, while offering the same or better time-zero degradation rate indicators. We explicitly verified that further scaling to $L_G \simeq 150$ nm, instead, requires a smoothening of the drift region and junction doping to prevent high fields and maintain a good balance between performance and hot carrier effects.

5. Conclusions

TCAD simulations point out how, at constant gate length and doping profiles, dual-oxide LDMOS FinFET compliant with ≃16 nm FinFET layout rules can achieve $R_{DS,on}$ and f_T values comparable to those of thin ITL devices but with lower I_B and I_G. Furthermore, when reducing the L_G, the $R_{DS,on}$, f_T, and the I_G of dual-oxide LDMOS remarkably improve, at the only cost of a limited increase in I_B at low V_{GS}. The latter can be alleviated by optimizing the doping profiles, the position of the thin/thick oxide transition, and the drain junction doping.

These qualitative trends suggest, within the limits of a calibrated but local impact ionization model, the possibility of shortening L_G in a dual-oxide LDMOS, thus improving the key performance metrics with limited deterioration of time-zero degradation rate indicators and, likely, of the device lifetime. This choice is relevant for the design of the next generation RF mixed-signal for System-on-Chip, since it yields better performance in a smaller device footprint while keeping hot carrier degradation under control.

CRediT authorship contribution statement

Alessandro Ruggieri: Writing – original draft, Methodology, Investigation, Formal analysis, Data curation, Conceptualization. **Lisa Tondelli:** Writing – review & editing, Visualization. **Luca Selmi:** Writing – review & editing, Supervision.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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Data availability

The authors do not have permission to share data.

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