electronic materials

Article

Impact of SiN Passivation on Dynamic-R_{ON} Degradation of 100 V p-GaN Gate AlGaN/GaN HEMTs

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Abstract

In this paper, the impact of SiN passivation on dynamic-R_{ON} degradation of AlGaN/GaN HEMTs devices is put in evidence. To this end, samples showing different SiN passivation stoichiometry are considered, labeled as Sample A and Sample B. For dynamic-R_{ON} tests, two different experimental setups are employed to investigate the R_{ON}-drift showing up during conventional switch mode operation by driving the DUTs under both (i) resistive load and (ii) soft-switching trajectory. This allows to discern the impact of hot carriers and off-state drain voltage stress on the R_{ON} parameter drift. Measurements performed with both switching loci shows similar dynamic-R_{ON} response, indicating that hot carriers are not involved in the degradation of tested devices. Nevertheless, a significant difference was observed between Sample A and Sample B, with the former showing an additional R_{ON}-degradation mechanism, not present on the latter. This additional drift is totally ascribed to the SiN passivation layer and is confirmed by the different leakage current measured across the two SiN types. The mechanism is explained by the injection of negative charges from the Source Field-Plate towards the AlGaN surface that are captured by surface/dielectric states and partially depletes the 2DEG underneath.

Keywords: gallium nitride; HEMTs; p-GaN; dynamic-R_{ON}; SiN; passivation

Academic Editor: Wojciech Pisula

Received: 27 May 2025
Revised: 8 September 2025
Accepted: 3 October 2025
Published: 7 October 2025

Citation: Cioni, M.; Cappellini, G.; Giorgino, G.; Chini, A.; Parisi, A.; Miccoli, C.; Castagna, M.E.; Constant, A.; Iucolano, F. Impact of SiN Passivation on Dynamic-R_{ON} Degradation of 100 V p-GaN Gate AlGaN/GaN HEMTs. *Electron. Mater.* **2025**, *6*, 14. https://doi.org/10.3390/electronicmat6040014

1. Introduction

AlGaN/GaN High Electron Mobility Transistors (HEMTs) represent one of the best options to replace Silicon devices in power-switching applications due to their high frequency and high-power capabilities [1,2]. However, dynamic ON-resistance (R_{ON}) degradation [3,4] still limit their performances well below expectations, making it difficult to reach the promised efficiencies in switching converters [5]. This dynamic-R_{ON} could be induced by several factors. As a relevant example, dopants introduced in the GaN buffer to increase the blocking voltage [6] could introduce trap states in the buffer that could be ionized when relatively large drain voltage (V_{DS}) is applied in off-state [7]. This could expose negative charges that partially depletes the 2-Dimensional Electron Gas (2-DEG), thus increasing the R_{ON} when the device is set back to on-state. However, buffer traps are not the only possible contributions to dynamic-R_{ON}, since surface states and/or traps in

the dielectrics could play a similar role in increasing the on-state resistance. Particularly, surface traps [8] may be ionized by large off-state drain voltage and by hot-carrier effects. Concerning the latter, these effects can be triggered by ON/FF and OFF/ON transitions performed at non-zero current and for this reason can come into play under inductive load or resistive load switching trajectory. However, surface states can be ionized also in absence of hot carrier effects, since relatively high drain voltages applied in off state can ionize traps at the passivation/AlGaN interface [9,10] and/or favor the injection of electrons from the source field-plate towards the AlGaN surface [11]. In both cases, the accumulation of negative charges in the gate-drain access region would cause the partial depletion of the 2DEG and thus induce an increase in the R_{ON} of the device.

In this scenario, the SiN dielectric used as passivation for 100 V AlGaN/GaN HEMTs can play a critical role for trapping effect taking place at the device surface. This can be due to two main reasons: (i) the SiN chemistry can change the configuration of states at the AlGaN surface where the dielectric is deposited, in turn changing the amount of trap states that can be ionized/filled; (ii) a different SiN composition can yield different insulating properties of the material, thus changing the amount of negative charges that can be injected from the field-plate and being trapped at the surface. Accordingly, goal of this work is to study the impact of the SiN passivation layer on the dynamic-R_{ON} degradation of GaN-based HEMTs with the aim to optimize the device processing and prevent large R_{ON} drifts.

To this end, two different samples (namely Sample A and Sample B) are compared in this work, presenting as only difference between them the stoichiometry of the SiN passivation dielectric. The idea is rather simple: by comparing the dynamic-R_{ON} behavior between the two samples, we can put in evidence the role of the SiN passivation and, by studying the underlying physics, we can provide feedback to the manufacturing process to optimize the fabrication steps.

In order to understand the underlying physics, the simple comparison between the two different samples is not sufficient. In fact, we need to understand if the root cause for the behavior is associated to hot carriers or to pure off-state drain bias. To do so, we compare the dynamic-R_{ON} results obtained under both restive load trajectory [12,13] and soft-switching trajectory [14–17]. The former characterization is performed by means of a custom measurement setup which allows to obtain an outstanding time resolution to accurately measure the dynamic evolution of the R_{ON} parameter and gain more physics insight on the trapping effects involved. On the other hand, soft-switching tests are performed with a commercial system AM3200 by AMCAD (Rockleigh, NJ, USA) which presents a reduced time resolution but allows to properly define the dead times required to switch ON/OFF the device at zero-current.

After the acquisition of the dynamic-R_{ON} results, the properties of the two different SiN dielectrics are compared in terms of leakage current on simplified test structures. This aims to better understand the physical mechanism governing the R_{ON} drift but also to provide a possible diagnostic tool to sense the SiN quality prior to perform a complete dynamic-R_{ON} characterization.

The paper is organized as follows. Section 2 reports a description of Devices Under Test (DUTs), while Section 3 shows the custom measurement setup used to study the dynamic-R_{ON} degradation under restive load switching conditions. Then, Section 4 shows the results obtained for both Sample A and Sample B, investigating the impact of temperature on the dynamic-R_{ON} behavior. The results are then compared to the soft-switching characterization reported in Section 5, highlighting the impact of the off-state drain voltage on the parameter drift. All the tests have been performed with grounded substrate configuration. To better understand the underlying physics, the leakage across the different SiN

dielectric of Sample A and B is characterized in Section 6, yielding to a potential model that explains the experimental behavior. Finally, conclusions are drawn in Section 7.

2. Device Description

DUTs were 100 V AlGaN/GaN HEMTs grown on Silicon substrate. Normally off operation was obtained by means of a p-GaN gate structure [18], while the GaN buffer was Carbon (C) doped to obtain a semi-insulating layer [19], with a whole thickness of about 2 µm. The Gan channel thickness ranged between 300 nm and 700 nm. The gate width (W_G) was 0.4 mm, while the gate length (L_G) was <1 µm. The gate-source (L_{GS}) and gate-drain (L_{GD}) distance were <1 µm and <2 µm, respectively (see Figure 1). After the epitaxial growth and the p-GaN etching step, two different passivation were considered. Particularly, the material used as passivation was Silicon Nitrice (SiN) and the only difference between the two SiN types was the stoichiometry between Silicon and Nitrogen precursors, yielding to the Sample A and Sample B considered for the study. After the passivation deposition and the contacts opening, the Source Field-Plate was defined through a metal deposition step, providing the device geometry shown in Figure 1a. Figure 1b,c reports the I_D-V_{GS} and I_D-V_{DS} curves of Sample A and Sample B.

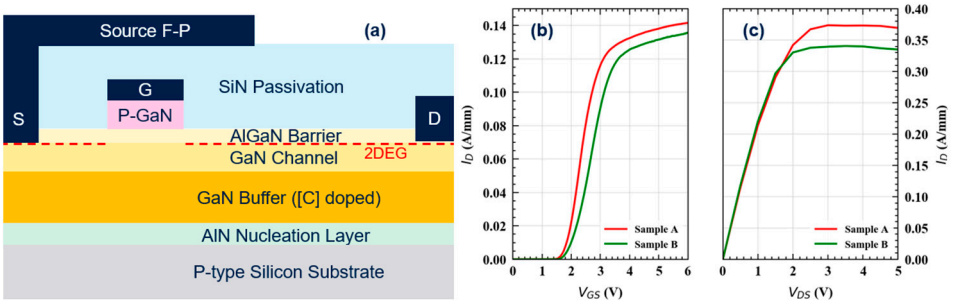

Figure 1. (**a**) Schematic Cross-Section of the Device Under Test (DUT). (**b**) I_D-V_{GS} curves of sample A and B acquired at V_{DS} = 0.5 V. (**c**) I_D-V_{DS} curves of sample A and B acquired at V_{GS} = 6 V.

3. Dynamic-R_{ON} Characterization Method

In order to characterize the dynamic-R_{ON} degradation of the DUTs, the custom measurement setup schematically depicted in Figure 2 was adopted.

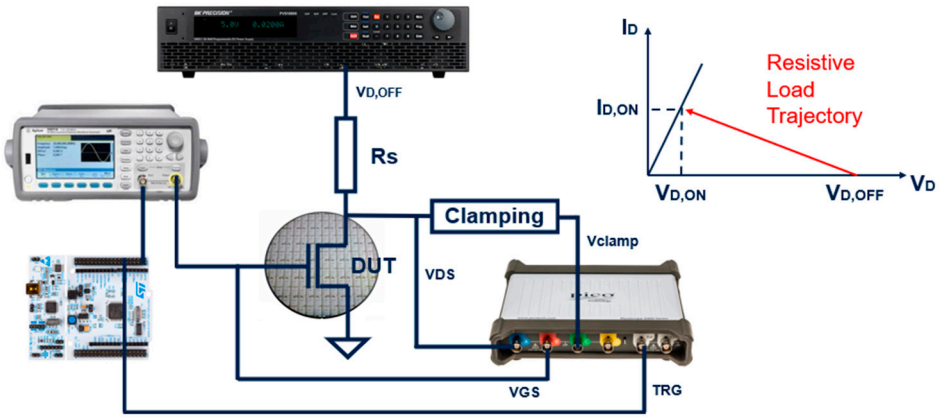

Figure 2. Simplified schematic of the custom experimental setup used for the characterization of the DUT under resistive load conditions and related switching trajectory experienced by the DUT during the ON/OFF, OFF/ON commutations.

The experimental setup consists of several instruments, whose operation is synchronized by means of a LabVIEW VI.

The device is continuously switched ON and OFF by means of a waveform generator providing a pulsed V_{GS} signal ranging between $V_{G,OFF}$ = 0 V and $V_{G,ON}$ = 6 V.

The drain of the DUT is connected to a high-voltage power supply by means of a series resistance (R_S) whose value is set in order to fix the $I_{D,ON}$ current level flowing through the DUT at 20 mA/mm. This ensures that ON/OFF and OFF/ON transitions are performed under resistive load trajectory as depicted in Figure 2. This allows us to have a non-zero current level during the whole switching phase and to set the current level in linear region. Accordingly, to extract the R_{ON} value in on-state, it is sufficient to measure the on-state voltage level ($V_{D,ON}$) and compute R_{ON} as $V_{D,ON}/I_{D,ON}$. To this end, an additional clamping circuit, similar to the one described in [20], is used to limit the voltage read by the Digital Sampling Oscilloscope (DSO), thus allowing to reduce the scale of the DSO channel to few Volts and optimize the resolution to measure $V_{D,ON}$.

The DSO operates in block mode configuration, with the aim to exploit its segmented memory and optimize the time resolution of the system. This is very important in order to acquire data for short time interval of stress. Nevertheless, dynamic-R_{ON} drift can arise also after long stress time and a linear sampling distribution would be ineffective for capturing both short and long-time behavior of the DUT. For this reason, the DSO acquisition is triggered by means of a Micro Controller Unit (MCU) that generates the trigger (TRG) signal only for some predefined periods, making it possible to logarithmically distribute the samples over time. This allows to acquire data for long stress time with a good time resolution, but without saturating the DSO segmented memory [21].

An example of the typical waveforms experienced during the characterization is reported in Figure 3.

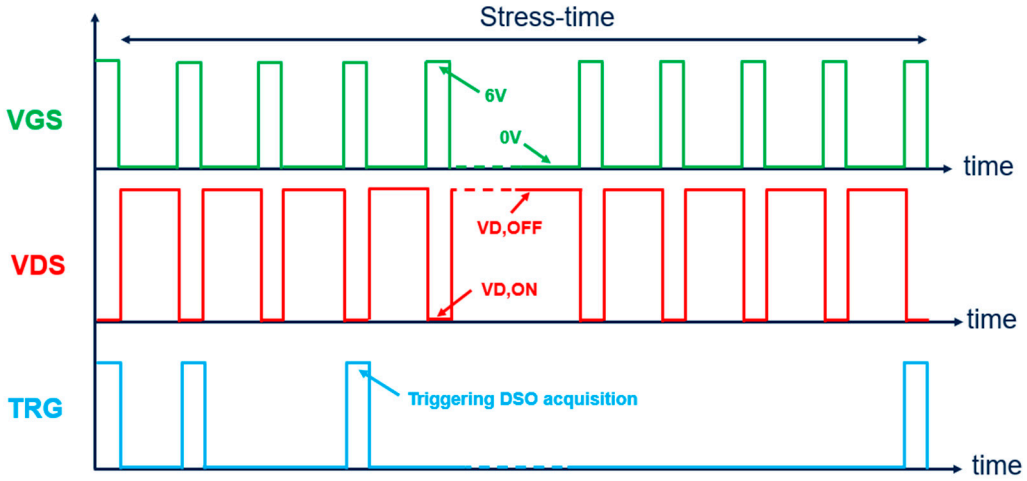

Figure 3. Typical waveforms experienced during the on-the-fly characterization with the custom experimental setup. The V_{GS} signal is pulsed with 2 µs T_{ON} and 10 µs period between 6 V $V_{G,ON}$ and 0 V $V_{G,OFF}$; accordingly, the V_{DS} changes between low $V_{D,ON}$ (<0.5 V to bring the DUT in its linear region) and relatively high $V_{D,OFF}$. The TRG signal is generated only for some predefined periods in order to logarithmically distribute the acquisitions over time.

As we can see by looking at Figure 3, the DUTs are continuously switched ON and OFF at every cycle with a 10 µs switching period and a 2 µs T_{ON}, but the TRG signal is generated only for some predefined periods, thus allowing the previously mentioned acquisition distribution over time. This allows to test the DUTs in a realistic operation conditions in which the switching period is not affected by the measurement and the R_{ON} extraction can be performed with a true on-the-fly characterization over 10 ks of cumulative stress time.

The experimental results obtained with the stress/measurement sequence just described are shown in the following Section.

4. Experimental Results

In this Section, Sample A and Sample B devices are tested by means for the characterization method described in Section 3. Particularly, the $V_{D,OFF}$ stress voltage applied was set to 50 V which is the typical drain bias employed for this kind of GaN Samples. Prior to the actual stress phase, the fresh R_{ON} parameter of the DUTs was extracted while biasing the device in on-state for few microseconds in order to set a reference value (R_{ON0}) for this parameter with respect to which the relative parameter drift can be computed. The dynamic-R_{ON} transients obtained for Sample A and sample B at 100 °C are reported in Figure 4.

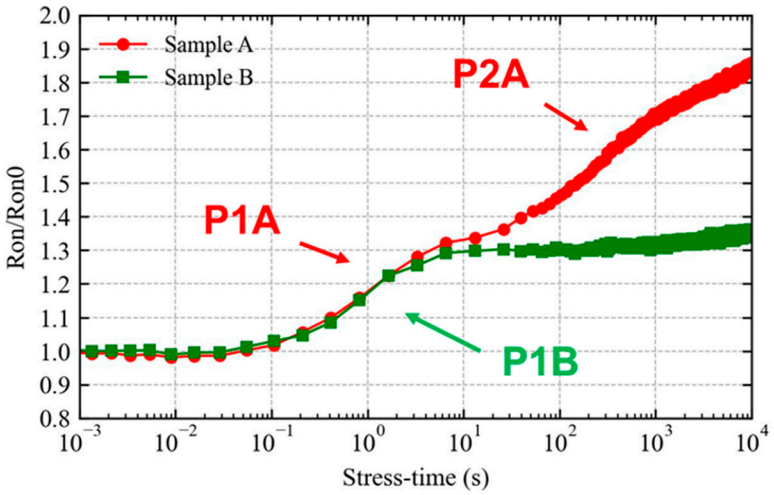

Figure 4. Dynamic-R_{ON} (R_{ON}/R_{ON0}) transients acquired at 100 °C with $V_{D,OFF}$ = 50 V on Sample A and Sample B.

The experimental results shown in Figure 4 already put in evidence a clear difference between the dynamic-R_{ON} behavior of Sample A and Sample B. In fact, even if the dynamic-R_{ON} transients are quite overlapped up to 2 s of cumulative stress time, Sample B shows a good saturating trend for longer stress times (reaching a 30%/35% of steady state drift) while Sample A features an additional transient increase in R_{ON} for this time range.

This behavior can be interpreted as follows. Both samples feature a similar R_{ON}-degradation mechanism for shorter times (hereby called process P1) that reaches its steady state before 10 s of cumulative stress time at 100 °C. For this reason, processes marked as P1A and P1B yield almost overlapped R_{ON} transients in this time range. On the other hand, Sample B shows an additional degradation process (named as P2A) that shows up for longer stress times and that is not observed on Sample B for the same considered time window. This put in evidence the presence of two distinct degradation processes that can be better discerned by looking at the trap signature in the two dynamic-R_{ON} transients. To this end, the experimental transients were fitted by means of stretched multiexponential functions [22–26] in order to extract the corresponding derivative $d(R_{ON}/R_{ON0})/dlogt$ reported in Figure 5.

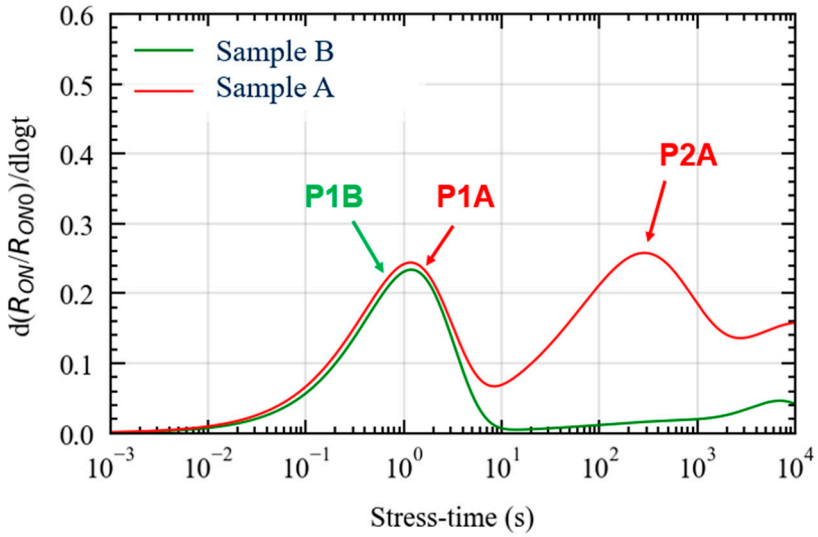

Figure 5. Derivatives $d(R_{ON}/R_{ON0})/dlogt$ plots acquired at 100 °C with $V_{D,OFF}$ = 50 V on Sample A and Sample B.

This plot is particularly useful for the trap state characterization, since the number of peaks in the derivative signal is equal to the number of trapping phenomena involved in the R_{ON}-drift. Moreover, the time at which the peak occurs is defined as the time constant (τ) of the trapping mechanism, while the amplitude of the signal is proportional to the amount of trapped charge variation induced by the process [27]. Accordingly, we can conclude that Sample A is affected by two trapping processes (P1A and P2A) while Sample B is affected by one single trapping process P1B which is characterized by the same time constant and same trapped charge variation of process P1A.

To better study the physics behind the observed behavior, we tested the two samples at different temperatures in the range between 25 °C and 125 °C. The results obtained on Sample A are reported in Figure 6.

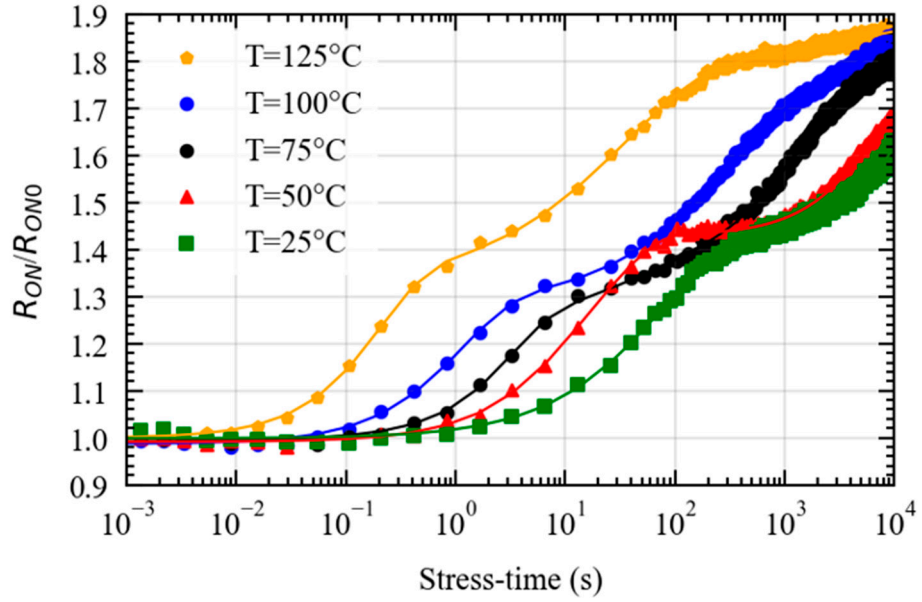

Figure 6. Dynamic-R_{ON} (R_{ON}/R_{ON0}) transients acquired at different temperatures (ranging between 25 °C and 125 °C) with $V_{D,OFF}$ = 50 V on Sample A.

As we can see by looking at Figure 6, an increase in temperature produces a speed-up in the dynamic-R_{ON} transients. This is visible for both Process P1A and P2A, suggesting

that the physical mechanisms governing both processes feature a positive thermal coefficient. This means that a thermally activated process like charge emission from traps and/or charge conduction mechanisms can be considered as possible explanation for the experimental evidence.

In order to make a comparison between the two samples available, the same characterization was repeated on Sample B, changing the temperature in the same range between 25 °C and 125 °C (see Figure 7).

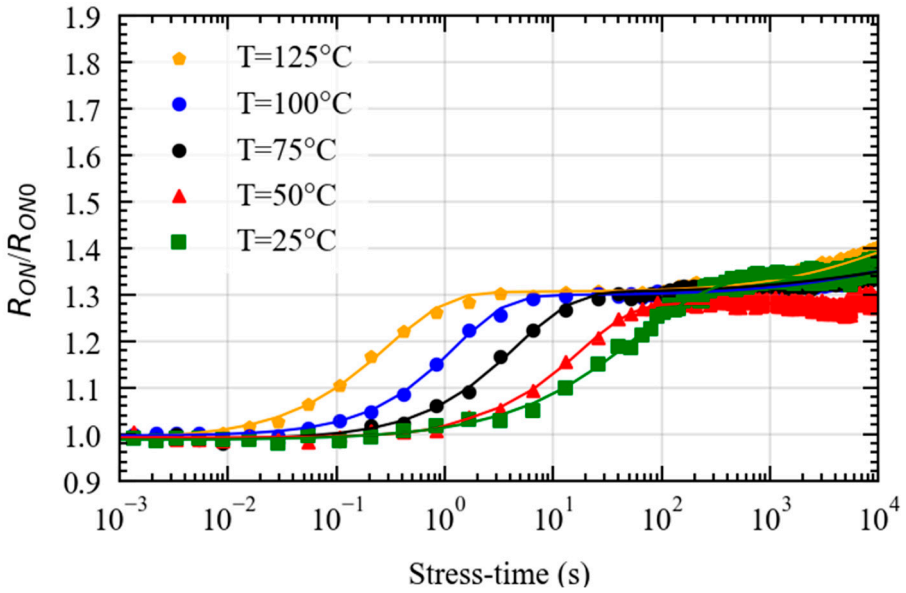

Figure 7. Dynamic-R_{ON} (R_{ON}/R_{ON0}) transients acquired at different temperatures (ranging between 25 °C and 125 °C) with $V_{D,OFF}$ = 50 V on Sample B.

By looking at the results reported in Figure 7, two important considerations can be made: (i) the process P1B is accelerated by an increased temperature, similarly to what was observed on Sample A for process P1A; (ii) the second process (that was marked on Sample A as P2A) is not present on Sample B in the whole temperature range explored. This thermal analysis is very important to further investigate the origin of the two degradation processes observed. To this end, we extracted the time constant obtained at different temperature for the two processes. To do so, all the experimental transients were fitted by means of stretched multiexponential functions [22–26] and the related tau (τ) were extracted in correspondence to each peak in the derivative plot [28]. The time constants (τ) extracted in this way are then used to build the Arrhenius plot reported in Figure 8.

The Arrhenius plot give us some important information. First, the processes P1A and P1B shows perfectly overlapped results, indicating the same activation energy (i.e., same slope of the points in the Arrhenius plot) and trap cross-section. Moreover, the P1A and P1B plots are quite aligned with the Arrhenius plot reported by Chen et al. in [29]. In that case, the R_{ON} degradation, and thus the Arrhenius plot obtained, was associated to the hole emission from C-related acceptors in the GaN buffer. Particularly, the relatively high drain voltage applied in off-state yields the emission of holes from C_N states in the buffer that exposes fixed negative charge in the layer, partially depleting the 2DEG [30–34]. This negative charge cannot be promptly recovered when the device is set back to on-state, causing a reduced DUT conductivity (i.e., an increased R_{ON}). Accordingly, P1A and P1B of this study are likely to be induced by the same physical mechanism. This is not only due to the good agreement between our experimental data and the previous report by Chen et al., but also by the fact that both Samples A and B in our study featured the same Carbon-doped GaN buffer layer and growth conditions. Given the commonality between

P1A and P1B, the root cause for both processes must be linked to this strong common feature between the two samples.

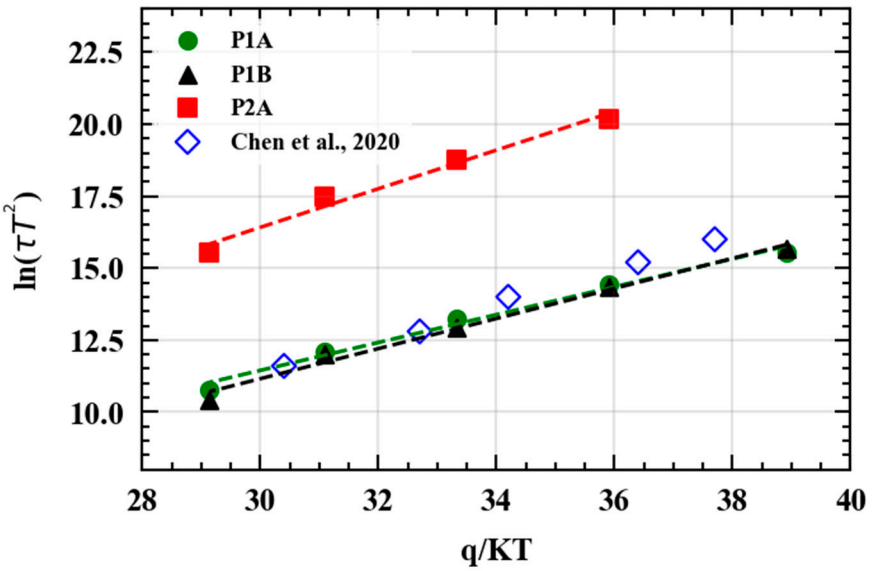

Figure 8. Arrhenius Plot obtained for the physical processes P1A, P1B and P2A. Processes P1A and P1B share similar coordinates with respect to the ones reported by Chen et al. in [29], suggesting that C-related Buffer traps are the responsible for both processes. Conversely, the process P2A is located in a different space of the Arrhenius plot and is likely to be related to a completely different mechanism.

On the other hand, the fact that the process P2A occupies a different location in the Arrhenius plot, indicates that this process must be related to a completely different mechanism. Moreover, this mechanism is present only on Sample A and totally absent on Sample B. Accordingly it must be linked to a different fabrication step between the two DUTs. In this scenario, the only difference between the two samples was related to the SiN passivation stoichiometry. For this reason, the trapping mechanism responsible for the additional degradation on Sample A is likely to take place at device surface where the SiN passivation is deposited.

According to this analysis, process P2A can be related to the accumulation of negative charge inside the SiN dielectric or at the interface between the SiN passivation and the AlGaN surface. Similarly to process P1, an increased negative charge in this region can repel electrons in the 2DEG, thus increasing the R_{ON} of the DUT.

Actually, several mechanisms can be responsible for trapping in this region and they can be divided in two main categories: (i) degradation due to hot-carriers and (ii) degradation due to off-state drain bias stress. Particularly, hot carrier effects have been reported by several literatures to be one of the main cause for negative charge accumulation at the surface of GaN-based HEMTs, linked to 2DEG electrons that overcome the potential barrier and get trapped in this region of the device. However, even without hot carriers, high field in the gate-drain access region can be responsible for the ionization of surface states [7], as well as injection of charges from the field-plate structure towards the AlGaN surface [11]. This would produce a similar electrical effect, since the negative charge stored at the surface yields a similar 2DEG depletion.

The test setup employed so far is not sufficient to discriminate between category (i) and (ii), since the device is subjected to relatively high drain bias in off-state and also experiences transitions at non-zero current that could be responsible for hot-carrier effects due to the simultaneous presence of large carrier density and high electric field in the channel.

In order to better study the mechanism responsible for process P2A, it is important to insulate hot-carrier effects from drain off-state voltage stress. To do so, a soft switching characterization is required, since transitions performed at zero-current can completely prevent hot carrier effects and leave drain off-state stress as the only possible player.

Accordingly, Section 5 reports the results obtained in soft-switching mode for the same Sample A and Sample B under investigation.

5. Soft-Switching Characterization

The Soft-Switching Characterization was performed by means of a commercial measurement setup AM3200 (see Figure 9). It consists of two synchronized pulse generators that are able to drive the gate and drain terminals of the DUT without having the crossing between V_{GS} and V_{DS} during the transitions. This ensure to achieve the Soft-Switching trajectory reported in Figure 9 and guarantee the absence of hot carrier effects.

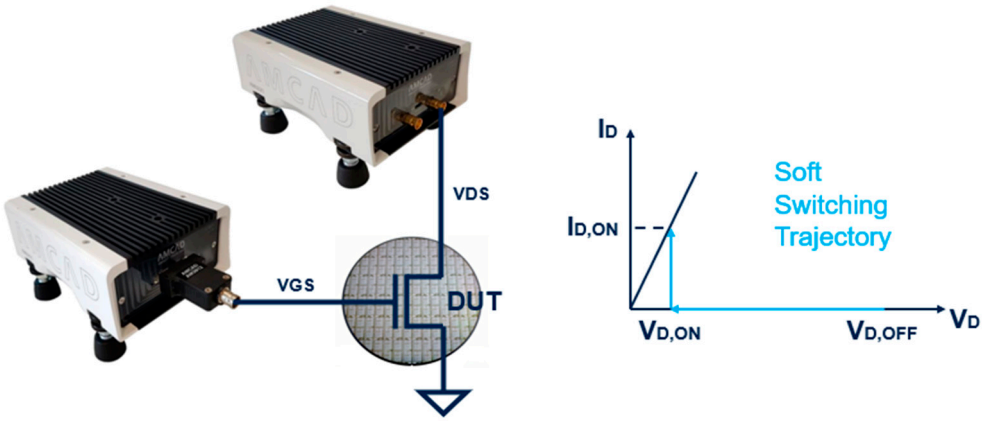

Figure 9. Simplified schematic of the commercial setup (AM3200 by AMCAD) used for the characterization of the DUT under soft-switching conditions and related switching trajectory experienced by the DUT during the ON/OFF, OFF/ON commutations.

The setup was programmed in order to obtain the same on-the-fly characterization presented in Section 3, so that the continuous switching behavior is still maintained but the hot-carrier interaction can be avoided. The Stress/Measurement sequence implemented with the AM3200 system is shown in Figure 10, in which the dead time between V_{DS} and V_{GS} transitions is highlighted (about 200 ns).

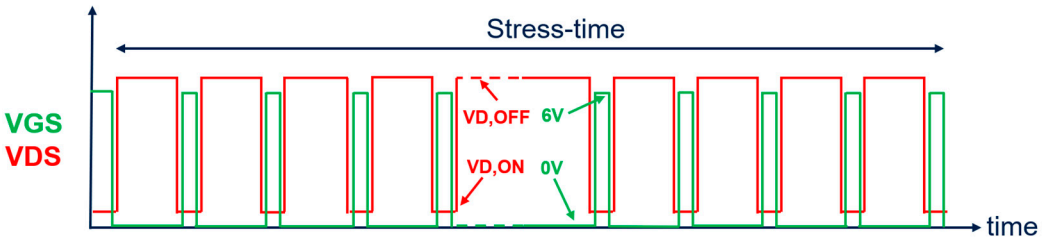

Figure 10. Typical waveforms experienced during the on-the-fly characterization with the commercial experimental setup AM3200. The V_{GS} signal is pulsed with 2 µs T_{ON} and 10 µs period between 6 V $V_{G,ON}$ and 0 V $V_{G,OFF}$; accordingly, the V_{DS} changes between low $V_{D,ON}$ (<0.5 V to bring the DUT in its linear region) and relatively high $V_{D,OFF}$. The V_{DS} transitions are performed at zero-current in order to drive the DUT in soft-switching conditions.

In this case, the T_{ON} was kept at 2 µs and the same period used with the custom setup was maintained (10 µs). However, the stress time was reduced to 1000 s. This is mainly due to the fact that the commercial system does not have the option to logarithmically trigger

the acquisitions as done for the custom system and to avoid the saturation of the memory with a linear sampling distribution, the time resolution was decreased. In fact, the system was able to monitor just four decades of time (e.g., from 0.1 s to 1000 s).

Sample A and Sample B were first tested with a $V_{D,OFF}$ equal to 50 V at 100 °C and 150 °C. The experimental results obtained are reported in Figure 11a and Figure 11b, respectively.

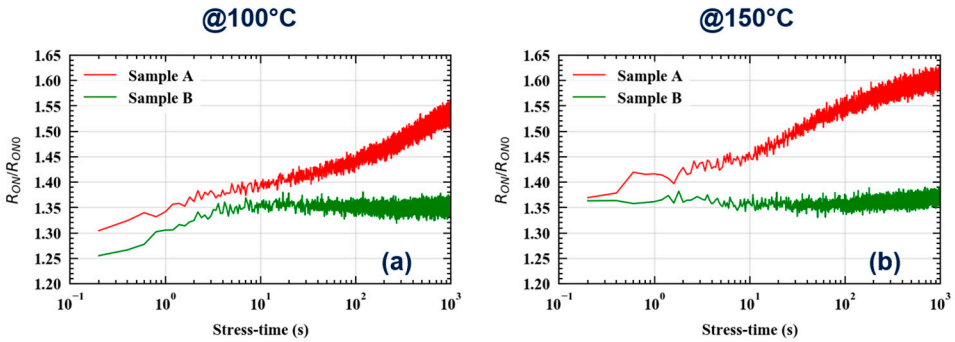

Figure 11. Dynamic-R_{ON} (R_{ON}/R_{ON0}) transients acquired the AM3200 system at 100 °C (**a**) and 150 °C (**b**) on Sample A and Sample B. In Both cases, $V_{D,OFF}$ was fixed at 50 V.

The results presented in Figure 11 yield two important insights. First of all, the difference between Sample A and Sample B is visible also with the AM3200 setup. In fact, Sample B reaches a steady state degradation before 10 s of cumulative stress time at 100 °C, whereas Sample A shows an additional drift for longer stress times. Moreover, the R_{ON} degradation transients are thermally activated, since we observed a speed-up while increasing the temperature to 150 °C. This indicates that we are able to observe the same electrical effect also in Soft-Switching conditions. Thus, the process P2A that is visible only on Sample A is not due to hot carrier effects, but purely induced by the off-state drain bias. In fact, hot carrier effects are expected to show a negative thermal coefficient due to a reduced mean free path for carriers when temperature increases. Conversely, the positive thermal coefficient observed for both processes P1 and P2, along with the coherent results observed for restive load and soft-switching trajectories, can be used to rule out hot-electrons as a possible explanation for the dynamic-R_{ON} drifts analyzed in this work. Another important observation is related to the measurements performed at 150 °C. In fact, the first point acquired after 0.2 s of stress on Sample A and Sample B is quite aligned. Then, Sample B shows a stable parameter for longer stress time, while Sample A starts to increase and approach a stable value only after 1000 s. This suggests that, at 150 °C, we can appreciate the whole dynamics of the process P2A in the 0.2 s to 1000 s time window. Accordingly, the characterization at 150 °C can be used to study just the process P2, since the process P1 is too fast to fall inside the measurement window and thus provides a common offset for both Sample A and B in the observation time window. Based on this assumption, we can further investigate the mechanism responsible for process P2A by studying the impact of the $V_{D,OFF}$ level only on the P2A related R_{ON}-drift. To this end, we performed the same characterization at 150 °C, by varying the $V_{D,OFF}$ in the 10 V to 80 V voltage range. The results obtained are reported in Figure 12a in which the dynamic R_{ON} transients are presented in terms of R_{ON}/R_{ON0*} ratio. More specifically, the parameter R_{ON0*} is the R_{ON} value measured after 0.2 s of stress time which provides the common offset of process P1. In this way, we are able to discard the R_{ON}-drift due to P1A and just see the drift induced by the process P2A.

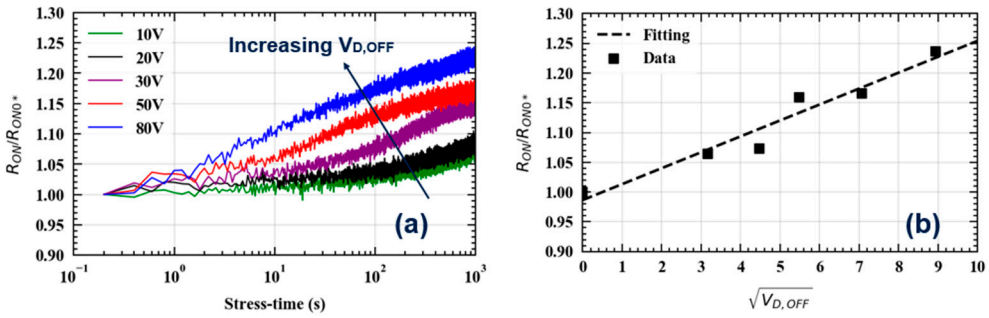

Figure 12. (**a**) Dynamic-R_{ON} (R_{ON}/R_{ON0*}) transients acquired the AM3200 system at 150 °C at different $V_{D,OFF}$ levels (10 V, 20 V, 30 V, 50 V and 80 V). (**b**) Dynamic-R_{ON} (R_{ON}/R_{ON0*}) value obtained after 1000 s of stress time represented as a function of the square root of the corresponding $V_{D,OFF}$.

The data reported in Figure 12a shows that the applied $V_{D,OFF}$ has a double effect on the dynamic-R_{ON} induced by process P2A. (i) Increasing $V_{D,OFF}$ we see a speed-up in the dynamic-R_{ON} transient and (ii) increasing $V_{D,OFF}$ we see an increase in the R_{ON}-drift. This effect can provide important insights in the underlying physics and to further investigate the root cause for the process P2A, we built the correlation graph of Figure 12b. In fact, by plotting the R_{ON}-drift of process P2A with respect to the square root of the $V_{D,OFF}$ stress applied we found a pretty good linear correlation. This dependence on the square root of the applied voltage (i.e., applied field) is a typical signature of Poole-Frenkel conduction [35]. This kind of conduction mechanism is the one typically governing the leakage inside SiN dielectrics [36,37]. Since the process P2 has been already associated to the SiN passivation dielectric, this observation suggests that the injection of negative charges across the SiN dielectric can be considered as the root cause for the observed P2A in Sample A. In order to further understand if this hypothesis is valid, we characterized the SiN dielectric properties of Sample A and Sample B in Section 6.

6. SiN Dielectric Characterization and Physical Mechanism

In this Section we focused our attention on the characterization of the different SiN passivation featured by Sample A and Sample B. Particularly, we wanted to investigate the insulating properties of the two different dielectrics to correlate them with the observed dynamic-R_{ON} behavior. To do so, we employed a simplified test structure which consisted on a simple Capacitor obtained between the field-plate metal and the 2DEG, separated by the SiN dielectric. The simplified cross section of the tested structure is shown in Figure 13a.

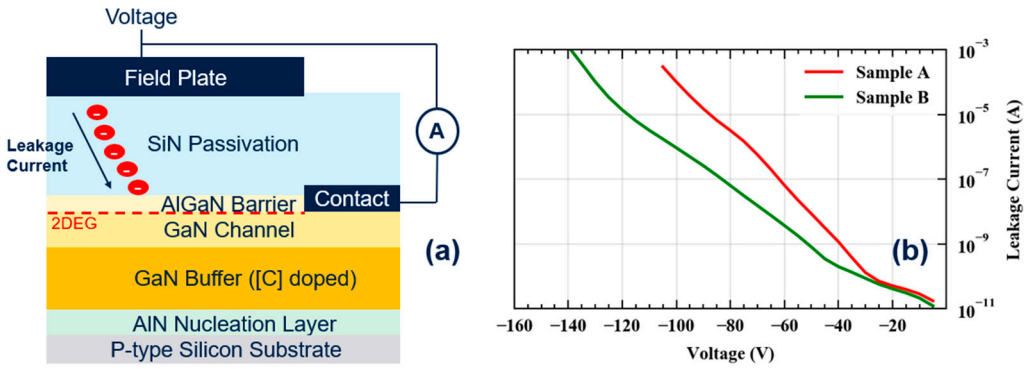

Figure 13. (**a**) Test Structure used to measure the leakage current across the SiN passivation layer. (**b**) Leakage current measured across the SiN Passivation on Sample A and Sample B by applying a negative voltage on the metal field-plate.

The test consisted in the application of a negative voltage between the field-plate metal and the ohmic contact in touch with the 2DEG and to the monitoring of the current

across the Capacitor (i.e., across the SiN dielectric). This configuration is similar to the one experienced by the real transistor when relatively high drain bias are applied to the drain ohmic contact, since the Source Field-Plate is grounded and the Field-Plate experiences a negative potential difference with respect to the ohmic drain. The leakage current was measured on both Sample A and Sample B, yielding the difference highlighted in Figure 13b. As we can see, the Sample A show a larger leakage current with respect to the Sample B, stemming for an increased electron flow across the SiN dielectric. These different isolation properties can explain the difference in dynamic-R_{ON} behavior between the two tested samples according to the simplified schematic reported in Figure 14.

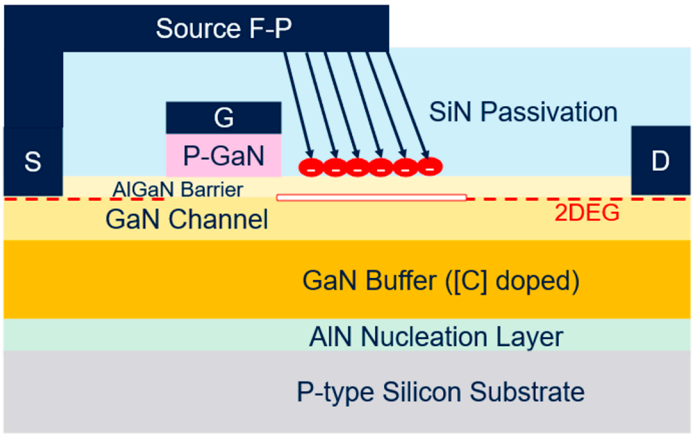

Figure 14. Schematic of the proposed mechanism for explaining the additional dynamic-R_{ON} drift experienced by sample A for long stress time: the injection of electron from the field-plate to the surface induces the trapping of negative charges at the SiN/AlGaN interface, yielding a partial depletion of the 2DEG underneath and a consequent rise in the DUT's R_{ON}.

In fact, the physical mechanism responsible for the R_{ON}-degradation process P2A can be synthetized as follows. At relatively large Drain bias, the negative Field-Plate to Drain potential favors the injection of electrons towards the device surface. This flow of electrons is stronger on Sample A as indicated by the higher leakage current in Figure 13b. This electron flow can be trapped in pre-exiting states at the Passivation/AlGaN interface or inside the SiN passivation and deplete the 2DEG underneath, thus reducing the 2DEG density and increasing the R_{ON} of the DUT. This explanation is consistent with the $V_{D,OFF}$ dependence observed for the process P2B, since the leakage across the SiN passivation increases with the applied voltage. It is important to mention that the different SiN stoichiometry between Sample A and Sample B can also affect the amount of trap states at the device surface and/or inside the dielectric that can be filled by the injected negative charge. This difference, accompanied by a different leakage current, yields to the overall different behavior of the two samples, highlighting the strong impact of the SiN passivation on the dynamic-R_{ON} degradation of the tested devices.

7. Conclusions

In this work, the impact of SiN Passivation on dynamic-R_{ON} degradation of AlGaN/GaN HEMTs devices was put in evidence. To this end, we compared two samples showing different SiN Passivation stoichiometry marked as Sample A and Sample B. For dynamic-R_{ON} tests, two different experimental setups have been employed to investigate the R_{ON}-drift showing up during conventional switch mode operation by driving the DUTs under both (i) resistive load and (ii) soft-switching trajectory. This allowed us to exclude hot carriers as the reason for the observed drifts. Conversely, the increased R_{ON} was totally associated to the relatively high drain bias applied in off-state. Interestingly, a

significant difference was observed between Sample A and Sample B dynamic behavior, indicating a strong impact of the SiN passivation layer on the R_{ON} drift. Sample A was affected by an additional R_{ON} drift that was not present on Sample B. This additional drift was explained by the injection of negative charges from the Source Field-Plate towards the AlGaN surface that are captured by surface/dielectric states and partially depletes the 2DEG underneath. This was in line with higher leakage current measured across the SiN layer of Sample A. This result is very important because it puts in evidence the role of the SiN passivation dielectric in defining the dynamic behavior of GaN-based HEMTs. Moreover, the correlation found between the leakage current across the dielectric and the dynamic-R_{ON} drift, suggests that the leakage measurement can be used as a diagnostic tool to find possible weaknesses in the SiN passivation without the need to perform the complete dynamic tests.

Author Contributions: M.C. and G.C. contributed equally to this work. Conceptualization, M.C. and G.C.; methodology, M.C.; software, A.P.; validation, A.P., A.C. (Alessandro Chini) and M.C.; formal analysis, M.C.; investigation, M.C. and G.C., resources, F.I., A.C. (Aurore Constant) and M.E.C.; data curation, M.C. and G.C.; writing—original draft preparation, M.C. and G.C.; writing—review and editing, M.C., G.C., G.G. and C.M.; visualization, M.C.; supervision, M.E.C. and F.I.; project administration, F.I.; funding acquisition, F.I. All authors have read and agreed to the published version of the manuscript. Maria Eloisa Castagna passed away prior to the publication of this manuscript. All other authors have read and agreed to the published version of this manuscript.

Funding: This research was funded by the ECSEL JU under Grant Agreement No. 101007310.

Data Availability Statement: The data presented in this study are available on request from the corresponding author due to confidentiality reasons.

Acknowledgments: The authors would like to acknowledge Gianluca Marletta, Santo Reina, Santo Principato and Clarice Di Martino for the technical support.

Conflicts of Interest: The authors declare no conflict of interest.

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