Analysis of Dynamic-R_{ON} and V_{TH} shift in on-wafer 100-V p-GaN HEMTs Emulating Monolithically Integrated Half-Bridge Circuits

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***Abstract*—In this paper, we present electrical characterization data concerning the degradation of critical device parameters (threshold voltage, V_{TH}, and on-state resistance, R_{ON}) of 100- V p-GaN HEMTs to be employed in monolithically integrated half-bridge circuits. To this purpose, a custom characterization setup emulating the stress conditions of either the Low Side (LS) or High Side (HS) device was realized. This was necessary as the LS device degrades only during the OFF-state condition, whereas the HS device degrades also during the ON-state as a consequence of the finite source-to-body voltage. In either configuration, the device is periodically switched on and off (T_s = 10 µs and t_{ON} = 2 µs) for up to 1000 s and both V_{TH} and R_{ON} are monitored for several decades to determine the time evolution of the parameters. The interpretation of experimental results was aided by calibrated device numerical simulations. We found that both LS and HS device have the same V_{TH} and R_{ON} dynamics, but the HS device experiences a larger degradation of both parameters due to the back-gating effect. Characterization performed at different substrate temperature (T) revealed an activation energy of ≈0.7 eV for both V_{TH} and R_{ON} transients, which is signature of hole emission from C-related buffer traps. Furthermore, hole leakage current from the Schottky gate during ON-state was found to be beneficial as it partially compensates the building up of negative charges in buffer.**

Index Terms*— *p-GaN HEMTs, Half-Bridge, Dynamic R_{ON}, Hole Redistribution Model, C-doping, V_{TH} Drift, Gate leakage

I. INTRODUCTION

GaN High Electron Mobility Transistors (HEMTs) are leading the wave of next-generation power switches due to their high frequency and high power density capability [1]. Lateral GaN-on-Si technology is particularly appealing due to the possibility of monolithically integrate the GaN HEMTs inside integrated circuits (ICs), allowing for a compact design of the power module with reduced parasitics [2]. Despite the high potential of the technology, charge trapping processes that take place both at the surface and in the buffer affect the stability and reliability of these devices [3], [4], [5] . Generally, trapping-related issues are addressed in the literature at the device level to focus on the physics of the trapping processes [6], [7], [8], [9], [10], [11], and therefore do not investigate the effects of degradation on the device in a switching circuit under practical bias conditions. For instance, GaN devices to be monolithically integrated in a power IC share a common substrate potential. This causes, for instance, High Side (HS) and Low Side (LS) devices in a half-bridge configuration to have different source-to-substrate potential (depending on the state of the device itself) which is turn leads to different levels of degradation of ON-resistance (R_{ON}) and threshold voltage (V_{TH}) [12]. Although several isolation techniques can be employed to mitigate these effects, we investigated the feasibility of half-bridge integration using standard GaN HEMT structures without any additional isolation layers. Quantifying and understanding the different degradation behavior of LS and HS devices is mandatory for successful application of GaN HEMTs in monolithically integrated converters.

This work aims to fill this gap by investigating the degradation mechanisms of GaN HEMTs under realistic switching conditions, focusing on both HS and LS devices. Previous studies have addressed the effects of gate leakage, dynamic ON-resistance, and threshold voltage shifts in either LS configurations or back-gating conditions [12], [13], [14], [15]. This study explores the transient dynamics of R_{ON} and V_{TH} in HS configurations up to 100 kHz of switching frequency, providing novel insights into the distinct stress-induced degradation mechanisms affecting HS devices. This study extends our previous conference papers [16], [17] by including new experimental data on V_{TH} degradation in both LS and HS configurations, with a focus on the effects of varying temperature and duty-cycle.

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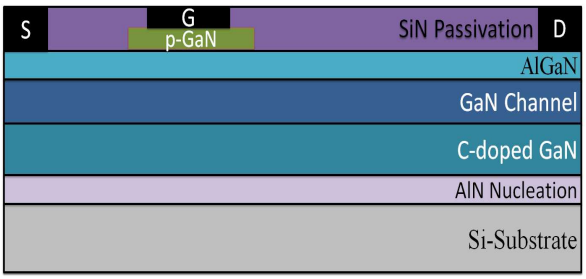

Fig. 1 Cross-Section of the DUT (a). The combination of L_{GD} < 2 µm and the p-GaN contact under the gate ensure a normally-off operation in the 100 V range.

We found that the activation energies (E_A's) of V_{TH} and R_{ON} are comparable for both LS and HS configurations meaning that the effect causing the degradation is the same (e.g. C-related acceptor in buffer).

Reducing the Duty cycle in HS reduces the ON-stress and makes the degradation level closer to the one present in LS. Gate leakage from the Schottky diode compensate the back-gating effect. Simulations have been refined based on the experimental results and have been used to confirm and provide a physical interpretation of the obtained experimental results.

The paper is organized as follows. Section II describes the DUT and the design of the custom circuit used to assess degradation of LS and HS devices. Section III reports on the experimental results obtained at different temperature and duty cycle. Section IV presents the numerical simulation results that were carried out to aid the interpretation of the results. Section V draws the conclusions of this work

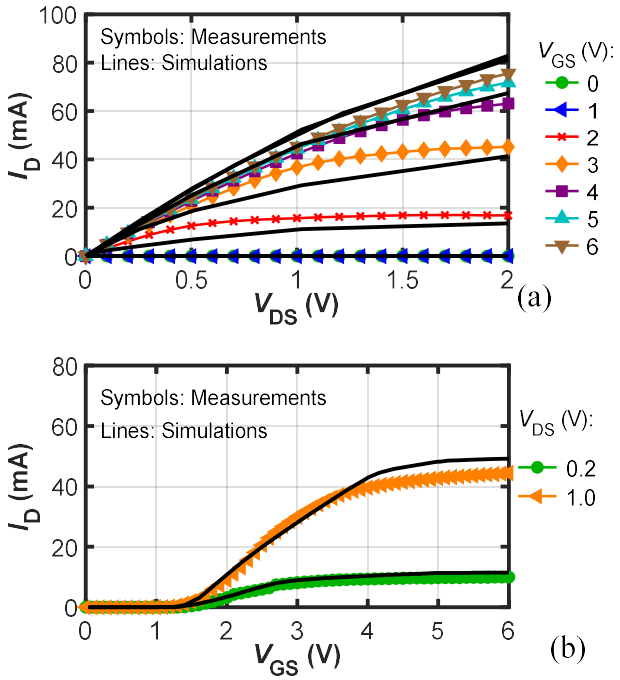

Fig. 2. Measured and Simulated I_D-V_{GS} (a) and I_D-V_{DS} (b). There is a good match between simulations and measurement. From (a) we can extract V_{TH}= 1.5 V and from (b) R_{ON} = 20 Ω.

II. Device Under Test (DUT) and Circuit Design

This section describes the Devices Under Test (DUTs) and the custom circuit was used to emulate the half-bridge configuration to assess degradation of LS and HS devices.

A. DUT Description

Device Under Test (DUT) is an on-wafer AlGaN/GaN heterojunction HEMT, presenting a short gate length (L_G < 1 µm). A p-GaN gate is used to achieve normally-off operations, depleting the 2-DEG at the AlGaN/GaN interface under the gate even for V_{GS}=0 V. Gate-Drain distance (L_{GD}) is below 3 µm allowing operation in the 100 V range, GaN buffer was doped with Carbon to obtain a semi insulated layer [6]. The schematic cross-section of the device is shown in Fig. 1. The typical DC transfer (I_D-V_{GS}) and output curves (I_D-V_{DS}) are shown in Fig. 2. The extracted static threshold voltage and ON-resistance are 1.5 V and 20 Ω, respectively.

B. Circuit Design

Devices monolithically integrated in a half-bridge circuit share the same substrate potential, which leads to different

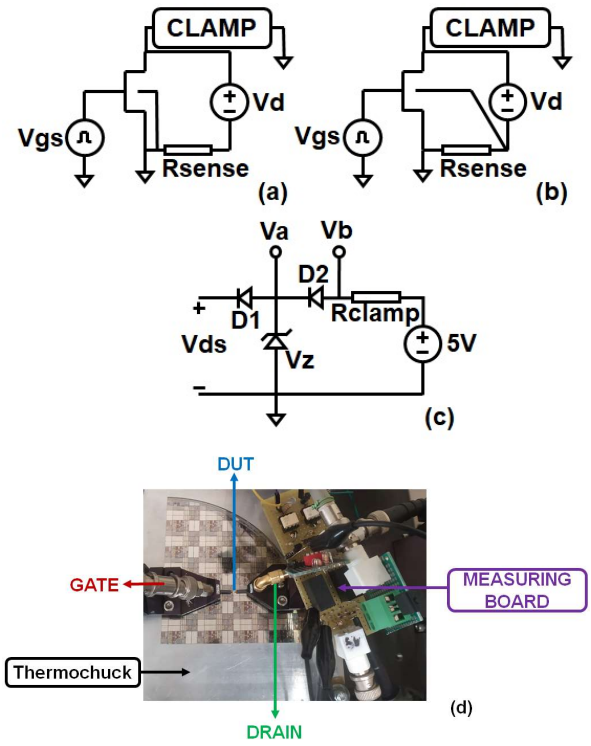

Fig. 3 Circuit used for the measurement in LS and HS. In LS (a) the body and the source are tied together, while in HS (b) the body of the DUT is connected to the negative pin of the V_D, emulating the HS device in half-bridge configuration. The clamping circuit (c) blocks the rise of the V_{DS} in the OFF-state to the Zener voltage (4.7 V) to improve the DSO resolution. In the ON-state, $V_{DS} = 2V_a$-V_b. A photograph (d) of the measurement setup is shown for reference.

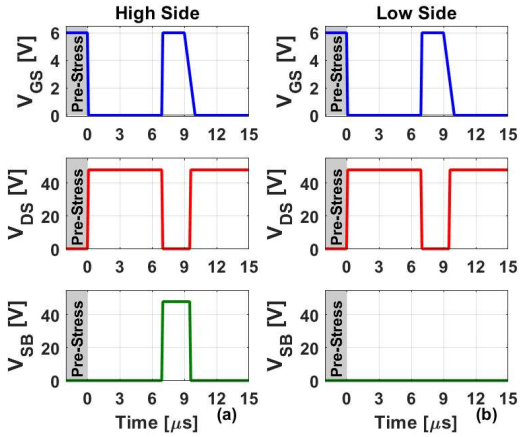

Fig. 4 In HS (a) V_{DS} switch between 48 V and ~200 mV while there is a non-null voltage between source and body (V_{SB} = 48 V) during the t_{on}. In LS (b) the V_{DS} behaves like in HS, but the substrate and the body are tied together (V_{SB} = 0 V).

degradation of devices depending on whether they are in the LS or HS configuration. To assess the different degradation mechanisms on on-wafer devices we realized a custom circuit that emulates the operation in either LS or HS configuration on standard GSG layout device structures typically adopted during the development of power device technology [18], [19].

The circuit is schematically depicted in Fig. 3. V_D = 48 V is provided through a couple of DC/DC isolated converters. R_{SENSE} is used to probe the DUT current and thus to measure both V_{TH} and R_{ON}. The clamping circuit is used to improve the resolution of the acquired signal by the Digital Storage Oscilloscope (DSO) considering the large voltage span over the DUT between 48 V (OFF-state) to ~ 100 mV (ON-state) [20].

To emulate the bias condition for the device in LS configuration, both the source and the substrate/body terminals are grounded. This ensures that the source-body voltage (V_{SB}) remains at 0 V regardless of the state of the device. Conversely, for the device in HS configuration, the body terminal is shorted to the negative terminal of the DC/DC isolated converter that provides the supply voltage. This way, the body terminal is effectively floating and sets its value to either 0 V or $-V_D$ depending on whether the device is in the OFF- or ON-state, respectively. By connecting the body to the source or to the negative terminal of V_D (see Fig. 3) it is possible to select the configuration that emulates either LS (panel a) or HS (panel b) bias conditions. Fig. 3 (d) shows a picture of the measurement setup described above.

III. Experimental Results

A. Switching Measurements

For the R_{ON} and V_{TH} experiments we use a waveform generator to drive the DUT's gate terminal with a pulsed signal that modulates V_{GS} between 6 V and 0 V to switch from ON- to OFF-state. The measurements are performed with a period of T_s = 10 µs, t_{ON} = 2 µs and a fall time of 1 µs. During t_{ON} and the fall time,

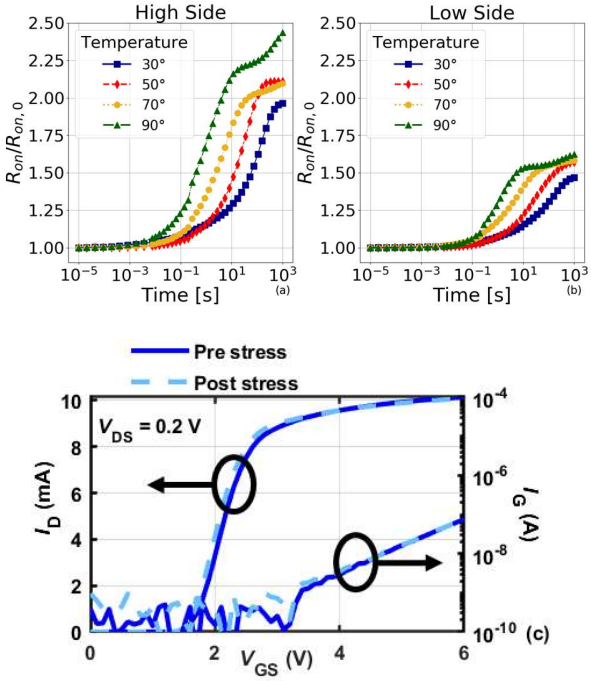

Fig. 5 R_{ON} degradation for HS (a) and LS (b) for different temperatures, the temperature accelerates the traps dynamic and the maximum degradation. The DC characterization performed before and after the stress (c) show no difference, meaning that the degradation is fully recoverable.

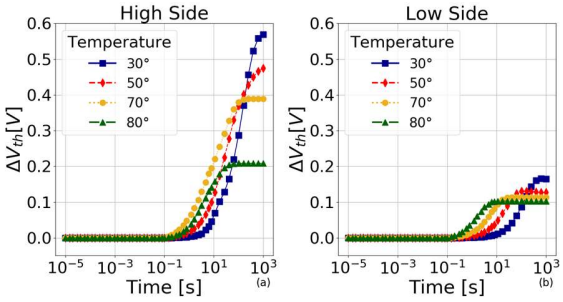

Fig. 6 V_{TH} degradation for HS (a) and LS (b) the dynamic is the same seen for R_{ON}. The reduced maximum V_{TH} shift with increasing temperature can be attributed to the increasing free hole density in the p-GaN layer with higher T.

the drain current is extracted to determine the ON-resistance and the threshold voltage, similarly to what reported in [21].

V_{TH} is extracted as the V_{GS} value at which I_D is equal to 1 mA. The total measurement time is 1000 s for both V_{TH} and R_{ON}. We repeat both measurements at different substrate temperatures (T) from 30 °C to 90 °C (ΔT = 20 °C) for R_{ON} and from 30 °C to 80 °C (ΔT = 20 °C from 30 °C to 70 °C and ΔT = 10 °C from 70 °C to 80 °C) for V_{TH}. A thermal chuck was employed to set and control the temperature. The setpoint temperature was reached and maintained for 5 minutes before connecting the DUT to ensure it was reached and stabilized before the stress

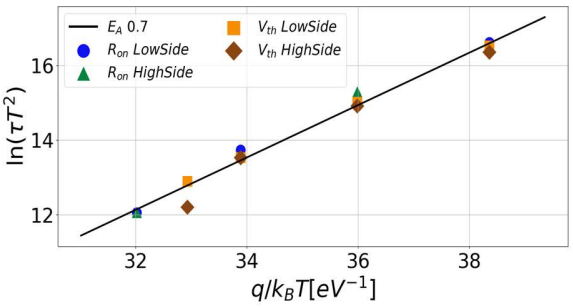

Fig. 7 Arrhenius Plot for V_{TH} and R_{ON} in HS and LS. An overall good match between the time constant and the E_A extracted was observed, compatible with the hole emission from the C-related acceptor traps in buffer.

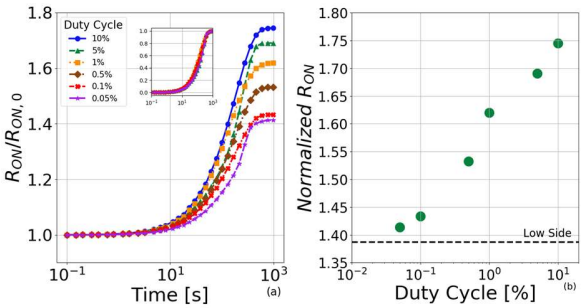

Fig. 8 R_{ON} transient (a) and maximum value (b). The black dotted line represents the LS limit that is the value that theoretically the HS should reach when the Duty Cycle (δ) is 0%. As δ increases, R_{ON} increases as well.

measurement begins. From the temperature measurements, we can calculate the time derivative to extract the time constants (τ's), which are then used to construct the Arrhenius plot and determine the activation energies (E_A's). In Fig. 4 the first period of the waveform used for the measurement is shown for HS, see panel (a) and LS, see panel (b). Before the beginning of the measurement, we keep the device at $V_{SB} = 0$ V and $V_{DS} \sim 100$ mV to set a common, stress-free initial condition for both LS and HS case.

The dynamic on-resistance ($R_{ON}/R_{ON,0}$) is shown in Fig. 5 at different temperatures for both LS and HS configurations. $R_{ON,0}$ is taken as the first R_{ON} measurement of the stress sequence. As it can be seen from Fig. 5, in both cases dynamic R_{ON} is similarly accelerated by temperature, but the amplitude of the degradation is not the same.

Specifically, for the LS configuration the maximum degradation increases from ≈ 45% at 30 °C to ≈ 60% at 90 °C.

For the HS case instead, the maximum degradation increases from ≈ 95% at 30 ° C to ≈ 140% at 90 °C. LS device degrades due to the electrical stress from the drain only when the device is in OFF-state (V_{DS} = 48 V) [22]. In HS we have an additional stress component that arises from the non-null source-to-body voltage in ON-state [23].

In fact, in this case the so-called back-gating effect (due to $V_{SB} >$ 0 V) reduces the 2-DEG with respect to the LS case and thus increases the degradation caused by the C-related acceptor [13].

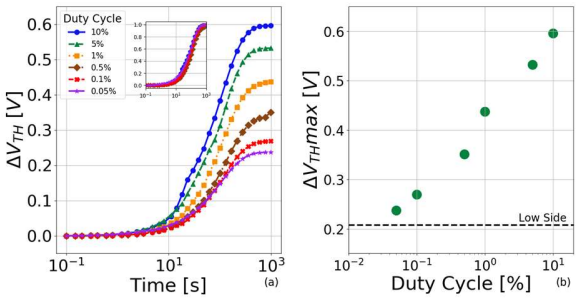

Fig. 9 V_{TH} transient (a) and maximum value (b). The black dotted line represents the LS limit that is the value that theoretically the HS should reach when the Duty Cycle is 0%. Also for V_{TH} there is a direct proportionality with δ that is coherent with the R_{ON} results.

Under these conditions, the additional degradation observed in HS is caused by an electrostatic effect present when the body and the source are at different potentials. As a result, the initial R_{ON} value as well as the amplitude of the dynamic-on resistance is higher in HS compared to LS, due to the depletion of the 2-DEG.

Moreover, Fig. 5c shows DC characteristics measured before and after applying the stress. As it can be seen, no significant difference is observed between the two sets supporting the hypothesis that the drift observed during the switch-mode operation is related to a fully recoverable mechanisms due to charge/discharge of traps located in the carbon doped GaN-buffer layer.

The V_{TH} drift (V_{TH}-$V_{TH,0}$) is shown in Fig. 6 at different temperatures. The V_{TH} dynamics has the same behavior of the one already observed for R_{ON}. In HS, see Fig. 6 (a), the maximum drift reduces from about from about 0.55 V at 30 °C to 0.2 V at 80° C. In LS, see Fig. 6 (b) it reduces from about 0.18 V at 30° to 0.1 V at 80 °C. Since ΔV_{TH} decreases with temperature, we chose to stop at 80 °C, because at 90 °C the threshold shift becomes too small and difficult to measure with sufficient precision.

The enhanced V_{TH} shift observed in the HS case with respect to LS has the same root cause as that of the dynamic R_{ON}, i.e., the back-gating effect. Conversely, the reduced maximum V_{TH} shift with increasing temperature can be attributed to the increasing free hole density in the p-GaN layer with higher T (Mg is an acceptor with an energy level ≈0.2 eV above the valence band [1]) that reduces the depletion layer thickness at the Schottky junction with the gate metal, thus reducing the overall V_{TH} instability [24], [25].

From the R_{ON} and V_{TH} plot at different temperatures we can extract the time constant (τ) associated with each curve and build the Arrhenius plot to characterize the trapping phenomena behind the degradation effect. The Arrhenius plot is shown in Fig. 7. Notably, similar τ's are extracted from both R_{ON} and V_{TH} transients in either configuration, indicating that the mechanism causing both parameters drift is the same. The back-gating effect present in the HS configuration has the only effect of enhancing the degradation amplitude, while the dynamics (governed by the trapping process) remain unchanged between

LS and HS. Based on the extracted activation energy (E_A) of about 0.7 eV one can identify the degradation mechanism as being the hole emission from the C-related acceptor traps inside the buffer [26], [27], [28]. The OFF-state condition in fact induces an increase in hole emission from the afore mentioned traps, that consequently become negatively charged. An increase in the negative charge in the buffer under the access region and under the gate determines the observed increase in R_{ON} and V_{TH}, respectively. Surface-related dynamics effects either associated with the p-GaN layer and/or surface traps along the access region also affect instability of the devices. Previously, we observed different E_A (compared to the one extracted in this work) of both dynamic R_{ON} and V_{TH} drift after applying negative/positive gate bias stress [29], [30], suggesting that these effects do not play a major role in the time/temperature range under investigation in this work.

The deviation of the extracted E_A from the theoretical value for the C-related traps of 0.9 eV can be explained as being due to the Poole-Frenkel effect that causes a reduction in the barrier potential for hole emission from the C-related acceptor traps with increasing electric field, in turn determining an increased emission rate with respect to the equilibrium conditions [31].

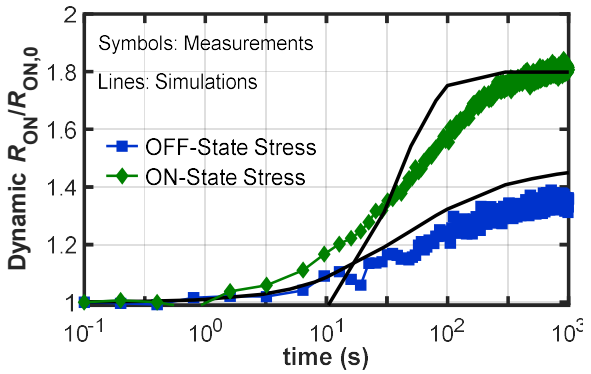

Fig. 10 Measured and simulated dynamic R_{ON} in term of $R_{ON}/R_{ON,0}$.The ON-state stress shows a significantly higher degradation respect to the OFF-state stress. this is caused by the back-gating effect that deplete the 2DEG during the ON-state.

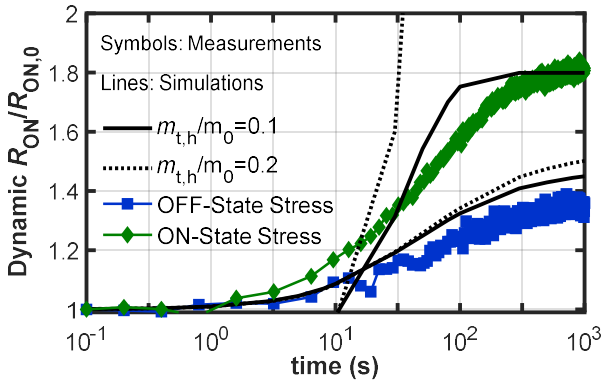

Fig. 11 Simulated dynamic R_{ON} in OFF- and ON-state stress conditions. Two sets of simulations are shown, for different hole tunneling mass affecting gate current (i.e., higher $m_{t,h}$, lower gate current). Experimental data is shown for reference.

B. Duty Cycle

Since the device in HS configuration degrades during both ON and OFF-state, we investigated the parametric degradation with varying duty cycle. Measures were obtained by switching V_{GS} between 6 V and 0 V to switch from ON- to OFF-state with a period of T_s = 100 ms with a duty cycle (δ) changing from 0.05% to 10%. The temperature was kept at 30 °C.

Fig. 8(a) shows the dynamic ON-resistance ($R_{ON}/R_{ON,0}$) with varying δ. The maximum R_{ON} degradation reduces from ≈ 75% for δ = 10% to ≈ 40% with δ = 0.05%, see Fig. 8b. As δ reduces, the overall degradation gets closer to the one found in LS because the ON-stress is reduced, as expected. To show that δ only affects the magnitude of the degradation but not the dynamics of the process, the inset of Fig. 8(a) shows dynamic ON-resistance for each δ plotted between 0 and 1 (i.e., translated by its initial value and normalized to its final value). Because all the normalized R_{ON} curves overlap with each other, they have the same τ of about 150 s, confirming that δ only affects the magnitude but not the dynamic process.

Fig. 9(a) shows the V_{TH} shift with varying δ. The behavior is similar to that of dynamic R_{ON}. In Fig. 9(b) the maximum V_{TH} drift is shown, threshold reduces from ≈ 0.6 V with δ = 10% to ≈0.25 V with δ = 0.05%. Also in this case, the dynamics of the process is not affected by variation of δ, see inset in Fig. 9(a). The fact that the dynamics of both R_{ON} and V_{TH} is not affected by δ further proves that the physical mechanism causing the parametric degradation is the same for both LS and HS devices.

IV. Discussion

To further investigate the physical mechanism responsible for the observed dynamic effects on R_{ON} and V_{TH}, we performed numerical device simulations. For this purpose, we used the commercial TCAD tool SDevice [32]. Drift-diffusion formalism was employed to simulate charge transport. Piezoelectric polarization charge at the AlGaN/GaN interface was computed through the default strain model of the simulator. To account for trapping effects in the buffer, associated with the presence of C-related acceptor traps, one Shockley-Read–Hall (SRH) trap-balance equation was used for each distinct trap level, thus allowing to compute dynamic trap occupation without any quasi-static approximation.

C-related traps in the GaN buffer were modeled by considering two trap levels, i.e., one dominant deep acceptor at E_V+0.9 eV and a shallow donor trap at E_C−0.11 eV [33], [34] . More details of the simulation setup can be found in our previous works where several experimentally observed degradation effects associated with trapping were modeled [22], [26], [30], [35], [36].

The high number of switching cycles (10^7 cycles for T_s = 10 µs), occurring during the experimental sequence used to extract dynamic R_{ON}, see Fig. 4, would require an impractical amount of time to simulate the exact same conditions used in the experiments. To perform a comparison as fair as possible, we performed dynamic R_{ON} experiments while applying either OFF-state or ON-state stress for a total cumulative time of 1000 s.

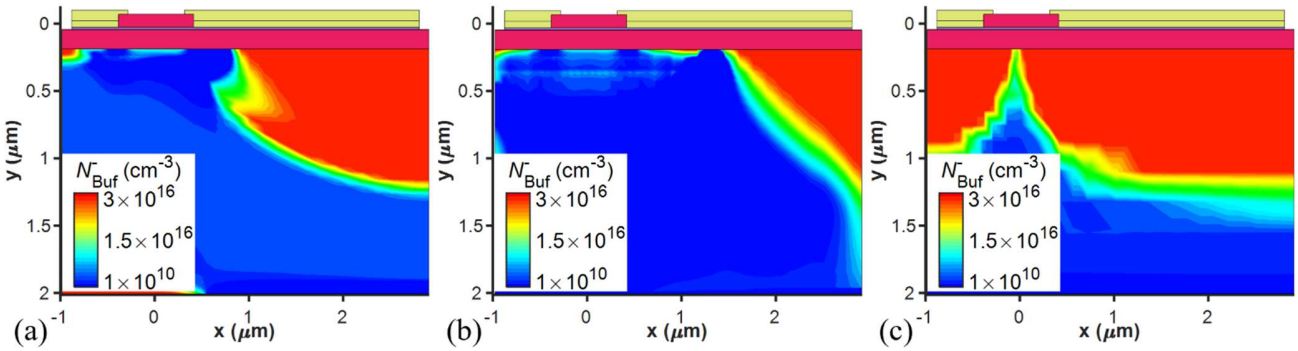

Fig. 12 Simulated net ionized acceptor trap concentration ($N^-_{C,Eff}$) in the buffer after 1000-s stress in (a) OFF-state and (b) ON-state conditions (with $m_{t,h}/m_0 = 0.1$). High voltage stress leads to hole emission from C-related acceptor traps in the buffer that become negatively charged, in turn causing R_{ON} degradation. During ON-state stress, the positively biased gate terminal injects hole into the device that partially neutralize acceptor traps under the source and gate contacts. Panel (c) corresponds to the limit case, i.e., 1000-s stress in ON-state conditions with no gate current, which corresponds to considerable dynamic R_{ON}, much higher than the experimental one.

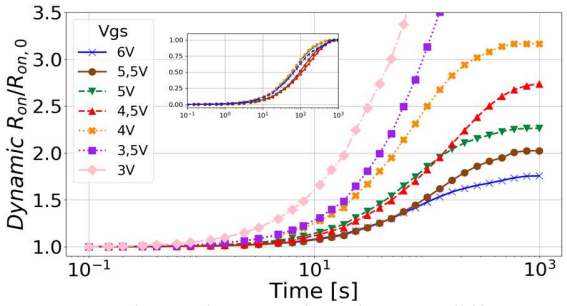

Fig. 13 Dynamic R_{ON} in term of $R_{ON}/R_{ON,0}$ at different V_{GS}. We can notice that at higher V_{GS} the degradation is reduced. In the insert the normalize dynamic is shown and all the curves exhibit a similar behavior.

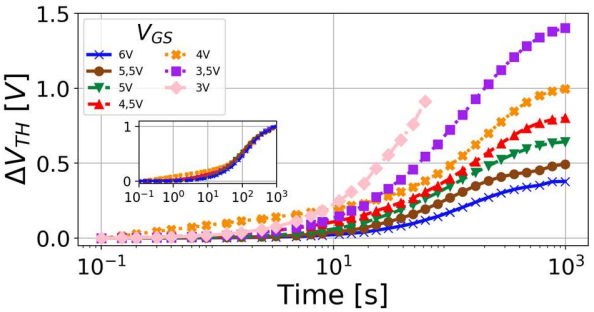

Fig. 14 V_{TH} drift at different V_{GS}. We can notice that at higher V_{GS} the degradation is reduced. In the insert the normalize dynamic is shown and all the curves exhibit a similar dynamic behavior. When the V_{GS} goes below 3 V, the device cannot be turned-on.

During the OFF-state stress experiment, source and body contacts were all tied to ground, while the gate was periodically switched on to measure R_{ON}. During the ON-state stress experiment, the gate was kept fixed at 6 V while the body was tied to the negative pin of the DC/DC converter. In both cases the stress is applied for a cumulative time of 1000 s.

Results are shown in Fig. 10 (symbols) in terms of normalized R_{ON} ($R_{ON}/R_{ON,0}$) where $R_{ON,0}$ is the first acquisition. During OFF-state stress, degradation suffered from R_{ON} is 36%, while during the ON-state stress is significantly higher, around 80%. The dynamic of the process is similar to that of results obtained in Fig. 6, indicating that the configuration does not affect the mechanisms at play. This means that these experiments can be used as a proxy to more conveniently understand (through the comparison with simulations) the mechanism occurring in the LS and HS configurations. In fact, the former is affected only by degradation occurring due to OFF-state stress, whereas the latter is affected also by ON-state stress. Therefore, we will consider results obtained with OFF- and ON-state stress experiments as being representative of the ones obtained in Fig. 5(a) and (b), respectively.

Simulation results are also reported in Fig. 10 (lines), showing an overall agreement with experiments from a qualitative perspective. This agreement indicates that the main responsible for dynamic R_{ON} during OFF-state stress is the hole redistribution occurring in the buffer after being emitted by C-related acceptor traps [26]. The emission of holes from traps near the channel/buffer interface causes an increase of negatively trapped charge in the buffer, thus reducing 2-DEG concentration and hence causing R_{ON} to increase. During ON-state stress instead, we attribute the increased dynamic R_{ON} (with respect to OFF-state stress) to the concurring effects of hole emission from C-related traps and back-gating from the substrate.

As observed in [26], stress from the substrate terminal (i.e., V_{SB} > 0 V) leads to similar effects to OFF-state stress conditions. The enhanced dynamic R_{ON} in ON-state stress conditions thus comes from the higher sensitivity of 2-DEG on ionized buffer traps due to the back-gating effect.

Interestingly, simulations provide an additional insight: the back-gating effect is partially counterbalanced by gate leakage current. In fact, during ON-state the reversely biased Schottky junction between the gate metal and p-GaN layer injects holes into the device due to leakage [37]. Upon reaching the buffer (attracted by the negative potential applied on the substrate), the injected holes partially neutralize the acceptor traps in the buffer (i.e., they get trapped by C-related acceptors) and thus

partially counteract the back-gating effect. This can be appreciated with the aid of Fig. 11, that shows the simulated dynamic R_{ON} with different effective hole tunneling mass ($m_{t,h}$) at the Schottky junction, a parameter that modulates the gate leakage current, i.e., higher $m_{t,h}$ corresponds to lower gate leakage. The lower the gate leakage the higher dynamic R_{ON} because of reduced compensation of negative charge in the buffer by holes injected from the gate. Fig. 12 shows the profile of ionized acceptors in the buffer in the (a) OFF-state, (b) ON-sate with finite gate leakage current and (c) with no gate leakage current (as limiting case). Comparison of (b) and (c) clearly indicates the difference in concentration of ionized traps when gate leakage current model is activated or not. Similar beneficial effects of the gate leakage current on current collapse were observed in [12] on p-GaN HEMTs with gate Ohmic contact, further supporting the interpretation provided here.

Finally, we investigated the role of gate leakage current with experiments by performing again R_{ON} and V_{TH} experiments with reduced gate voltage during the ON-state. The same configuration used to obtain Fig. 10 (i.e., ON-stress conditions) was employed. The motivation behind lowering the gate voltage is simply that it reduces the gate leakage current. Thus, for lower V_{GS} an increase in both dynamic R_{ON} and V_{TH} shift is expected. Fig. 13 and 14 show the results of these experiments in terms of dynamic R_{ON} and V_{TH} shift, respectively. V_{GS} was reduced from 6 V in steps of 0.5 V down to 3 V. Further lowering V_{GS} would cause the device to turn partially OFF during the experiments thus making it impossible to evaluate either R_{ON} or V_{TH}.

Fig. 13 shows that lowering V_{GS} causes an evident increase of dynamic R_{ON} due to reduction in hole leakage current to counteract the back-gating effect. For V_{GS} < 4 V, the drastic increase of dynamic R_{ON} is due to the reduced overdrive caused by V_{TH} increase, that moves the operating point of the device towards a semi-OFF condition. V_{TH} shift shown in Fig. 14 also increases with lower V_{GS}, providing further evidence of the role of gate leakage current on the observed results. The curve taken at V_{GS} = 3 V is incomplete because in these conditions the overdrive reduced down to a point at which current could not be measured dependably anymore (because the device switched partially OFF, as explained earlier). Notice that reducing V_{GS} does not affect the dynamics of parametric degradation, as indicated by the insets in Fig. 13 and 14 that show the normalized R_{ON} $[(R_{ON}/R_{ON,0}–1)/(R_{ON,1000\ s}/R_{ON,0}–1)]$ and V_{TH} $[(V_{TH}–V_{TH,0})/(V_{TH,1000s}–V_{TH,0})]$. This normalization allows a direct comparison of the transient behavior between the different $V_{GS,ON}$ by bringing all curves in the same dynamic range.

V. Conclusions

In this paper, we investigated the dynamic on-resistance (R_{ON}) and threshold voltage (V_{TH}) shifts in on-wafer 100-V p-GaN HEMTs, using a custom experimental setup designed to perform dynamic transients for R_{ON} and V_{TH} measurements, emulating conditions experienced by devices monolithically integrated in switching circuits. Specifically, we developed a circuit to reproduce the switching conditions up to 100 kHz of devices in the Low- (LS) and High-side (HS) of an half-bridge configuration. Because of the sharing of the substrate terminal by these devices, the degradation mechanism of devices in LS and HS configuration differs. We found this difference to cause only a higher degree of degradation (in terms of both R_{ON} and V_{TH}) on the S device with respect to the LS one. Instead, the dynamics of the processes is not influenced by the configuration of the device, establishing that a common mechanism is causing the degradation. This mechanism is the increased negatively charged trap concentration related to C-doping in the buffer, identified with the aid of numerical simulations. The higher degradation observed in the HS case is attributed to the finite source-to-body voltage, that causes a back-gating effect for which the device experiences degradation even during the ON state. Finally, both simulations and experiments indicated the counter-balancing role of the gate leakage current against the back-gating effect during ON-state, that reduces the accumulation of negative charge in the buffer, thereby limiting R_{ON} and V_{TH} increase.

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