



Article

Device Design Implications on $R_{ON} \times Q_{OSS}$ FOM in p-GaN Power HEMTs: A Simulation Study

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Abstract

In this paper, we analyze by means of numerical simulations the device design implications on the $R_{ON} \times Q_{OSS}$ Figure of Merit (FOM) in p-GaN power HEMTs to be employed in soft-switching converters. During switching, p-GaN power HEMTs experience dynamic R_{ON} increase but also dynamic Q_{OSS} reduction, effectively establishing a trade-off between the two device parameters. This trade-off stems from the physical mechanism of hole redistribution within the C-doped buffer. Device design choices such as field plate length, channel and buffer thickness as well as C-doping concentration influence both parameters; however, the relative variation of the two parameters is not necessarily symmetric. Simulations are therefore carried out to identify the best device design choices depending on the target trade-off between R_{ON} and Q_{OSS} .

Keywords: p-GaN HEMT; dynamic R_{ON} ; dynamic Q_{OSS} ; $R_{ON} \times Q_{OSS}$; C-doping; hole redistribution model; TCAD simulations; resonant converter; efficiency

1. Introduction

Gallium Nitride (GaN) has established its presence among wide-band-gap semiconductors for applications mainly in the power electronics and RF domains [1–3]. The advantages of GaN-based devices over other material systems stem from its excellent intrinsic material properties but also from the High Electron Mobility Transistor (HEMT) structure, which effectively enables high-voltage and high-frequency operation. From a device point of view, GaN-based HEMTs offer both low conduction losses (i.e., low R_{ON}) and low switching losses (i.e., low Q_G), with E-mode p-GaN HEMTs having the best $R_{ON} \times Q_G$ figure of merit amongst commercial devices [4]. Notwithstanding these merits, GaN-based devices suffer from significant dispersion effects related to trapping that affect their stability and reliability during operation [5]. One of the primary sources for dispersion is the traps in the buffer introduced by C-doping in the buffer [1], which are energetically located at about 0.9 eV above the GaN valence band [6]. The cause of dispersion is essentially the exchange of holes with the valence band, a process which exhibits a long time constant, typically in the order of tens of seconds at $T = 30^\circ\text{C}$ [1,6,7]. The emission and redistribution of holes within the buffer modulate the number of ionized traps in the buffer itself, in turn modulating the two-dimensional electron gas (2DEG) concentration and therefore affecting the ON-state resistance (R_{ON}) [6]. Recently, we showed how the hole redistribution in the buffer also modulates the output charge ($Q_{OSS} = Q_{GD} + Q_{DS}$) as this quantity also depends



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on 2DEG concentration (i.e., the non-linear, non-constant output capacitance $C_{OSS} = C_{GD} + C_{DS}$ varies if 2DEG varies) [8,9]. The correlation between dynamic R_{ON} and Q_{OSS} was first attributed to C-related traps in the buffer by the experimental study of Cioni et al. [8]. In the study, a simultaneous on-the-fly characterization of the two parameters was performed under switching conditions at 200 V. It was shown how dynamic R_{ON} increased with time while dynamic Q_{OSS} decreased, and more specifically it was observed how the variation of the two parameters followed an exponential evolution over time with approximately equal time constants in a wide temperature range from 25 to 150 °C. This behavior was reproduced with numerical simulations in our previous work, where it was shown how both dynamic R_{ON} increase and dynamic Q_{OSS} decrease could be explained with the hole redistribution model [9]. Figure 1 summarizes these findings by showing how the activation energy (E_A) of dynamic R_{ON} (Q_{OSS}) increase (decrease) is 0.81 eV, which correlates with the C-related trap energy level (0.9 eV). Dynamic R_{ON} and Q_{OSS} are defined as relative values with respect to the value prior to stress, i.e., dynamic $R_{ON} = R_{ON}(t)/R_{ON}(0)$, dynamic $Q_{OSS} = Q_{OSS}(t)/Q_{OSS}(0)$.

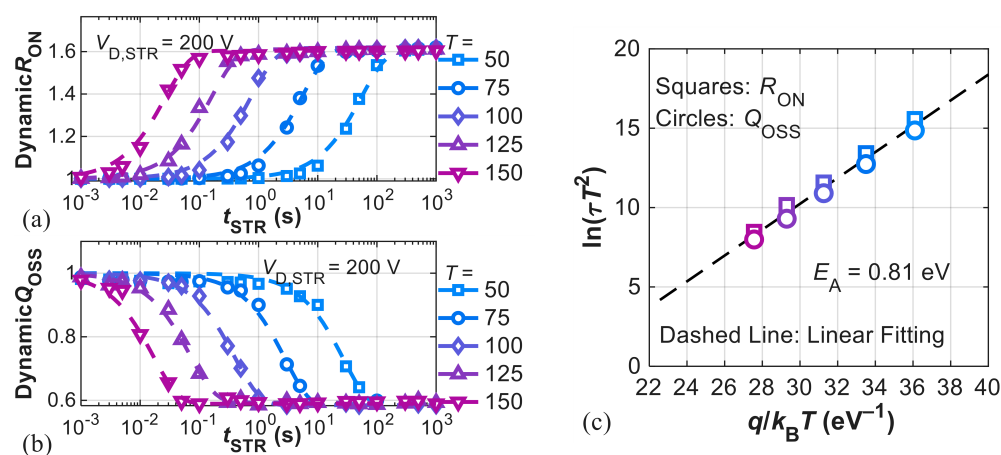


Figure 1. Dynamic (a) R_{ON} and (b) Q_{OSS} transients. Simulations were carried out at $V_{D,STR} = 200$ V at different temperatures, $T = 50$ – 150 °C ($\Delta T = 25$ °C). Dashed lines are the stretched-exponential fitting curves of the data. (c) Arrhenius plot extracted from the dynamic R_{ON} and Q_{OSS} transients. The dashed line is the linear fitting of the data, from which an $E_A = 0.81$ eV was extracted in both cases, correlating with the C_N trap level (0.9 eV).

In this work, we build upon the findings of [9] to show the effects of different design choices on the relative trade-off between R_{ON} and Q_{OSS} . Therefore, while the conference paper in ref. [9] focuses on clarifying the physical mechanism behind dynamic R_{ON} and Q_{OSS} correlation, namely the hole redistribution due to C-related traps, here the focus is on the design implications on the trade-off mentioned above, and on the possible strategies to minimize the FOM $R_{ON} \times Q_{OSS}$, as discussed in the following.

We employ numerical simulations to show the sensitivity of both R_{ON} and Q_{OSS} on channel, barrier, and buffer thickness, carbon concentration, field plate(s) length, and passivation(s) thickness. Here, we focus on $Q_{OSS} = Q_{GD} + Q_{DS}$ rather than Q_G (or Q_{GD} only) because in soft-switching converters Q_{OSS} is more detrimental to losses than Q_G , especially at high voltage ratings [10], and switching losses are almost absent (conversely, in hard-switching conditions, Q_{GD} is the limiting factor). More specifically, in soft-switching and resonant converters, switching losses are almost completely removed by including a dead-time interval during the period to ensure zero-voltage switching (ZVS) conditions. However, longer dead-time duration leads to higher conduction losses as the RMS current needed to transfer power to the output has to increase if the duty cycle reduces [10]. Dead-time duration is limited by Q_{OSS} (i.e., it corresponds to the time taken to discharge the

non-linear output capacitance C_{OSS}), since the transistor drain-to-source voltage needs to be brought to zero volts in order to have ZVS. Therefore, design of GaN HEMTs for power converters working in soft-switching conditions should aim to minimize $R_{ON} \times Q_{OSS}$ [10–12].

2. Simulation Setup

In this section we describe the numerical simulation setup in terms of device structure, models, and main simulation parameters. The structure is shown in Figure 2, which resembles a typical p-GaN HEMT for power applications. Note in particular the three separate field plates used to shield the drain edge of the gate terminal from large electric field peaks [13]. Note that field plate 1 is connected to the gate terminal, whereas field plates 2 and 3 are connected to the source terminal. The drain overhang is used to reduce the electric field peak at the drain terminal occurring at very large reverse voltages. Consistent with the structure in [7], which served as a template for the simulated device, the substrate was realized out of conductive p-type silicon, which is short-circuited to the source and thus grounded to the reference potential (0 V).

The numerical model is described as follows. The 2D numerical device simulations were carried out with the SDevice simulator (Synopsys Inc., Sunnyvale, CA, USA). Drift-diffusion was the model used to account for charge transport. Mobility was set to $1800 \text{ cm}^2/\text{Vs}$ in the 2DEG, exponentially decaying with temperature. Piezoelectric polarization charge was included at the AlGaN/GaN interface by using the default strain model of the simulator, leading to a 2DEG concentration of $\approx 7 \times 10^{12} \text{ cm}^{-2}$. Note that at the passivation/barrier interface, the polarization model was deactivated (i.e., we assumed that the negative polarization charge at this interface is completely compensated by an equal positive surface charge). Incomplete ionization of Mg-related acceptors in the p-GaN gate region was included in the model (the Mg ionization energy was set to 0.16 eV above the GaN valence band edge). Gate leakage was accounted for through hole tunneling across the Schottky junction formed by the gate metal contact and the p-GaN region. Source and drain contacts were modeled as Schottky junctions, with a similar approach to that discussed in [14]. Impact ionization was modeled with Chynoweth’s law. To model the vertical leakage conduction through the substrate and nucleation layers, we employed a similar strategy to that discussed in [15]. Dynamic effects related to C-doping traps were accounted for by adding one Shockley–Read–Hall (SRH) trap-balance equation for each distinct trap. Carbon doping in the GaN buffer was modeled by considering two different trap levels: a dominant deep acceptor trap at $E_V + 0.9 \text{ eV}$ and a shallow donor trap at $E_C - 0.11 \text{ eV}$. The nominal trap concentrations were 4.3×10^{17} and $4 \times 10^{17} \text{ cm}^{-3}$ for C-related acceptors and donors, respectively. This corresponds to an effective acceptor density ($N_{C, \text{Eff}}$) of $3 \times 10^{16} \text{ cm}^{-3}$. This particular choice is in line with what was done in ref. [7] to have a quantitative agreement with experimental results regarding dynamic R_{ON} . Table 1 collects the relevant parameter values used for the reference device.

Table 1. Relevant parameter values used in the simulations for the reference device.

Parameter	Symbol	Value
Channel thickness	t_{Chan}	0.3 μm
Barrier thickness	t_{Bar}	12 nm
Buffer thickness	t_{Buf}	4.7 μm
Field plate 1 length	$L_{\text{FP},1}$	3 μm
Field plate 2 length	$L_{\text{FP},2}$	10 μm
Field plate 3 length	$L_{\text{FP},3}$	15 μm

Table 1. Cont.

Parameter	Symbol	Value
Passivation 1 thickness	$t_{\text{Pas},1}$	0.25 μm
Passivation 2 thickness	$t_{\text{Pas},2}$	0.25 μm
Passivation 3 thickness	$t_{\text{Pas},3}$	1 μm
Effective C-related trap concentration	$N_{\text{C,Eff}}$	$3 \times 10^{16} \text{ cm}^{-3}$
2DEG mobility	$\mu_{\text{n,2DEG}}$	1800 cm^2/Vs
2DEG concentration	n_{2DEG}	$7 \times 10^{12} \text{ cm}^{-2}$

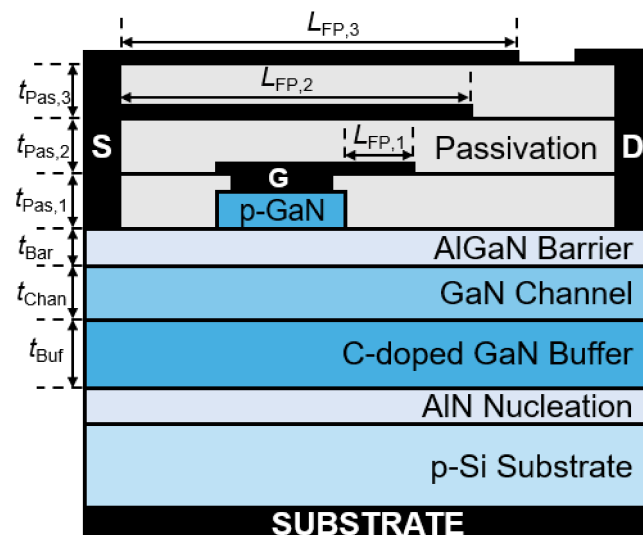


Figure 2. Cross-section of the simulated 2D device. The geometrical parameters subject to variation in the analysis are indicated.

3. Numerical Simulation Results

The results described in the following are obtained from numerical simulations that mimicked the experimental conditions used in [8] to characterize dynamic R_{ON} and Q_{OSS} . The simulated experiment consisted of the OFF-state stress condition applied for 1000 s, after which R_{ON} and Q_{OSS} were evaluated. R_{ON} was probed by switching the device ON (i.e., $V_{\text{GS}} = 6 \text{ V}$, $V_{\text{DS}} = 1 \text{ V}$) for 5 μs . Q_{OSS} was instead probed by switching V_{DS} from the stress value to 0 V within a 25 μs time window, during which Q_{OSS} was obtained by integrating I_{D} over time. Specifically,

$$Q_{\text{OSS}} = \int_{t(V_{\text{DS}}=V_{\text{DS,STR}})}^{t(V_{\text{DS}}=0)} I_{\text{D}}(t) dt$$

The Q_{OSS} thus defined represents the total output charge. Because the Q_{OSS} is taken while the output capacitance discharges, the sign of the current I_{D} is negative (and thus also Q_{OSS}); therefore, the absolute value is taken.

Figure 3 shows a sketch of the waveforms employed in the simulations to assess R_{ON} and Q_{OSS} during the simulated experiments. The on-pulse duration of 5 μs to monitor R_{ON} and the 25 μs -long ramp to bring V_{DS} from $V_{\text{DS,STR}}$ to 0 V were set in agreement with the experimental setup defined in [8]. While the on-pulse duration is exactly the same as that in [8], the ramp duration agrees with the typical ramp duration in the experiments, which, however, is not defined *a priori*, because the drain potential is set by an external generator through a series resistance which is used to monitor the current during the switch-OFF. In the simulations, however, the drain potential is set directly; therefore, the ramp duration is given as an input. Nonetheless, neither the on-pulse nor the ramp time influences the

R_{ON} and Q_{OSS} probing as long as their duration is well below the time constant of the hole emission process which defines the trap charge state (at $T = 30\text{ }^{\circ}\text{C}$, the time constant is typically in the order of tens of seconds; therefore, this requirement is satisfied by the waveform durations set in the simulations). Stress duration of 1000 s was set in agreement with experimental conditions used in [8].

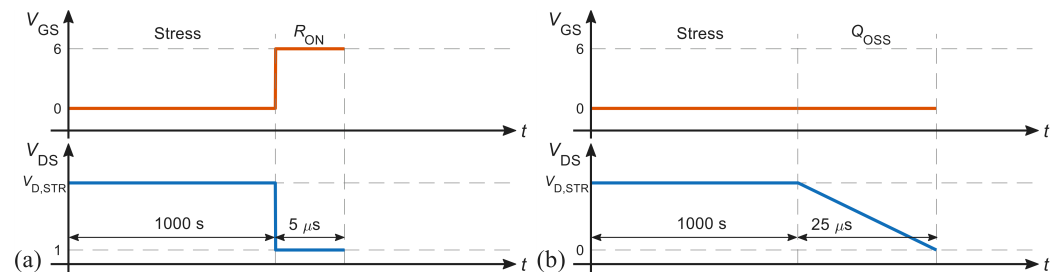


Figure 3. Sketch of V_{GS} and V_{DS} waveforms applied during simulations to extract (a) R_{ON} and (b) Q_{OSS} after stress. After application of OFF-state stress conditions for 1000 s, (a) assessment of R_{ON} is carried out in the ON-state for 5 μs , and (b) assessment of Q_{OSS} is carried out during switching of V_{DS} to 0 V for 25 μs . The time diagrams are not to scale and are for illustration only.

R_{ON} and Q_{OSS} were also evaluated after applying stress only for 10 μs in order to compare the $R_{ON} \times Q_{OSS}$ with commercial devices. We refer to the values extracted in this way as ‘prior to stress’, since C-related traps are well known to cause negligible dispersion effects at such short time scales at $T = 30\text{ }^{\circ}\text{C}$, see for instance [6,7]. Therefore, R_{ON} and Q_{OSS} extracted in this way are only affected by the electrostatics of the device and not by dynamic effects associated with traps.

Table 2 shows the comparison with state-of-the-art GaN HEMTs rated at 650 V. In the simulations, R_{ON} is extracted at $V_{GS} = 6\text{ V}$, $V_{DS} = 1\text{ V}$. Q_{OSS} is extracted instead at $V_{GS} = 0\text{ V}$, $V_{DS} = 400\text{ V}$. The $R_{ON} \times Q_{OSS}$ extracted from the simulations is in the range of reported commercial technologies, providing a useful benchmark for the simulated device. Notice that the simulated device has a width of 1 mm; therefore, to make the simulated R_{ON} value comparable with those of commercial devices, a scaling factor of 200 (commercial devices have widths as large as hundreds or thousands of mm) was used to divide R_{ON} ; Q_{OSS} was then obtained by multiplying by the same factor of 200. Nevertheless, $R_{ON} \times Q_{OSS}$ remains unaffected by scaling.

The nominal breakdown voltage (V_{BR}) of the simulated device is 877 V. However, generally commercial devices are de-rated with respect to their actual V_{BR} for reliability concerns; therefore, the simulated device should be considered as a 26% de-rated 650 V device. Even so, the comparison with commercial technology is intended as a technology benchmark for $R_{ON} \times Q_{OSS}$ rather than a direct device-to-device comparison.

Table 2. Comparison of $R_{ON} \times Q_{OSS}$ of different commercial devices (values obtained from datasheets of vendors) rated for 650 V. The value extracted from the simulated device is in line with the state of the art.

Device	R_{ON} (m Ω)	Q_{OSS} (nC)	$R_{ON} \times Q_{OSS}$ (n Ω C)
GAN041-650WSB (Nexperia)	35	150	5.25
SGT070R70HTO (ST) *	53	94.7	5.02
GS66516T (GaN System, now Infineon)	25	134	3.35
NTBL050N65GN1 (onsemi)	39	107	4.17
INN650D080BS (Innoscence)	80	60	4.8

Table 2. Cont.

Device	R_{ON} (m Ω)	Q_{OSS} (nC)	$R_{ON} \times Q_{OSS}$ (n Ω C)
TP65H050G4WS (Renesas)	50	120	6.0
IGLT65R055D2 (Infineon)	55	35	1.9
Simulated Device **	63.3 (12.66 Ω mm)	40.4 (0.202 nC/mm)	2.55

* Rated at 700 V. ** Width of simulated device is 1 mm; therefore, to make simulated R_{ON} and Q_{OSS} values comparable with those of commercial devices, a scaling factor of 200 was used ($R_{ON} \times Q_{OSS}$ remains unaffected).

3.1. Results After 1000-s Stress

Results of the sensitivity analysis are presented in Figure 4. Each panel shows the dependence of R_{ON} , Q_{OSS} , and $R_{ON} \times Q_{OSS}$ on a single geometric parameter (all the others were kept fixed at their nominal value, reported in Table 1). The values are normalized to that of the reference device for a more immediate comparison. The values reported in Figure 4 are those taken at the end of the stress experiment illustrated in Figure 3 (the values prior to the stress experiment are reported in Section 3.2).

Figure 4a shows the effect of channel thickness (t_{Chan}) variation: t_{Chan} increase moves the C-related traps away from the 2DEG, thereby reducing their influence on the channel electrons, hence R_{ON} decreases and at the same time Q_{OSS} increases. This leads to an almost constant $R_{ON} \times Q_{OSS}$ (it decreases by about 3%). By the same token, a thinner t_{Chan} increases R_{ON} and decreases Q_{OSS} as the C-related traps are more effective in reducing the 2DEG concentration. Again, reducing t_{Chan} leads to an almost constant $R_{ON} \times Q_{OSS}$, as the decrease in Q_{OSS} is almost completely mirrored by an R_{ON} increase.

Figure 4b shows that barrier thickness (t_{Bar}) increase only negligibly affects R_{ON} and Q_{OSS} , while its reduction causes R_{ON} to slightly increase, therefore leading to a small $R_{ON} \times Q_{OSS}$ increase of about 5% with a 50% reduction of t_{Bar} . The fact that R_{ON} increases also prior to stress as shown in Figure 6b indicates that the increase due to t_{Bar} reduction is caused by an electrostatic effect (barrier thickness reduction causes a decrease in 2DEG concentration, due to a larger difference between the conduction band and the Fermi level at a given bias [1]).

Interestingly, Figure 4c shows that both R_{ON} and Q_{OSS} vary significantly with buffer thickness (t_{Buf}). When t_{Buf} decreases, R_{ON} is reduced because for a given trap concentration the number of traps that become negatively charged is lower (because the volume is lower); therefore, the modulation of 2DEG by traps in the buffer is weaker and R_{ON} reduces. Opposite considerations apply when t_{Buf} increases. Regarding Q_{OSS} , on top of the previous considerations about the variation of buffer traps, t_{Buf} reduction also increases Q_{OSS} ; therefore, an additional increase of Q_{OSS} is observed; t_{Buf} increase instead reduces Q_{OSS} by about 20%. The effect of t_{Buf} on Q_{OSS} due to C_{OSS} modulation can be inferred from Figure 6c, which again shows results prior to stress (and thus allows one to appreciate the electrostatic contribution to the parameter variation). Overall, decreasing t_{Buf} causes an $R_{ON} \times Q_{OSS}$ reduction of less than 10%; on the other hand, $R_{ON} \times Q_{OSS}$ increases with increasing t_{Buf} up to almost 50% for a 100% t_{Buf} increase. Therefore, while reducing t_{Buf} might be beneficial to reduce R_{ON} , increasing it leads to an overall penalty in device performance, because R_{ON} increase is more severe than Q_{OSS} reduction.

Figure 4d–f show the sensitivity on the length of the three field plates present in the structure (see Figure 2). Figure 4d shows that field plate 1 length ($L_{FP,1}$) variations cause negligible variation of both R_{ON} and Q_{OSS} . The slight R_{ON} reduction (Q_{OSS} increase) with increasing $L_{FP,1}$ is attributed to the fact that a longer field plate increases the shielding effect of the ground bias (applied on the gate terminal in the OFF-state) against electric field peaks, thereby reducing the effect of trapped charge in the regions below the field

plate itself. However, these variations are within 3% of the reference value, so little gain is to be expected from increasing $L_{FP,1}$. Instead, when considering variations of field plate 2 length ($L_{FP,2}$) as shown in Figure 4e, we can observe a more complex picture. Within $\pm 50\%$ $L_{FP,2}$ variations, R_{ON} and Q_{OSS} vary symmetrically and by almost the same amount, as indicated by the fact that $R_{ON} \times Q_{OSS}$ remains almost constant. However, increasing $L_{FP,2}$ by 100% causes R_{ON} and Q_{OSS} to vary more considerably. While R_{ON} reduction is explained by the shielding effect discussed before for $L_{FP,1}$, the considerable Q_{OSS} increase is mainly due to the increased coupling between the source and drain terminals, which increases C_{DS} (recall that this field plate is connected to the source terminal, see Figure 2). We conclude therefore that the effect of capacitive coupling between source and drain is more relevant to Q_{OSS} variation than the electric field shielding effect, as confirmed by the fact that $R_{ON} \times Q_{OSS}$ increases. Again, the electrostatic increase of C_{DS} inducing Q_{OSS} increase can be appreciated from the results prior to stress, see Figure 6e. The effect of $L_{FP,3}$ variations leads to similar results to those of the other field plates, as shown in Figure 4f. In this case, we also observe how $R_{ON} \times Q_{OSS}$ remains almost constant ($L_{FP,3}$ was not increased by more than 50% because further increase would cause an overlap of field plate 3 with the drain overhang shown in Figure 2).

As a general remark, we observe how field plates should be designed keeping in mind two constraints: on the one hand, field plates provide the beneficial effect of shielding from electric field peaks in the off-state; on the other hand, they increase the gate–drain and source–drain coupling (i.e., C_{GD} and C_{DS}), which affect dynamic performance. Therefore, design of field plates is constrained by this trade-off, and depending on the target application either reducing or increasing field plate length might be more beneficial. Still, these considerations mostly apply to field plates 2 and 3, since field plate 1 is significantly shorter than the other ones, and much closer to the active region, therefore acting more as an electric field shield than anything else.

Concerning the modulation of the passivation thicknesses ($t_{Pas,1}$ – $t_{Pas,3}$), Figure 4g–i show that both R_{ON} and Q_{OSS} variations are limited. Therefore, no significant advantage can be obtained from the variation of passivation thickness (provided that leakage is kept under control).

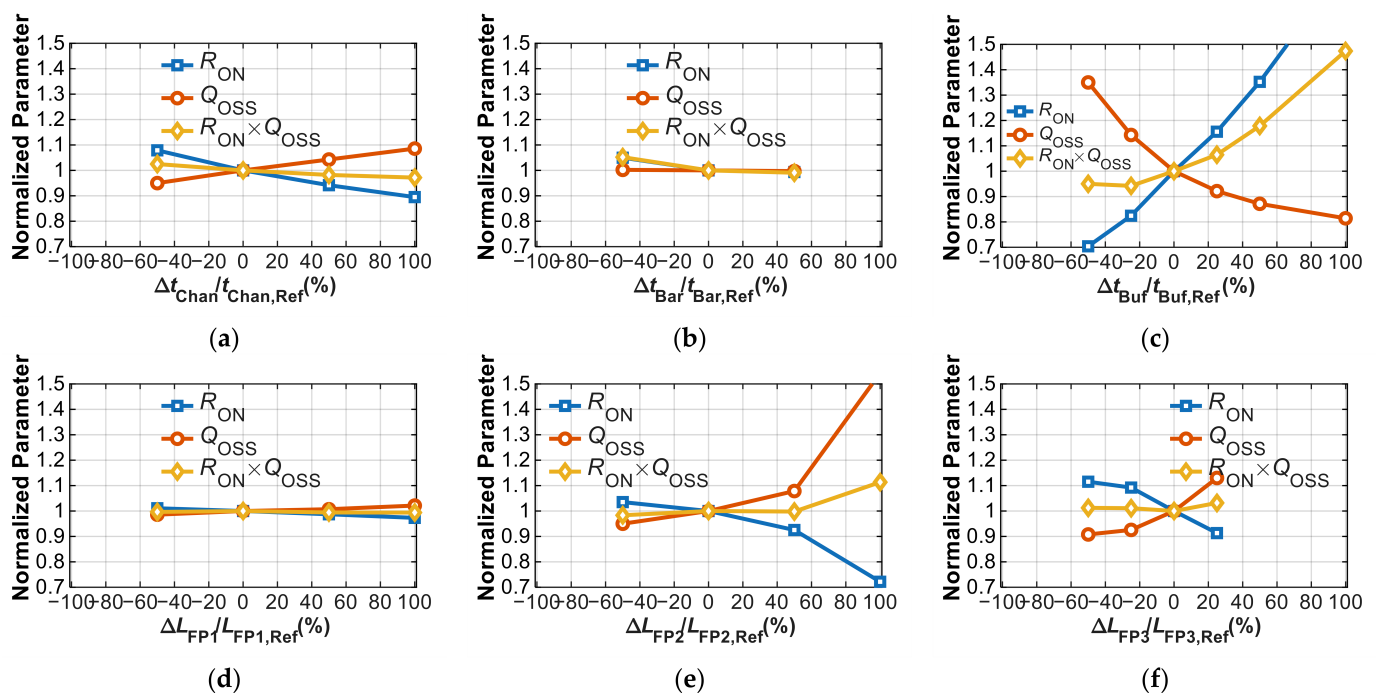


Figure 4. Cont.

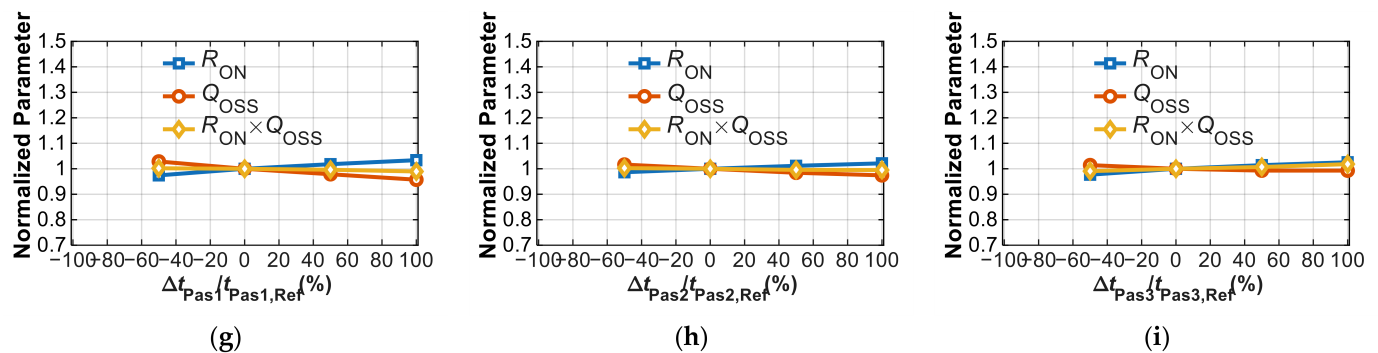


Figure 4. Sensitivity of R_{ON} , Q_{OSS} , and $R_{ON} \times Q_{OSS}$ on variation of geometric parameters: (a) channel thickness, t_{Chan} ; (b) barrier thickness, t_{Bar} ; (c) buffer thickness, t_{Buf} ; (d) field plate 1 length ($L_{FP,1}$); (e) field plate 2 length ($L_{FP,2}$); (f) field plate 3 length ($L_{FP,3}$); (g) passivation 1 thickness, $t_{Pas,1}$; (h) passivation 2 thickness, $t_{Pas,2}$; (i) passivation 3 thickness, $t_{Pas,3}$. Parameters were evaluated at the end of the stress phase, with $V_{D,STR} = 400$ V applied for 1000 s at $T = 30$ °C.

Another important parameter that causes significant variation on R_{ON} and Q_{OSS} is the concentration of C-related traps in the buffer ($N_{C,Eff}$). Variation of $N_{C,Eff}$ is shown in Figure 5. An increase (decrease) in effective trap concentration increases (decreases) R_{ON} and decreases (increases) Q_{OSS} ; these results are expected since C-related traps affect both R_{ON} and Q_{OSS} as established in [8,9]. We notice how $R_{ON} \times Q_{OSS}$ follows $N_{C,Eff}$ variations; therefore, it would be advisable to reduce $N_{C,Eff}$ as much as possible, provided that requirements on leakage and breakdown voltage are satisfied. We would like to point out that the picture above holds true as long as the increase in effective acceptor trap concentration occurs with increasing C-doping concentration. This might not hold true for very high C-doping concentration (i.e., higher than 10^{19} cm⁻³) for which the compensation by donors might also increase, overall leading to a reduced effective acceptor trap concentration [16].

Results in Figures 4 and 5 were obtained at $T = 30$ °C and for a single $V_{D,STR} = 400$ V. Temperature is known to accelerate dynamic R_{ON} and Q_{OSS} degradation, in the sense that at a given time, variation of both parameters is larger in magnitude compared to the $T = 30$ °C case. However, after 1000 s stress, as can be appreciated from Figure 2, dynamic R_{ON} and Q_{OSS} have reached a steady-state condition; therefore, from a qualitative point of view the trends in Figures 4 and 5 are expected to remain unaffected by temperature. Regarding $V_{D,STR}$ variation, the picture is more complex as one has to consider that both dynamic R_{ON} and Q_{OSS} vary non-monotonically with $V_{D,STR}$, as reported in [8,9]. Therefore, the choice of $V_{D,STR}$ will change the magnitude of degradation of both parameters, but not the qualitative behavior.

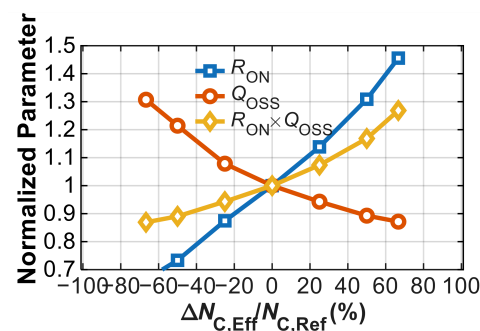


Figure 5. Sensitivity of R_{ON} , Q_{OSS} , and $R_{ON} \times Q_{OSS}$ on variation of effective C-doping-related traps in the buffer ($N_{C,Eff}$). $V_{D,STR} = 400$ V at $T = 30$ °C. Parameters were evaluated at the end of the stress phase.

Results in Figures 4 and 5 are obtained with the substrate grounded. The expected impact of having a floating substrate is to exacerbate the magnitude of dynamic R_{ON} (and consequently Q_{OSS}), as suggested in [17]. Having the substrate grounded, the device configuration in this work resembles that of a low-side device in a half-bridge configuration. While not specifically addressed in this work, in the case of monolithic integration of a half-bridge on a single substrate, the high-side device is expected to experience worse degradation in magnitude compared to the low-side one [18,19].

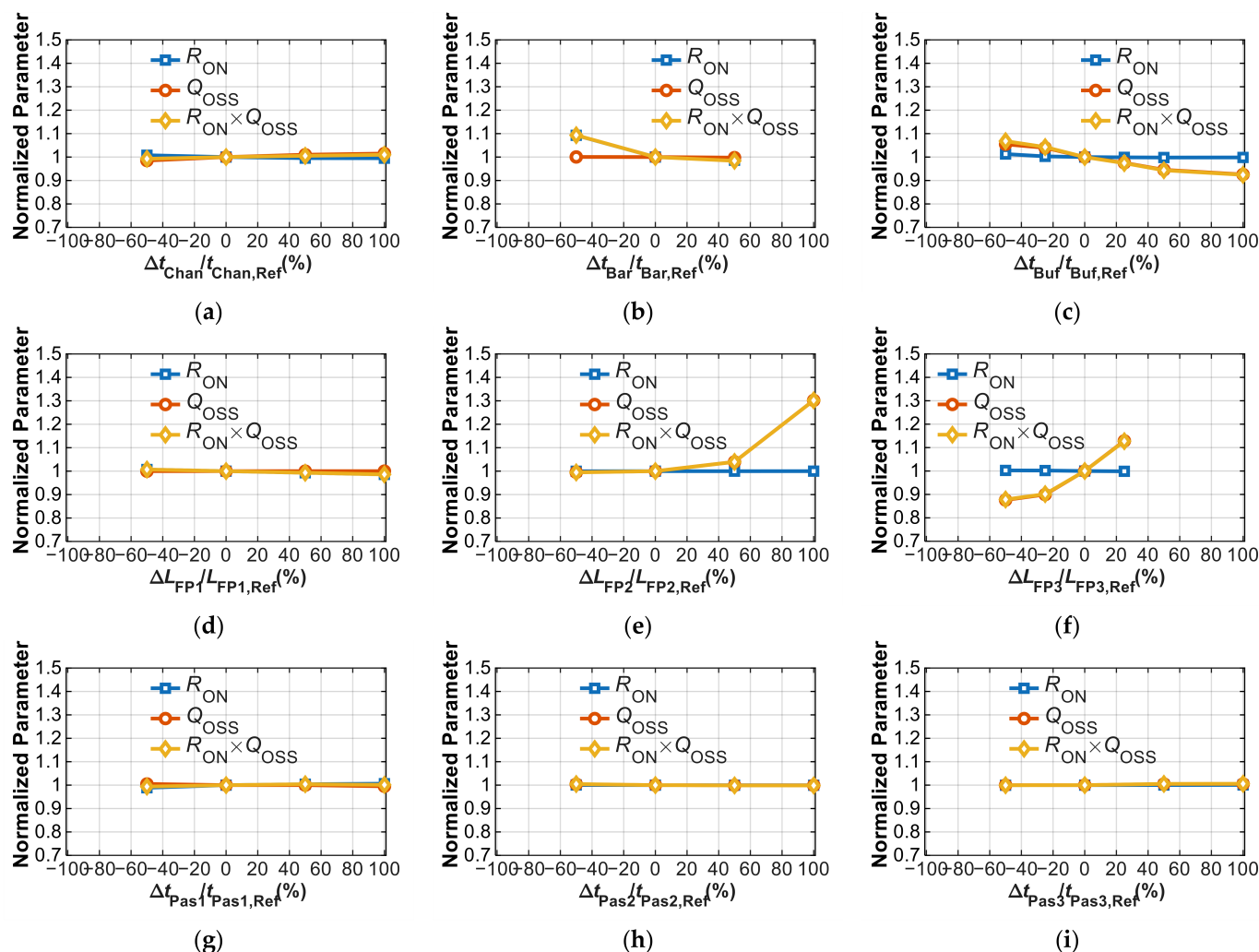


Figure 6. Sensitivity of R_{ON} , Q_{OSS} , and $R_{ON} \times Q_{OSS}$ on variation of geometric parameters: (a) channel thickness, t_{Ch} ; (b) barrier thickness, t_{Bar} ; (c) buffer thickness, t_{Buf} ; (d) field plate 1 length (L_{FP1}); (e) field plate 2 length (L_{FP2}); (f) field plate 3 length (L_{FP3}); (g) passivation 1 thickness, $t_{Pas,1}$; (h) passivation 2 thickness, $t_{Pas,2}$; (i) passivation 3 thickness, $t_{Pas,3}$. Parameters were evaluated prior to the stress phase at $T = 30^\circ\text{C}$.

3.2. Results Prior to Stress

Figure 6 reports the simulation results of the sensitivity analysis on R_{ON} and Q_{OSS} obtained prior to the stress test (i.e., as specified in Section 2, these results are obtained after applying stress for 10 μs , which is short enough not to induce any measurable effect of dynamic R_{ON} and Q_{OSS} at $T = 30^\circ\text{C}$). This data complements the one shown in Figure 4, and the comparison allows assessing the effect of prolonged operation on R_{ON} , Q_{OSS} , and on the $R_{ON} \times Q_{OSS}$ FOM. Generally, we observe from Figure 6 how R_{ON} and Q_{OSS} are much less affected by parameter variations compared to Figure 4. This is attributed to the fact that the effect of C-related traps manifests itself only with the passing of time; therefore,

R_{ON} and Q_{OSS} variations prior to stress (for instance, with t_{Bar} variation) have only to do with the electrostatics of the device, and not with C-related trapping effects. However, in some cases Q_{OSS} variation is significant even prior to stress due to electrostatics, see for instance Figure 6c,e,f. These variations have to do with device capacitance modulation induced by geometric parameter variations.

Lastly, Figure 7 shows the influence on the parameters of $N_{C,Eff}$ variation prior to the stress phase. Interestingly, both R_{ON} and Q_{OSS} remain almost insensitive to variations because the trap time constant is longer than the evaluation time window (i.e., carbon has little effect on R_{ON} and Q_{OSS} prior to stress). In practice, data presented in Figures 4 and 5 are more important to the designer as the device will inevitably incur degradation during operation.

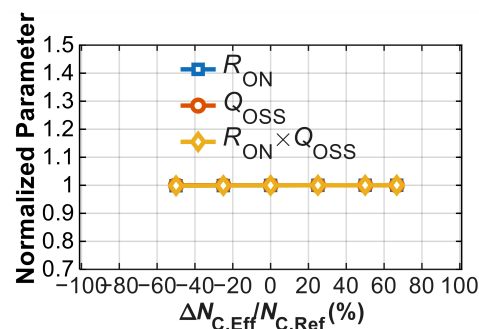


Figure 7. Sensitivity of R_{ON} , Q_{OSS} , and $R_{ON} \times Q_{OSS}$ on variation of effective C-doping-related traps in the buffer ($N_{C,Eff}$). Parameters were evaluated prior to the stress phase at $T = 30^\circ\text{C}$.

3.3. Discussion

From the results obtained so far, we observe that reducing $R_{ON} \times Q_{OSS}$ is possible by increasing channel thickness, decreasing buffer thickness, reducing source-connected field plate length, or reducing effective carbon doping concentration. Table 3 summarizes the variations obtained in terms of R_{ON} , Q_{OSS} , and $R_{ON} \times Q_{OSS}$ when performing the above variations. A comparison of the values obtained after and prior to stress allows one to immediately quantify how much of the variation is due to trapping effects or to electrostatic effects. In Table 3, we add a comparison of the breakdown voltage (V_{BR}) and leakage current ($I_{D,Leak}$) variation obtained with respect to the nominal case for each of the main parameters of interest identified with the previous analysis. V_{BR} was defined as the V_{DS} at which $I_D = 1\text{ mA/mm}$ when $V_{GS} = 0\text{ V}$ (for the nominal case, $V_{BR} = 877\text{ V}$), whereas $I_{D,Leak}$ was taken at $V_{DS} = 650\text{ V}$ (for the nominal case, $I_{D,Leak} = 1.33\text{ nA/mm}$). From Table 3 we can observe how increasing t_{Chan} or L_{FP2} length gives negligible variation in V_{BR} , and reduction of $N_{C,Eff}$ leads to about 5% reduction in V_{BR} . Only when reducing t_{Buf} by 50% does V_{BR} reduce significantly by 39%. Concerning $I_{D,Leak}$ instead, increasing t_{Chan} leads to about 1.44 nA/mm leakage current, whereas reducing L_{FP2} almost leaves $I_{D,Leak}$ unaffected. When decreasing t_{Buf} by 50%, $I_{D,Leak}$ is not defined as the device breaks down below 650 V ; for reduced $N_{C,Eff}$ instead $I_{D,Leak}$ increases by about 26 times to 35.9 nA/mm (this increase is in line with the difference between typical and maximum leakage current of commercial devices listed in Table 2). These indications give a clear picture to a designer of the trade-off between $R_{ON} \times Q_{OSS}$, V_{BR} , and $I_{D,Leak}$ upon critical parameter variations.

Table 3. Summary of R_{ON} , Q_{OSS} , $R_{ON} \times Q_{OSS}$, and V_{BR} variation upon variation of the most critical design parameters obtained from Figures 4 and 5 (values between brackets are those obtained from Figures 6 and 7).

Parameter Variation	R_{ON} Variation	Q_{OSS} Variation	$R_{ON} \times Q_{OSS}$ Variation	V_{BR} Variation	$I_{D,Leak}$ Variation
+100% t_{Chan}	−11% (<1%)	+8.6% (+1.5%)	−3% (+1%)	<1%	+8.3%
−50% t_{Buf}	−30% (+1.3%)	+35% (+5.4%)	−5% (+6.8%)	−39%	N.A. *
−50% $L_{FP,2}$	+3.5% (<1%)	−5% (<1%)	−2% (<1%)	<1%	<1%
−66.7% $N_{C,Eff}$	−33.5% (<1%)	+30.7% (<1%)	−13% (<1%)	−5%	$\times 26$ **

* $I_{D,Leak}$ is not defined because the device breakdown voltage is less than 650 V in this case. ** This increase is in line with the difference between typical and maximum leakage current of commercial devices listed in Table 2.

4. Conclusions

We analyzed by means of numerical simulations the device design implications on the $R_{ON} \times Q_{OSS}$ Figure of Merit (FOM) in p-GaN power HEMTs to be employed in soft-switching converters. R_{ON} and Q_{OSS} are strongly affected by C-related traps in the buffer; hence, device design can significantly affect their values by varying the amount of modulated negative trapped charge in the buffer. The analysis reveals that reducing $R_{ON} \times Q_{OSS}$ is possible by either: increasing channel thickness, decreasing buffer thickness, reducing source-connected field plate length, or reducing effective carbon doping concentration. These indications stem from the investigated device structure and parameter ranges, therefore they should be intended as simulation trends rather than general optimization rules.

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