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Indium-Gallium-Arsenide n-Channel MOSFETs for CMOS Technology Extension Beyond the 16-nm Node

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“Everyone knows that something is impossible to realize until someone arrives who doesn’t …and then invents it”

Albert Einstein

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List of Acronyms

ALD: atomic layer deposition
CMOS: complementary metal oxide semiconductor
CP: charge pumping
DIBL: drain-induced barrier lowering
DOS: density of states
DWB: direct wafer bonding
EOT: equivalent oxide thickness
GIDL: gate-induced drain leakage
HEMT: high-electron mobility transistors
ISSG: in situ steam generated
ITRS: International Technology Roadmap for Semiconductors
MBE: molecular beam epitaxy
MOCVD: metal organic chemical vapor deposition
MOSCAP: metal oxide semiconductor capacitor
MOSFET: metal oxide semiconductor field effect transistor
PDA: post deposition annealing
RIE: reactive ion etch
RTA: rapid thermal annealing
SoC: system-on-chip
SiP: system-in-package
TLM: transmission line model
TSCIS: trap spectroscopy by charge injection and sensing
UID: unintentionally doped

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Chapter I: Introduction

For the last 30 years, Moore's law has been a guiding principle for the semiconductor industry. To sustain the Moore's law a continuous scaling of Si metal oxide semiconductor field effect transistors (MOSFETs) has been required. Nowadays, this era of Si-based MOSFETs scaling is approaching severe physical and technological limitations. As happened with the introduction of high-k/metal gate structures for logic in late 2007, the time for innovation has come also for MOSFET semiconductor material and/or structure.

Extensive research efforts are today devoted to the investigation of alternative materials or devices able to overcome Si limits, thus enabling the scaling of complementary metal oxide semiconductor (CMOS) technology under the 16-nm technology node. A very important role, among the solutions proposed, is played by III-V FET, and in particular by InGaAs MOSFETs. The latter are being the favorite candidates for n-channel Si-MOSFET. This dissertation describes the research on these devices I have been involved in during my Ph.D. at the Ph.D. School in Information and Communication Technology, University of Modena and Reggio Emilia, Italy.

The dissertation is organized as follows.

Chapter II will give a brief overview of Si-CMOS in the last decade, and will introduce future directions for beyond-CMOS technologies. After some considerations on current status and future downscaling of CMOS, the main challenges of the scaling will be discussed. Then, the importance of introducing high-mobility III-V semiconductors to further enhance device performance will be explained. Eventually III-V current technology will be presented with particular relevance to Ge- and InGaAs-based MOSFETs.

Chapter III will address the effects of interface traps in inversion-type InGaAs MOSFETs with ZrO_2 gate dielectric. By means of two-dimensional device simulations reproducing experimental data, I will analyze the interface trap impact on both standard MOSFETs and capped MOSFETs. In the latter a thin $In_{0.2}Ga_{0.8}As$ cap layer is interposed between the gate dielectric and the $In_{0.53}Ga_{0.47}As$ channel to attenuate the interface-related mobility degradation. A detailed analysis of the effects of both acceptor and donor nature of traps will be provided together with the description of the non-trivial behaviour associated with donor-like interface traps in capped MOSFETs.

In **Chapter IV** we will present some guidelines for the future optimization and scaling of InGaAs MOSFETs. The study is carried out using an InGaAs quantum-well MOSFET with Al_2O_3 gate dielectric as a baseline structure. In this device the $In_{0.53}Ga_{0.47}As$ channel is buried in between an InP cap layer and an InAlAs buffer layer creating a quantum well channel structure. The study will be focused on two main aspects: (i) interface-trap influence on device characteristics and, consequently, criteria for optimal barrier materials, (ii) analysis of optimal buffer doping type for device scaling. Points (i) and (ii) will be addressed by means of device simulations considering as benchmarking parameters the threshold voltage, the subthreshold slope, and on/off-state current. These parameters are of critical significance in InGaAs MOSFETs for digital circuits.

The interest in developing InGaAs MOSFETs is due to the intrinsic InGaAs high electron mobility. Thus, an accurate mobility estimation is of paramount importance to compare III-V devices and technologies. In **Chapter V** we will present the limitations and error sources of one of the most commonly-adopted technique for electron mobility estimation: the split-CV technique. I will analyze the impact of the different errors that limit the accuracy of split-CV mobility extraction in a $In_{0.53}Ga_{0.47}As$ quantum-well MOSFET having Al_2O_3 gate dielectric and InP barrier. By means of two-dimensional device simulations, current and capacitance curves of the device under investigation will be reproduced. Then I will identify and quantify the errors affecting the split-CV technique. Eventually, error sources will be identified as: spurious charge contributions in non-channel semiconducting layers, access resistances, drift-diffusion channel transport and drain leakage current. All of these effects can potentially impact split-CV channel mobility extraction accuracy in any heterostructure-based field-effect transistor.

Chapter VI will be focused on interface-trap characterization and extraction at III-V/high-k interface and Si/SiO_2/high-k interface. For III-V MOSFETs, the poor quality of high-k/semiconductor interface is one of the main limitations for development of a commercial device. High density of interface traps strongly impacts the device performance in terms of threshold voltage, subthreshold slope, and on/off-state currents effectively nullifying the benefits derived from a high mobility semiconductor. I will present a new generalized technique for interface-trap extraction in III-V devices. The technique is based on combining together theory of two well known methods: the Terman method and the high-low frequency method. I will apply the method for interface-trap characterization in $In_{0.53}Ga_{0.47}As$ MOSCAPs with Al_2O_3 gate dielectric. On the other hand, to characterize Si/SiO_2/high-k interface, I will use charge pumping technique and trap spectroscopy by charge injection and sensing on a particular wafer obtained with slant-etch technique. This technique allows a continued scaled profile of SiO_2 along the wafer to be obtained, thus permitting to investigate the role of different SiO_2 thicknesses on trap density. Eventually trap parameters extracted with the two method listed above will be compared with trap parameters derived from gate current leakage simulation matching experimental data.

Overall results will be summarized in **Chapter VII**.

Figure I.1 shows the schematic cross section of an InGaAs MOSFET and the critical points of its structure that have been addressed in my Ph.D. research and will be debited in the following chapters.

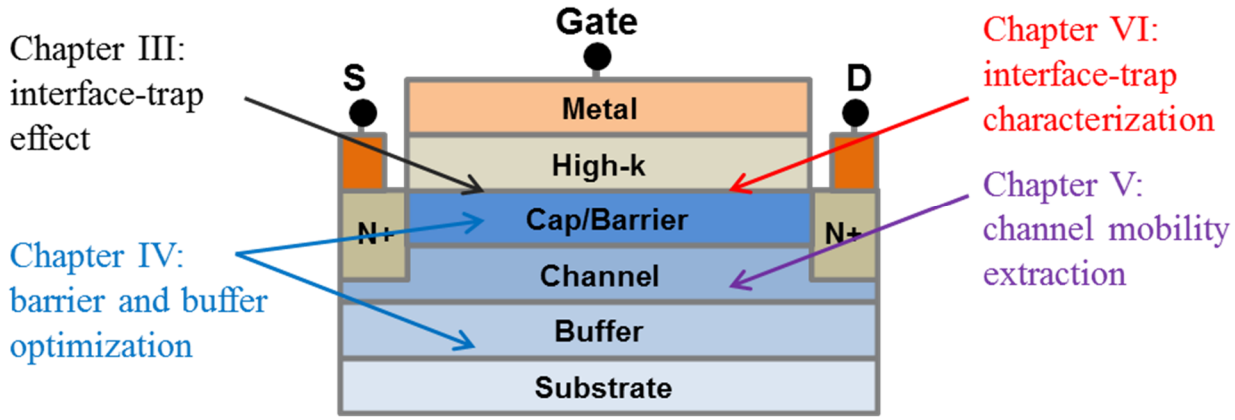

Fig. I.1: Critical points of an InGaAs MOSFET. Each point will be discussed in detail in the correspondent chapter.

Chapter II: III-V MOSFETs

Moore's law has provided guidelines and principles to advance semiconductor industry during the last 30 years. To sustain the Moore's law, a continuous scaling of Si-based MOSFETs is required. The current technological node is the 22-nm one, and next steps foreseen by International Technology Roadmap for Semiconductor (ITRS) will be 16-nm and 12-nm. However, this roadmap does not guarantee that Si-based CMOS scaling will extend that far. This is to be expected, since the gate length for 11-nm technological node may be smaller than 6 nm and the supply voltage should be scaled down 0.5 V.

Within this scenario, identifying a new semiconductor logic device technology that can sustain Moore's law for a few additional generations is becoming increasingly pressing. Often mentioned candidates are III-V materials or nanotubes/nanowires, molecular electronics, spin-based computing, and single-electron devices.

However, at this time, many of these device concepts are hardly beyond the prototyping stage. In contrast, III-V FETs and, in particular, InAlAs/InGaAs HEMTs constitute real device technology making InGaAs MOSFETs, that are derived from this technology, the favorite candidate for n-channel Si-MOSFET replacement. In this chapter we present limits of Si-CMOS and promising directions of III-V FETs.

I.1 - CMOS: Past, Present and Future Perspective

Traditionally, the ITRS [1] has focused on the continued scaling of CMOS technology. However, since 2001, has been reached the point where the horizon of the roadmap challenges the most optimistic projections for continued scaling of CMOS (for example, MOSFET channel lengths below 6 nm). Thus, the ITRS must address post-CMOS devices. The roadmap is necessarily diverse for these devices, ranging from more familiar non-planar CMOS devices and III-V- based devices to exotic new devices such as spintronics or nanotubes. Whether extensions of CMOS or radical new approaches, post-CMOS technologies must further reduce the cost-per-function and increase the performance of integrated circuits. In addition, product performance increasingly does not scale only with the number of devices, but also with a complex set of parameters given by design choices

and technology. While microelectronics community during the past decades has continued to invent new solutions to keep Moore's law alive, there is increasing need for the development of "More than Moore" technologies which are based on merging Si technologies with new devices concepts, but also new materials and manufacturing processes, further than simply scaling with Moore's law (see Fig. II.1).

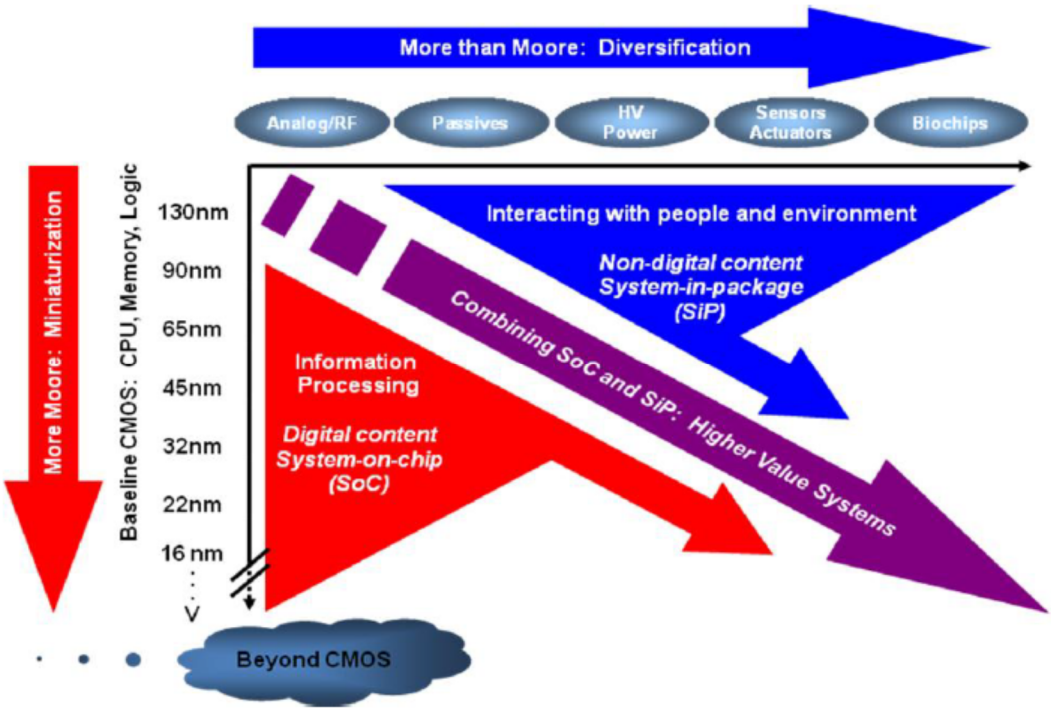

Fig. II.1: More Moore vs. more than Moore. Note that for technological node beyond 16 nm - 12 nm Si-CMOS scaling will not be further possible and beyond-CMOS solutions have to be developed [1].

Following Moore's law would allow the integration of an increasing number of transistors in a single chip, by downscaling dimension of elementary CMOS devices. Dimension downscaling would result in performance advantages in terms of data storage and digital signal processing in microprocessors, memories and logic devices. Devices listed above belong to the system-on-chip (SoC) family.

On the other hand non-CMOS solutions are employed in an entire field of applications such as passive component, sensors and actuators, biological functions, and even embedded software functions. Historically the dimension of non-CMOS devices do not scale with Moore’s law.

Moreover, nowadays is becoming attractive the integration of CMOS and non-CMOS based technologies within a single package called system-in-package, (SiP).Functions initially fulfilled by non-CMOS dedicated technologies may eventually be integrated onto a CMOS SoC, using mixed technologies derived from CMOS know-how.

To further reach the goal of better performance it is becoming incredibly important to develop the so called beyond-CMOS technologies. Beyond-CMOS involves emerging research devices and materials to provide functional scaling substantially beyond that attainable by ultimately scaled Si-CMOS. Among the new devices and materials under investigation have to be mentioned III-V high-mobility devices (MOSFET, HEMT, MOS-HEMT), carbon-based nano-electronics, spin-based devices, single-electron devices, atomic switches, and nano-electro-mechanical-system switches.

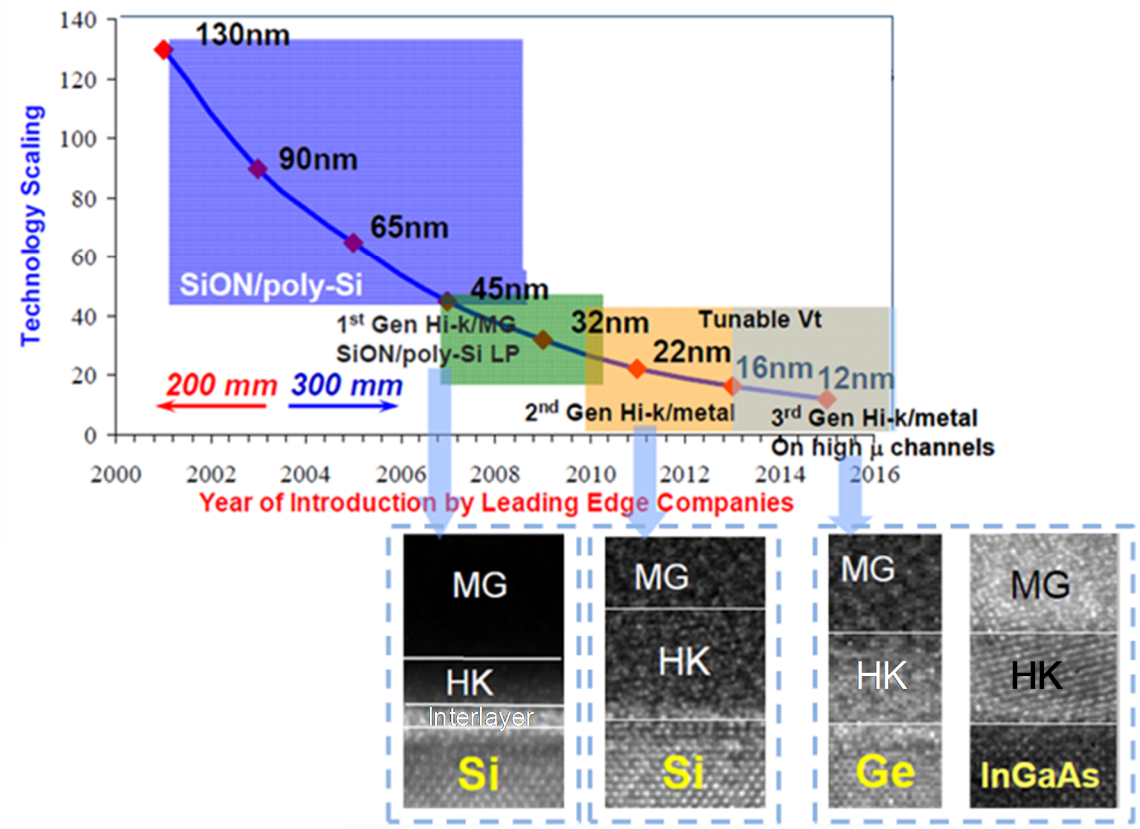

Fig. II.2: Gate stack critical role in roadmap.

Figure II.2 illustrates the downscaling of the technology node along with the gate stack solution adopted to both overcome limits introduced by reducing dimensions and increase device performance. One of the main limitation for the Si-based MOSFET scaling has been represented by the oxide thickness reduction. To maintain charge control in the channel of the device, the gate capacitance has to be as high as possible, this could be obtained by shrinking the thickness of the SiO_2gate oxide. This solution worked until gate leakage current became non negligible and affected the device reliability (i.e. data retention in non volatile memory cells). At the 45-nm node, semiconductor factories introduced the 1stgeneration of transistors with high-k dielectric as a gate oxide. High-k materials such as HfO_2, ZrO_2 or Al_2O_3 thanks to their high dielectric constant

allowed to obtain the same equivalent oxide thickness (EOT) (thus the same channel charge control) with a thicker dielectric layer. EOT was further decreased with the 2nd generation (32 nm - 22 nm) of high-k oxide-based devices by substantially eliminating the SiO_2 interlayer. Anyway, removing interlayer was not drawback-free. High-k/semiconductor interface can not be grown by means of a natural oxide, and the process of oxide deposition results in an interface with high density of defects impacting the figure of merits of transistors. For future technologies, (16 nm and 12 nm), higher mobility materials such as Ge and InGaAs will be needed for channel transport enhancement. Theoretical studies suggest that approaching the ballistic regime of conduction, the FET saturation current is strongly correlated to the semiconductor mobility. High mobility would result in higher saturation current, thus, III-V semiconductor is nowadays seen as a solution to enhance the performance of beyond-CMOS technologies. Of course III-V semiconductor integration will introduce additional challenges for future high-κ dielectric stacks scaling due to the complex nature of their interfaces with channel materials.

I.2 - Scaling Challenges

Planar bulk CMOS scaling is facing difficulties in effectively controlling short-channel effects. A high channel doping is required to reduce short-channel effects and to set the threshold voltage properly. On the other hand, high doping results in undesirable effects such as band-to-band tunneling across the junction, gate-induced drain leakage (GIDL), and degradation of carrier mobility in surface channel. Moreover, with short channel length the effect of threshold voltage variability induced by random doping in the channel is becoming more and more important.

One of the most critical challenges for realizing high-performance MOSFETs with short channel lengths is the reduction of source/drain resistance. Higher current density and smaller dimension needed to follow the roadmap, pose a severe trade-off in scaling MOSFETs. Trade-off that becomes even more difficult for III-V semiconductor devices because of the low doping solubility and thermal doping activation limited by the presence of the high-k. A possible solution is represented by implant-free III-V MOSFETs, in such devices epitaxial growth technique (i.e. metal organic chemical vapor deposition (MOCVD) or molecular beam epitaxy (MBE)) are applied to produce high active doping densities without high temperature anneals.

Another trade-off limiting the MOSFET scaling is given by the necessity of scaling the EOT while keeping gate leakage currents within tolerable limits. Metal gate/high-k/SiO_2 interlayer gate stacks have been an effective solution to reduce EOT and limit gate leakage currents. However, the reduction or elimination of the SiO_2 needed to further scale EOT has been shown to cause high density of interface trap (i.e. 5×10^{12} $cm^{-2}eV^{-1}$ - 1×10^{13} $cm^{-2}eV^{-1}$) resulting in threshold voltage shift, Fermi level pinning, degradation of mobility and reliability issues. Growing quality high-k oxides on III-V materials has long been an industry goal and successes have started to appear only very

recently. Nevertheless, there is still much work to be done in the areas of high-k dielectrics, interface quality, variability, and reliability. Currently many research are investigating gate stack optimization with particular interest in buried-channel MOS-HEMT-like structures. In these structures a cap layer with wider bandgap than the channel is interposed between the high-k and the channel, this could help to: (i) tune the threshold voltage by choosing an adequate cap layer, (ii) reduce channel mobility degradation by outdistancing the inversion layer from the high-defective interface.

For planar devices, threshold voltage tuning and control by setting the gate stack effective work-function has proven to be challenging, and with a foreseen V_{DD} = 0.5 V for the 16 nm node it could be difficult to build enhancement-type MOSFETs. This issue will be even more critical for III-V MOSFETs because of the lack of channel doping as a variable. Effectively tuning the work-function over the bandgap would be very useful.

Approaching the ballistic regime, enhanced channel-carrier low-field mobility and high-field velocity are major contributors to satisfy the MOSFET current performance requirements. Among the solution proposed we find Si-strained devices and III-V semiconductors. The former have been successfully integrated in the industrial fabrication but showed to be less effective with scaling and, moreover, transport enhancement saturates with strain at some point. Thus, thanks to their high intrinsic mobility, III-V materials have shown to be the most effective solution for transport enhance. Anyway, most III-V materials lack good mobility for p-type carriers. A single channel material for both types of channels would be preferable, and materials other than InGaAs are being researched. Ge CMOS is promising for much higher intrinsic mobility for both n- and p-type carriers compared to Si, but n-channel suffers severe resistance issues due to source-drain doping and contact problems. N-channel InGaAs is instead a relatively mature technology and together with Ge p-channel could be a good choice for a CMOS solution even if it adds complexity to the whole process.

Eventually, as Si is the most common platform in the integrated circuit industry, it is largely desiderated to integrate InGaAs n-channel and Ge p-channel CMOS devices with Si technology. It is well known that an issue for the integration is that III-V MOSFETs suffer from low thermal tolerance and degradation of the high-k/semiconductor interface after high temperature processes. Furthermore, realization of high-quality III-V layers on a Si substrate is not straightforward and many techniques such as direct wafer bonding (DWB) and III-V semiconductor over insulator (III-V-OI) are currently evaluated to reach the integration goal.

I.3 - Why High Electron Mobility Semiconductors?

The effective mobility of inversion layer carrier is an important parameter controlling the current in traditional theories of MOSFETs [2],[3], but its role in nanoscale MOSFETs, where off-

equilibrium, velocity overshoot and quasi-ballistic transport dominate [4],[5], is less clear [6]. Under high drain bias where off-equilibrium transport dominates, mobility is not a well defined quantity. Anyway in [7], it was demonstrated that the drain current of a nanoscale MOSFET is directly related to the near-equilibrium mean-free-path for backscattering [6]. Moreover, recently it has been shown in strained devices [8],[9] that the saturation drain current (I_{Dsat}) is more strongly correlated to the low field mobility, which is measured in the same short-channel devices, than was previously believed [10].

Transport in MOSFETs can be explained as it follows [7]. Electrons are injected from the source side into the channel. At the source-channel junction electrons move across a potential barrier whose height is modulated by the gate voltage. Carriers drift along the channel and are extracted at the drain side. The role of the source-channel potential barrier is well known and usually considered in weak inversion regime or treating drain-induced barrier lowering (DIBL). The source-channel potential barrier exists also in above threshold regime. Its effect is well known, but since the channel charge screens the gate voltage, is frequently ignored in treating contemporary MOSFETs. This practice has been justified because transport across the channel has been the limiting factor, but transport across the source-channel barrier will increase in importance and will ultimately limit I_{Dsat} as gate length approaches zero [7].

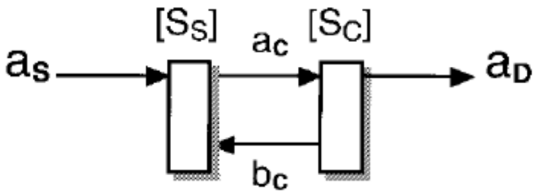

Fig. II.3: Two section model of the MOSFET under saturation conditions [7].

Scattering theory [7] allows to relate the current to transmission and reflection coefficients. In saturation conditions a MOSFET can be treated with the model displayed in Fig II.3. The source is modeled as a reservoir of carriers injecting a flux a_S to the source-channel barrier. A fraction t_c of the carriers injected move across the channel and reach the drain, and a fraction $r_c = 1-t_c$ is backscattered at the source-channel barrier and reenters the source [7].

The saturation current can be written as [7]:

$$I_{Dsat} = C_{OX} W_G v_T \left(\frac{1 - r_c}{1 + r_c}\right)(V_{GS} - V_T)\,. \qquad (II.1)$$

If there is no electric field in the channel, the backscattering coefficient can be defined as [7]:

$$r_{C0} = \frac{L}{L + \lambda}, \qquad (II.2)$$

where λ is the mean-free path.

On the other hand, when the electric field in the channel is present we can assume that carriers which travel only a short distance down a potential drop are unlikely to reemerge even if they backscatter. We assume the critical distance to be the distance over which the potential drops of k_BT/q and we write [7]:

$$r_{C\varepsilon} = \frac{l}{l + \lambda}, \qquad (II.3)$$

where $l = (k_BT/q)\varepsilon(0^+)$. Note that r_C is determined by the electric field profile near the source where the electrons have been heated no more than k_BT/q, so λ can be estimated from the low field mobility μ_n^0 to write [7]:

$$r_{C\varepsilon} = \frac{1}{1 + 2\mu_n{}^0\varepsilon(0^+)/v_T}. \qquad (II.4)$$

Equation above, approaches 1 if the electric field reduces to zero. In short-channel devices, some electrons can transmit across the field free channel, $r_C < 1$ and its value is given by r_{C0} (II.2). After this consideration we can write a more general expression [7]:

$$r_C = \frac{r_{C0}}{1 + 2\mu_n{}^0\varepsilon(0^+)/v_T}. \qquad (II.5)$$

To eventually find a connection between the scattering approach and conventional models, consider a device with a channel length long enough that $r_{C0} \approx 1$, then combining (II.1) and (II.4) we find [7]:

$$I_{Dsat} = \left[\frac{C_{OX}W_G}{\frac{1}{v_T} + \frac{1}{\mu_n{}^0\varepsilon(0^+)}}\right](V_{GS} - V_T). \qquad (II.6)$$

Equation above shows that I_{Dsat} is maximized by both a higher value of low-field mobility and an increased electrical field near the source. The effect of the two contributions is to reduce the source backscattering [7].

Therefore even approaching the ballistic regime in nanoscale MOSFETs, the low-field mobility continues to have physical meaning as a measure of the mean-free path into the critical region.

From this point of view, it can be understood why so many efforts are made to enhance carrier mobility by means of strained-Si or integrating III-V materials. Eventually scaling of MOSFETs for next technology nodes is likely to require alternate channel materials than Si in order to continue to improve speed ($I_{Dsat}/C_{inv}V_{DD}$) but with low supply voltage (V_{DD}= 0.5 V) at the same time. To attain higher drive currents, materials with light effective masses are greatly beneficial in quasi-ballistic transport with enhanced thermal velocity and injection at the source end. In current view the materials of choice seem to be InGaAs for n-channel and Ge for p-channel.

I.4 - InGaAs MOSFET Overview

As explained in the previous section, higher mobility results in higher current not only in long channel devices but also approaching the ballistic regime [7]. Thus, use of III-V compound semiconductors as n-type channel replacement materials has attracted great attention because of their excellent bulk electron mobilities.

Property/ Material	Si	Ge	GaAs	$In_{0.53}Ga_{0.47}As$	InAs
Eg (eV)	1.1	0.66	1.4	0.75	0.35
μ_n (cm^2/v-sec)	1,350	3,900	4,600	>8,000	40,000
μ_p (cm^2/v-sec)	480	1,900	500	350	<500
m^*/m_o	0.165	0.12	0.067	0.041	0.024
Lattice mismatch to Si	0	4%	4%	8%	12%
		pMOSFET		nMOSFET	

Table II.1: Comparison among electrical properties of Si, Ge, InGaAs and its components.

In particular (see Table II.1), InGaAs is the main candidate because if compared with Si it shows a very good compromise between GaAs and InAs properties. InAs shows an electron mobility (μ_n) of more than 40000 cm^2/Vs, but low effective mass (m^*/m_0) equal to 0.024 resulting in low density of states (DOS) and consequently low inversion capacitance. Moreover, InAs shows a 12% mismatch of reticular crystal with respect to Si, and this will require more effort to reach III-V over Si integration. On the other hand GaAs has a $\mu_n \approx 4600$ cm^2/Vs, $m^*/m_0 = 0.067$ and a lattice mismatch of 4%. As previously described the main goal is to enhance μ_n. A ternary compound InGaAs, with As molar fraction equal to 0.47, exhibits μ_n theoretically higher than 8000 cm^2/Vs

against a reduction in m^*/m_0 (= 0.041) that results in a not so critical DOS bottleneck. Moreover, InGaAs shows a good compromise in terms of bandgap (Eg) equal to 0.75eV.

Nevertheless, InGaAs suffers of low holes mobility (μ_p) that prevents the realization of an efficient p-channel MOSFET. To overcome this limitation, future CMOS device will probably integrate InGaAs n-channel and Ge p-channel devices. Indeed, Ge has μ_p = 1900 cm^2/Vs, six times larger than InGaAs where μ_p = 350 cm^2/Vs.

As a confirmation of the importance of III-V materials, Fig. II.4 shows the roadmap for DRAM production [1]. The roadmap identifies enhanced transport in the channel, by means of alternate channel like InGaAs and Ge, as the next feasible solutions to further match scaling requirements. Indeed nowadays, III-V and Ge CMOS is enough mature to move from initial research applications (black area) to development and optimization of this technology (light blue area). This phase is foreseen to continue until 2015 when qualification/pre-production will start (white area). Around two years should be needed in order to understand and deal with new different reliability, yield, and process integration issues associated with these innovative materials. Eventually it is projected that the first product will be introduced in 2018 (shaded area).

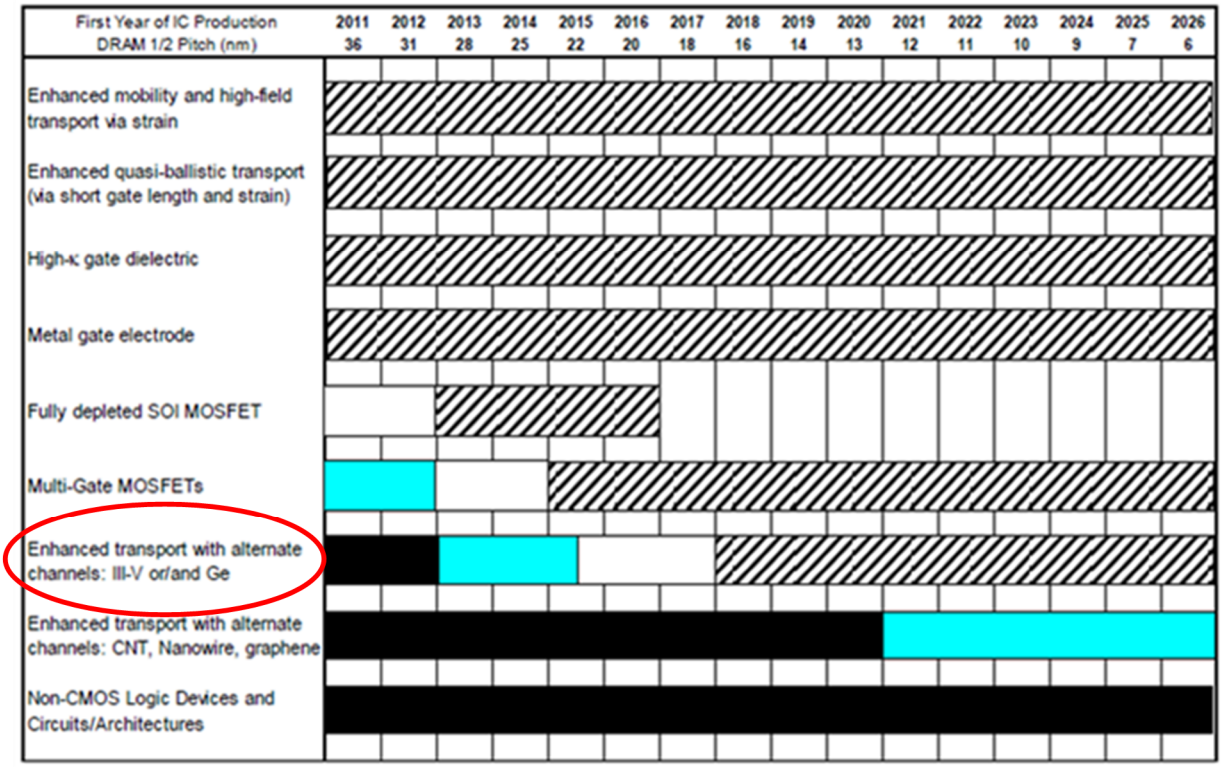

Fig. II.4: Roadmap for DRAM scaling. (Black) research required, (light blue) development underway, (white) qualification/pre-production, (shaded) continuous improvement [1].

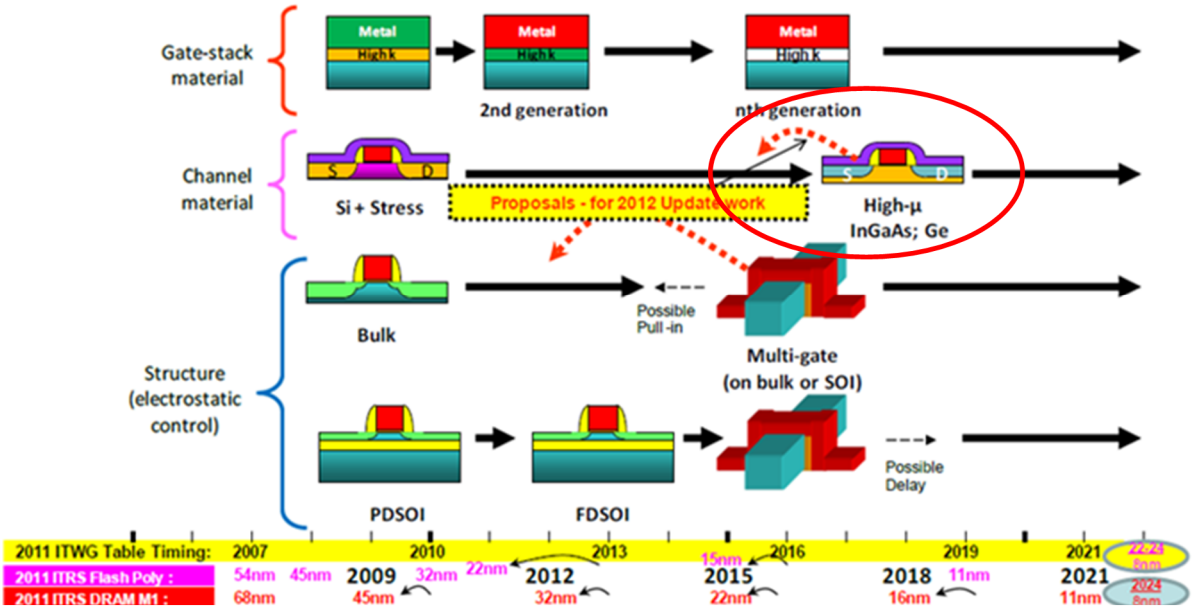

Fig. II.5: Foreseen timeline for CMOS scaling [1].

Further, Fig. II.5 shows the foreseen timeline for CMOS scaling in terms of gate-stack material, channel material and device structure [1]. Next generation of CMOS circuits should include metal/high-k gate dielectric, InGaAs and Ge semiconductor in a multi-gate or FINFETs structure. Technology and process to achieve metal/high-k gate stack are already known and used in Si-based CMOS. Each further generation of gate- stack has the purpose of improve the quality of the interface between high-k and semiconductor. To substitute Si in MOSFET channel, many efforts have been made in the previous decade to investigate III-V materials and Ge, and nowadays the technology is sufficiently mature that ITRS proposed to anticipate its qualification/pre-production from 2018 to 2015 [1]. Eventually, to obtain a better electrostatic control of the gate charge, multi-gate MOSFETs and FINFETs architecture are the proposed solution.

As an evidence of the improvement obtained in the last five years, here it follows a brief literature overview regarding InGaAs n-MOSFET research and development.

In 2007 Hudait [11] described for the first time the heterogeneous integration on Si (by means of a 1.3 μm buffer layer) of quantum-well n-MOS-HEMTs with $In_{0.7}Ga_{0.3}As$ channel. MOS-HEMTs with gate length (L_G) = 80 nm showed V_T = 0.11 V, μ_e = 10000 cm^2/Vs, I_{Dsat} 320 mA/mm and I_{ON}/I_{OFF} = 2150 at V_{DS} = 0.5 V with a voltage swing of V_{GS} 0.5 V. Enhancement-mode $In_{0.53}Ga_{0.47}As$ channel n-MOSFETs with Al_2O_3 gate dielectric were showed by Xuan [12]. MOSFETs with L_G = 0.5 μm were characterized by V_T = 0 V, μ_e = 2500 cm^2/Vs, I_{Dsat} = 490 mA/mm at V_{DS} = 2 V, transconductance peak (g_m) = 175 mS/mm, subthreshold slope (SS) of 240 mV/dec, DIBL = 350 mV/V and on state resistance (R_{on}) of 2300 Ωμm. The Al_2O_3/InGaAs interface, that nowadays is one of the main candidate for the gate stack, showed an interface trap

density (D_{it}) of 1.4×10^{12} $cm^{-2}eV^{-1}$. Another $In_{0.53}Ga_{0.47}As$ channel n-MOSFET with Al_2O_3 gate dielectric was demonstrated by Xuan [13]. For the 0.5 µm L_G device the following figures of merit were found: V_T = 0.25 V, μ_e = 2200 cm^2/Vs, I_{Dsat} = 425 mA/mm at V_{DS} = 2 V, g_m = 145 mS/mm, SS = 260 mV/dec, DIBL = 150 mV/V, R_{on} = 2000 Ωµm and again $D_{it} = 1.4\times10^{12}$ $cm^{-2}eV^{-1}$. Passlack [14] demonstrated $In_{0.7}Ga_{0.3}As$ channel n-MOSFETs with GdGaO gate oxide. For L_G = 1 µm device, it was found V_T = 0.26 V, μ_e = 5500 cm^2/Vs, I_{Dsat} = 407 mA/mm at V_{DS} = 2 V, g_m = 477 mS/mm, R_{on} = 1900 Ωµm, f_{max} = 37 GHz and f_t = 17 GHz. A similar $In_{0.7}Ga_{0.3}As$ channel n-MOSFET was demonstrated by Hill [15]. MOSFETs with Ga2O3/GaGdO gate dielectric and L_G = 1 µm showed V_T = 0.26 V, μ_e = 5230 cm^2/Vs, I_{Dsat} = 407 mA/mm at V_{DS} = 2 V, g_m = 477 mS/mm, SS = 102 mV/dec and R_{on} = 1920 Ωµm. This latter device represented the state of the art for MOSFETs, with the highest effective mobility and transconductance measured in 2007.

In 2008, Ok [16] presented an n-MOSFET with $In_{0.53}Ga_{0.47}As$ channel and HfO_2 gate dielectric, L_G = 20 µm, V_T = -0.3 V, μ_e = 1034 cm^2/Vs and I_{Dsat} = 44 mA/mm at V_{GS} -V_T = 2 V. $In_{0.53}Ga_{0.47}As$ n-MOSFET with HfAlO gate dielectric and L_G = 4 µm was showed by Lin (8). Device characteristics were: V_T = -0.3 V, μ_e = 1560 cm^2/Vs, I_{Dsat} = 54 mA/mm at V_{GS} = 3 V, g_m = 34 mS/mm, SS = 196 mV/dec, DIBL = 68 mV/V and $D_{it} = 3\times10^{12}$ $cm^{-2}eV^{-1}$.

Many works were presented in 2009. Sun [17] presented an $In_{0.7}Ga_{0.3}As$ channel quantum-well n-MOS-HEMT with Al_2O_3 gate dielectric. Devices with InAlAs barrier layer and L_G = 160nm showed: V_T = -0.6 V, μ_e = 3810 cm^2/Vs, I_{Dsat} = 825 mA/mm at V_{GS} = 1 V, g_m = 715 mS/mm and R_{on} = 3500 Ωµm. Yokoyama [18] showed for the first time the integration of III-V OI MOSFETs on a Si-substrate. $In_{0.53}Ga_{0.47}As$ channel n-MOSFET, fabricated using DWB Si-integration, showed the following figures of merit for the L_G = 500 µm device: μ_e = 1000 cm^2/Vs, and a $D_{it} \approx 10^{12}$ $cm^{-2}eV^{-1}$. Zhao [19] investigated the effect of an InP barrier layer on the performances of $In_{0.7}Ga_{0.3}As$ channel n-MOSFETs with Al_2O_3 gate dielectric. InP barrier layer substantially results in higher mobility. For a buried device with L_G = 20 µm, it was found: V_T = -0.25 V, μ_e = 4402 cm^2/Vs, I_{Dsat} = 98 mA/mm at V_{DS} = 2.5 V, g_m = 6.5 mS/mm and SS = 106 mV/dec. Lin [20] showed a common gate stack solution to integrate InGaAs and Ge in a CMOS with Al_2O_3 gate dielectric. For a L_G = 1.5µm, μ_e = 1300 cm^2/Vs and μ_p = 400 cm^2/Vs. I_{Dsat} = 600 mA/mm at $V_{GS} - V_T$ = 2 V (I_{Dsat} = 200 mA/mm at $V_{GS} - V_T$ = -1 V) and g_m = 340 mS/ mm (g_m = 95 mS/mm) for n-channel (p-channel) device. Extracted D_{it} in the order of 10^{12} $cm^{-2}eV^{-1}$. Lin [21] also presented an n-channel MOSFET with Al_2O_3 gate dielectric and L_G = 10 µm, characterized by $V_T \approx 0.3$ V, μ_e = 3000 cm^2/Vs, I_{Dsat} = 220 mA/mm at $V_{GS} - V_T$= 2 V, g_m = 140 mS/mm. Moreover $D_{it} = 1\times10^{12}$ $cm^{-2}eV^{-1}$ near the conduction band and $D_{it} = 2\times10^{13}$ $cm^{-2}eV^{-1}$ near the valence band.

In 2010 Hill [22] showed for the first time an $In_{0.53}Ga_{0.47}As$ channel quantum-well n-MOS-HEMT heterointegrated on a large diameter Si substrate fabricated with very large scale of integration (VLSI) compatible process. MOSFETs with L_G = 500 nm showed V_T = -0.25 V, μ_e = 2000 cm^2/Vs, I_{Dsat} = 471 mA/mm at V_{DS} = 1 V and g_m = 1005 mS/mm. Zhao [23] compared the performance of an $In_{0.7}Ga_{0.3}As$ channel quantum-well MOSFET with L_G = 20 µm and with single

InP barrier and composite InP/InAlAs barrier. Single barrier leads to $\mu_e \approx 3000$ cm^2/Vs and $I_{Dsat} \approx$ 100 mA/mm at $V_{DS} = 2.5$ V. Composite barrier helps to enhance $\mu_e = 4729$ cm^2/Vs and $I_{Dsat} = 132$ mA/mm at $V_{DS} = 2.5$ V. An $In_{0.53}Ga_{0.47}As$ channel n-MOSFET with HfAlO gate dielectric and $L_G =$ 2 µm were reported by Chin [24]. Investigated devices showed $V_T \approx 0.2$ V, $\mu_e = 1700$ cm^2/Vs, I_{Dsat} = 400 mA/mm at $V_{GS} - V_T = 3$ V, SS = 155 mV/dec, DIBL = 15 mV/V and a $D_{it} = 6.5\times10^{11}$ cm^{-2}eV^{-1}.

In 2011 Yokoyama [25] demonstrated $In_{0.53}Ga_{0.47}As$ channel n-MOSFETs with Al_2O_3 gate dielectric on a Si substrate using DWB integration. For a device with $L_G = 50$ µm, $\mu_e = 912$ cm^2/Vs, $I_{Dsat} = 1$ mA/mm and $I_{ON}/I_{OFF} = 10^5$ at $V_{DS} = 1$ V with V_{GS} voltage swing of 6 V. Xue [26] studied the effect of different barrier layer composition for an $In_{0.7}Ga_{0.3}As$ quantum well n-MOSFET with Al_2O_3 gate dielectric and $L_G = 20$ µm. It was found that among the studied solutions, composite barrier InP/InAlAs results in best performances such as $\mu_e = 5700$ cm^2/Vs, $I_{Dsat} = 123$ mA/mm at $V_{GS} - V_T = 2$ V and $g_m \approx 6$ mS/mm. Yonai [27] reported $In_{0.53}Ga_{0.47}As$ channel n-MOSFET with Al_2O_3 gate dielectric. For a device with $L_G = 50$ nm it was found: $V_T \approx -1$ V, $\mu_e = 4500$ cm^2/Vs, I_{Dsat} = 2400 mA/mm at $V_{GS} = 3$ V, $g_m = 1170$ mS/mm, SS ≈ 300-900 mV/dec and $R_{on} = 93$ Ωµm.

In 2012 Xue [28] demonstrated $In_{0.7}Ga_{0.3}As$ channel n-MOSFETs with composite InP/InAlAs barrier and Al_2O_3 gate dielectric. For $L_G = 40$ nm, $\mu_e = 5800$ cm^2/Vs, $I_{Dsat} = 600$ mA/mm at $V_{GS} - V_T = 1.4$ V, $g_m = 90$ mS/mm, SS = 130 mV/dec, DIBL = 175 mV/V and $D_{it} = 1\times10^{12}$ cm^{-2}eV^{-1}. Suleiman [29] investigated $In_{0.53}Ga_{0.47}As$ channel n-MOSFETs with HfO_2 gate dielectric. Devices with $L_G = 5$ µm showed $\mu_e = 1100$ cm^2/Vs, $I_{Dsat} = 120$ mA/mm at $V_{GS} - V_T = 2$ V, $g_m = 60$ mS/mm and $D_{it} = 5\times10^{11}$ cm^{-2}eV^{-1}. Egard [30] showed an high-frequency performance $In_{0.53}Ga_{0.47}As$ channel n-MOSFET with Al_2O_3 gate dielectric and $L_G = 55$ nm. Figures of merit can be summarized as it follows: $V_T = 0.06$ V, $I_{Dsat} = 2000$ mA/mm at $V_{GS} = 1.8$ V, $g_m = 1900$ mS/mm, SS = 187 mV/dec, $R_{on} = 199$ Ωµm, $D_{it} = 8\times10^{12}$ cm^{-2}eV^{-1}, $f_{max} = 292$ GHz and $f_t = 244$ GHz. Li [31] reported $In_{0.53}Ga_{0.47}As$ channel quantum-well MOSFETs with Al_2O_3 gate dielectric and InAlAs barrier. Electrical characteristics for the device with $L_G = 120$ nm included: $V_T = -1.6$ V, $\mu_e = 5260$ cm^2/Vs, $I_{Dsat} = 1884$ mA/mm at $V_{GS} = 1$ V, $g_m = 1126$ mS/mm, SS = 135 mV/dec, DIBL = 333 mV/V and $R_{on} = 156$ Ωµm. Zhou [32] presented an on-Si-substrate n-MOS-HEMT with $In_{0.53}Ga_{0.47}As$ channel, Al_2O_3 gate dielectric and InAlAs barrier. $L_G = 30$ nm devices were characterized by $V_T = -1.32$ V, $\mu_e = 4805$ cm^2/Vs, $I_{Dsat} = 1698$ mA/mm at $V_G = 1.5$ V, $g_m = 1074$ mS/mm and $R_{on} = 133$ Ωµm.

Chapter III: Interface Trap Effect in III-V Inversion Type MOSFETs

In this chapter interface-trap effects are analyzed in inversion-type, enhancement-mode $In_{0.53}Ga_{0.47}As/ZrO_2$ and $In_{0.53}Ga_{0.47}As/ In_{0.2}Ga_{0.8}As/ZrO_2$ n-channel MOSFETs, by comparing measurements and numerical device simulations of DC transfer characteristics. Device simulations can reproduce measured threshold voltages under the hypothesis that interface traps are donor-like throughout the InGaAs bandgap, allowing for strong inversion operation regardless of the relatively high interface-trap density. Effects induced by donor-like interface traps in MOSFETs having a thin $In_{0.2}Ga_{0.8}As$ cap layer interposed between gate dielectric and channel are qualitatively different from those observed in standard MOSFETs (without the cap). Increasing the donor-like trap density decreases the threshold voltage in capped devices, while it leaves it unchanged in uncapped ones. As a result, donor-like interface traps can explain the threshold-voltage difference observed in MOSFETs with and without the cap.

Device concepts that are being evaluated to replace typical Si MOSFETs include HEMT-like structures [33],[34], MOS-HEMTs [35],[15],[36],[37],[38],[39],[23], as well as inversion-type MOSFETs [40],[41],[42],[43],[44],[45],[46],[20],[47],[48]. Aspects still requiring research efforts and appropriate solutions encompass fundamental physics concerns, such as the limitations to the channel carrier density and drive current imposed by the small DOS [49],[50],[51], technological compatibility problems, like the integration of the III-V material system on the Si wafer [11], as well as process/device optimization issues, like gate-stack optimization [43],[46],[48],[52],[53],[16] and the reduction of source/drain contact and sheet resistances [38],[45],[54].

The poor quality of the dielectric interface has historically been the major obstacle on the path towards the development of III-V MOSFETs [55]. Recently, specific combinations of high-k dielectric materials, suitable deposition techniques, III-V channel materials and crystal orientations have been shown to allow for the fabrication of n-channel MOSFETs that are immune from Fermi-level-pinning problems [35],[15],[36],[37],[38],[39],[23],[40],[41],[42],[43],[44],[45],[46],[20], [47],[48],[52],[53],[16],[56]. Rather than to having achieved a low interface-trap density, these

results must be ascribed to the interface property of having a charge-neutrality level located at or, even, above the conduction-band edge (E_C). When this is the case, interface traps are donor-like throughout the semiconductor bandgap [20],[57],[58],[59]. This in turn leaves the Fermi level unpinned in the upper half of the bandgap, thus enabling actual inversion-type operation of the n-channel MOSFET.

Despite recent progresses, gate-stack optimization and, particularly, D_{it} minimization still represent major issues for the development of InGaAs MOSFETs (as well as for other III-V FETs). Even though channel inversion is not inhibited, interface traps can play a detrimental role in the device performance, by influencing key parameters, such as threshold voltage (V_T), channel mobility, and sub-threshold slope (SS), and thus impacting both on-state (I_{ON}) and off-state (I_{OFF}) currents. The same effects can be induced in MOS-HEMT structures as well.

Interface-trap generation is also expected to be one of the most severe reliability-limiting factors [60]. Developing an in-depth understanding of interface-trap effects in these devices is therefore crucial for both process/device optimization and reliability assessment purposes.

In this chapter, we address the effects of interface traps in inversion-type InGaAs MOSFETs with ZrO_2 gate dielectric[61]. Devices used in this study were provided by SEMATECH (Albany, NY, USA). Two-dimensional device simulations are adopted to gain insight into the interface-trap effects on DC transfer characteristics and to analyze the impact of different interface-trap distributions. Specific contributions improving the comprehension of mechanisms underlying interface-trap effects in the devices under study are as follows.

1) A quantitative comparison between experimental and simulated IV curves using D_{it} distributions in agreement with previous literature on InGaAs/Al_2O_3 MOSFETs [57] and supporting the conclusion that strong inversion is feasible also in the InGaAs/ZrO_2 devices considered here, thanks to the donor-like nature of interface traps within the InGaAs bandgap and regardless of the relatively high D_{it}.

2) The description of the non-trivial effects associated with donor-like interface traps in MOSFETs having a thin $In_{0.2}Ga_{0.8}As$ cap layer interposed between the gate dielectric and the $In_{0.53}Ga_{0.47}As$ channel. Including a cap with wider bandgap than the channel into the device epilayer structure is a means that has been adopted in both InGaAs MOSFETs and MOS-HEMTs to attenuate the interface-related mobility degradation [39],[23]. Understanding that interface-trap effects in these devices can be qualitatively different from those observed in standard MOSFETs (without cap layer) is important for their optimization.

3) A systematic analysis of the effects of increasing densities of donor-like and acceptor-like interface traps in MOSFETs with and without the cap layer that can be useful in the interpretation of reliability testing experiments.

III.1 - Device Fabrication

Devices under consideration are self-aligned, inversion-type, InGaAs/ZrO_2 MOSFETs having two different epilayer structures, one with the gate dielectric directly deposited onto the $In_{0.53}Ga_{0.47}As$ channel (uncapped devices), the other with a 2-nm $In_{0.2}Ga_{0.8}As$ cap layer interposed (capped devices). The latter is intended for mobility improvement by outdistancing the inversion channel forming at the $In_{0.53}Ga_{0.47}As/In_{0.2}Ga_{0.8}As$ interface from the dielectric surface. Devices were fabricated by SEMATECH (Albany, NY, USA).

$In_{0.53}Ga_{0.47}As$ growing in MBE
$In_{0.20}Ga_{0.80}As$ growing in MBE
ZrO_2 deposition by ALD
TiN/TaN deposition: 20nm/200nm
Gate patterning (RIE)
S/D implantation: Si (25KeV, 1E15)
S/D activation: RTA: 0°C-800°C
Metal deposition

Table III.1: Process flow of the tested devices.

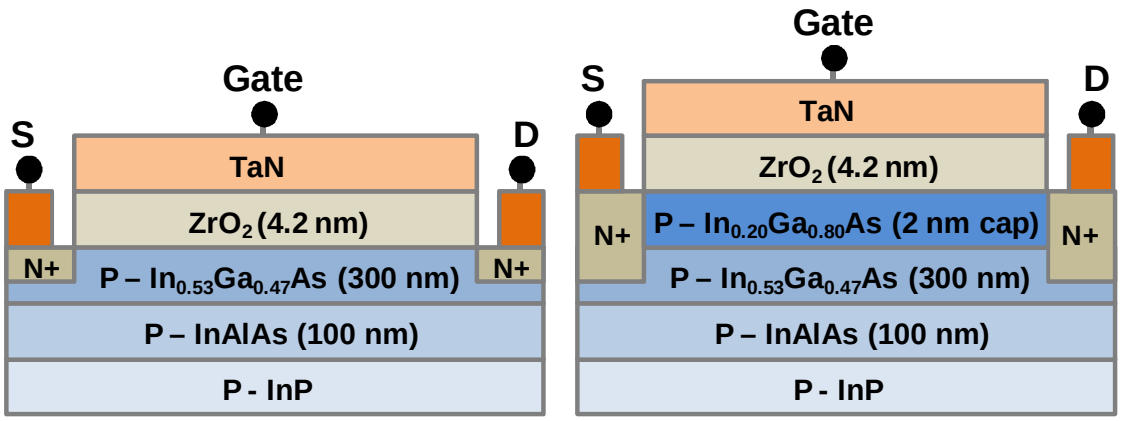

Fig. III.1: Schematic cross sections of devices under study. Left:$In_{0.53}Ga_{0.47}As/ZrO_2$ MOSFET (uncapped device). Right: $In_{0.53}Ga_{0.47}As/ In_{0.}2Ga0_{.8}As/ZrO_2$ MOSFET (capped device).

Figure III.1 shows schematic cross sections of the two device types. Gate length (L_G) is 10 µm for both structures. Gate width (W_G) is 600 µm.

The process flow for MOSFETs with TaN/ZrO_2 stacks is summarized in Table III.1. Epistructures were grown on InP by MBE. The high-k stack was processed using atomic layer deposition (ALD) without any surface pre-treatment (except for cleaning). The ZrO_2 thickness is 4.2 nm. Interfacial native oxide thickness is 0.5 nm. The ZrO_2 relative dielectric constant is 21. The resulting EOT is 0.8 nm. The TiN/TaN electrode was formed using ALD and reactive dc sputtering,

followed by reactive ion etch (RIE). After source/drain (S/D) activation with rapid thermal annealing (RTA) and laser anneal, low-resistance ohmic contacts were formed by using an AuGe/Ni/Au alloy.

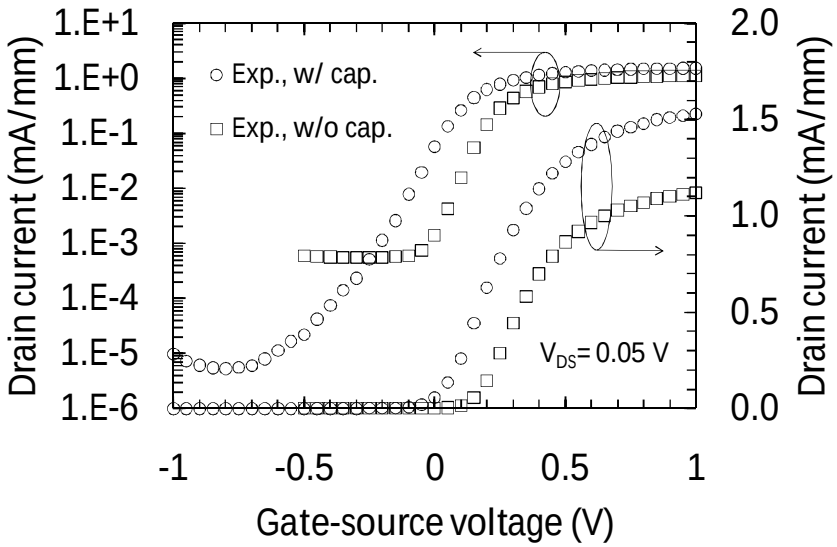

Fig. III.2: Experimental drain-current vs. gate-source-voltage characteristics at a drain-source voltage of 0.05 V for MOSFETs with and without the $In_{0.2}Ga_{0.8}$ As cap on both linear-linear (right y-axis) and log-linear (left y-axis) scales.

III.2 - Experimental Results

Figure III.2 shows experimental drain-current (I_D) vs. gate-source-voltage (V_{GS}) characteristics at a drain-source voltage (V_{DS}) of 0.05 V for representative devices with and without the $In_{0.2}Ga_{0.8}As$ cap.

As can be noted, capped devices show a smaller V_T than devices without the cap (≈0.03 V against ≈0.13 V). The sign of this V_T is opposite to the expected one. The introduction of the cap reduces the effective gate capacitance (for same gate metal and dielectric material and thickness). This should result in a positive V_T change. In section III.4, we will show that the negative V_T shift induced by the cap can result from the qualitatively different impact on V_T of interface traps in the two device types.

The subthreshold slope (SS) is slightly larger in the capped device than in the uncapped one (139 mV/dec against 107 mV/dec), suggesting a correspondingly higher D_{it}.

At small currents, the drain reverse leakage current dominates. The reverse leakage current floor is around the 10^{-6} A/mm and 10^{-8} A/mm level in the uncapped and capped device, respectively. This difference can be explained by the different electron lifetime characterizing wafers onto which devices with and without cap have been fabricated.

Devices with the cap, finally, exhibit a larger I_{ON} than those without. This is a combined effect of smaller V_T and larger transconductance. The latter is due to the higher channel mobility of capped devices, as confirmed by split-CV measurements, yielding peak mobilities of ≈1960 cm^2/Vs and ≈1500 cm^2/Vs for the capped and uncapped MOSFETs, respectively.

III-3. Device Simulations

Two-dimensional device simulations have been carried out using the code Dessis-8.0 (Synopsys Inc.) [62]. The adopted transport model is the drift-diffusion one. Nominal values have been adopted for the substrate p-type doping (5×10^{17} cm^{-3}) and for all geometrical parameters, including gate length (L_G=10 μm) and width (W_G=600 μm). TaN work function and ZrO_2 relative dielectric constant have been set in agreement with literature (Φ_M= 4.6 eV, k_{ZrO2}= 21).

The parameters of the Arora's model [63] have been adjusted to reproduce literature data from n-doped InGaAs [64], allowing doping-dependent mobility degradation in the source and drain regions to be accounted for. Source/drain doping has been modeled by Gaussian profiles. The latter have been adjusted to reproduce source/drain sheet resistances obtained from transmission line model (TLM) measurements (≈500 Ω/□), yielding a peak density of 1.85×10^{18} cm^{-3} (assumed at the InGaAs surface) with a junction depth of 50 nm. Source and drain contact resistances have been set in agreement with TLM measurements (1.5 Ω/mm).

The Lombardi's model [63] for mobility degradation at semiconductor-insulator interfaces has been adopted to reproduce the inversion mobility drop at high V_{GS} measured with the split-CV method in the two device types. Model parameters have in particular been adjusted to force the following, simplified power-law dependence of the surface mobility on the transverse electric field E_t: $\mu_n^{-1} = \mu_{peak}^{-1} + (a\times E_t^{-b})^{-1}$, where μ_{peak}=1500 $cm^2/(V\cdot s)$, $a=4.5\times10^{12}$ $cm^2/(V\cdot s)$, b=1.7 for the uncapped MOSFET, while μ_{peak}=1960 $cm^2/(V\cdot s)$, $a=9\times10^{12}$ $cm^2/(V\cdot s)$, b=1.67 for the capped one.

Carrier lifetimes have been adjusted, to fit the drain current leakage floor in the two device types. A value of 10^{-9} s was used for the capped device. A much shorter value (10^{-11} s) had to be adopted for the uncapped device, indicating a starting material of worse quality.

Simulator's default values have been adopted for bandgap and electronic affinity values of the $In_xGa_{1-x}As$ and $In_xAl_{1-x}As$ compounds, resulting in the band alignment shown in Fig. III.3.

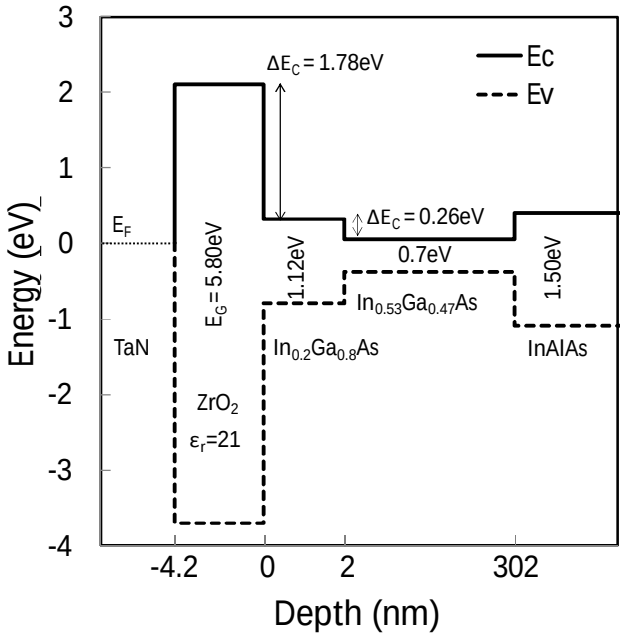

Fig. III.3: Band alignment along the device depth assumed in the simulations. The $In_{0.2}Ga_{0.8}As$ layer is present in the capped devices only. Depths are not to scale.

III.4 - Fitting of Experimental Characteristics

All simulation input parameters considered above have been set to either nominal or literature values, or they have been derived from measurements. Figure III.4 shows the outcomes of device simulations incorporating this geometrical and physical description for the two device types, as compared with the corresponding experimental curves (same as shown in Fig. III.2). Interface traps are for the moment neglected in the simulations. As can be noted, I_{ON} currents are well reproduced by simulations for both the uncapped and the capped device. V_T is matched for the uncapped device, only. Contrarily to what experimentally observed, the capped device is characterized, according to simulations, by a more positive V_T than the uncapped one. As already pointed out, this is actually what one should expect, considering that the $In_{0.2}Ga_{0.8}As$ cap layer reduces the gate capacitance. SS is underestimated by simulations in both device types.

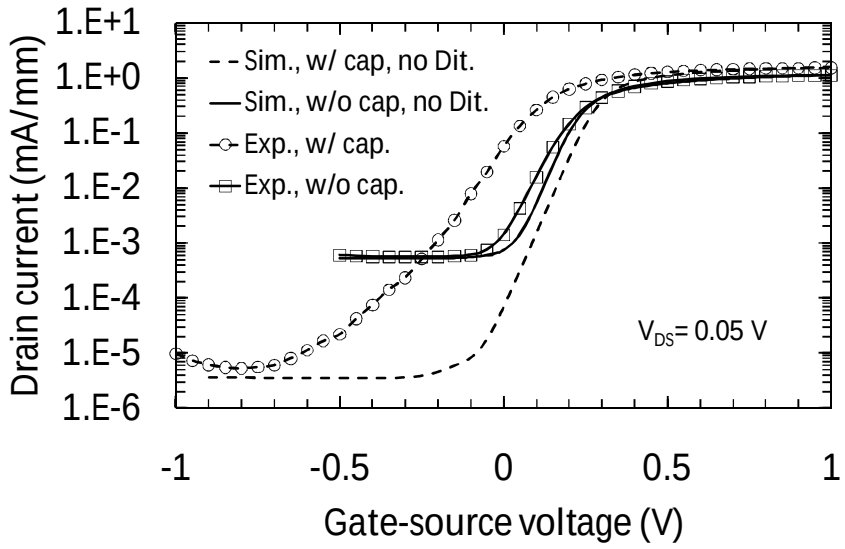

Fig. III.4: Experimental (symbols) drain-current vs. gate-source-voltage characteristics at a drain-source voltage of 0.05 V for MOSFETs with and without the $In_{0.2}Ga_{0.8}As$ cap, compared with the outcomes of device simulations neglecting interface traps (lines).

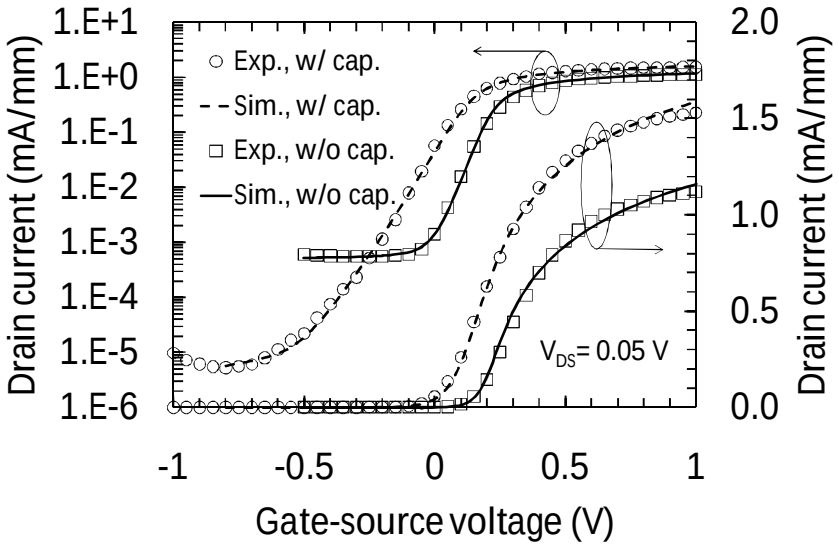

Fig. III.5: Experimental (symbols) and simulated (lines) drain-current vs. gate-source-voltage characteristics at a drain-source voltage of 0.05 V for MOSFETs with and without the $In_{0.2}Ga_{0.8}As$ cap on both linear-linear (right y-axis) and log-linear (left y-axis) scales. Simulations incorporate the D_{it} profiles shown in Fig. III.6.

By assuming simulations shown in Fig. III.4 as a reasonably physical description of the device behavior under the assumption of an ideal ZrO_2/InGaAs interface, we have then introduced interface traps in the simulations with the goal of reducing discrepancies from experiments. Noteworthy, this can only be accomplished if interface traps are assumed to be donor-like traps throughout the InGaAs bandgap. More particularly, the negative V_T shift induced by the

$In_{0.2}Ga_{0.8}As$ cap can be explained, provided that interface traps are donor-like. If interface traps are instead assumed to be acceptor-like, V_T shifts in capped devices towards more positive values, i.e. oppositely to what experimentally observed. This will clearly be shown in section III.4.2. On the other hand, experimental SS can be fitted by assuming either donor- or acceptor-like interface traps.

The fitting of the I_D-V_{GS} curves has been pursued, by adopting D_{it} distributions in qualitative agreement with interface-trap characterization results reported in [57] and [59], namely donor-like interface traps have been assumed to peak at the valence-band edge (E_V) and to decrease monotonically throughout the InGaAs bandgap. Gaussian profiles have specifically been adopted to shape the D_{it}. The best fitting achieved is shown in Fig. III.5, while the corresponding D_{it} profiles are plotted in Fig. III.6. In the latter, filled symbols corresponds to the portions of the D_{it} distributions that are actually scanned by the Fermi level as V_{GS} is swept from 1 V down to the value at which the drain leakage current floor masks any further gate-controlled I_D change (-0.1 V and -0.7 V for the uncapped and capped device, respectively). Open symbols are instead used for the remaining part of the D_{it} distributions. Simulations results shown in Fig. III.5 are sensitive to the filled-symbol part of D_{it} only. D_{it} distributions peaking at around midgap [65], but showing the same tail in the upper part of the gap as shown in Fig. III.6, would produce the same simulation outcomes shown in Fig. III.5.

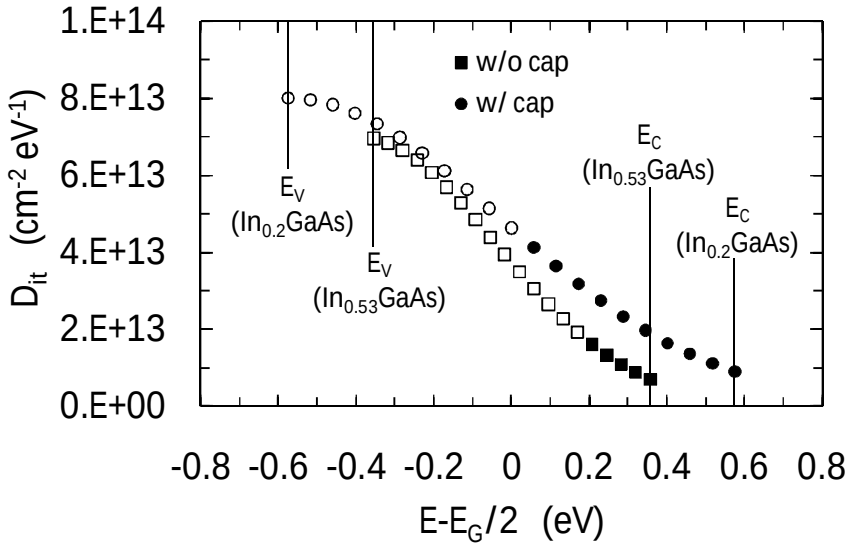

Fig. III.6: Density of donor-like interface traps assumed at the $In_{0.2}Ga_{0.8}As$ /ZrO_2 and at the $In_{0.53}Ga_{0.47}As$/ZrO_2 interface in the simulations shown in Fig. III.5 for the MOSFET with and without the $In_{0.2}Ga_{0.8}As$ cap, respectively.

As can be noted in Fig. III.5, an accurate description of both above- and sub-threshold I_D-V_{GS} behavior have been achieved for both device types.

Two simplifying assumptions implicit in the adopted D_{it} distributions are worth being pointed out.

1) We assumed interface traps to be donor-like throughout the bandgap also for $In_{0.2}Ga_{0.8}As$, whereas, in this material, the charge neutrality level is expected to be farther from E_C than for $In_{0.53}Ga_{0.47}As$ [58]. $Ga_2O_3(Gd_2O_3)/In_{0.2}Ga_{0.8}As$ MOS capacitors with free-moving Fermi level near E_C have actually been reported in [66], suggesting that acceptor-like traps in the upper part of the $In_{0.2}Ga_{0.8}As$ bandgap have a relatively-low density. Moreover, $In_{0.2}Ga_{0.8}As$ is used as the cap layer material (not as the channel material) in our devices. As will be shown in Fig. III.13, the Fermi level at the $ZrO_2/In_{0.2}Ga_{0.8}As$ interface of capped devices is still 0.2 eV below E_C at $V_{GS}=V_T$. Acceptor-like traps located closer to E_C (from E_C-0.2 eV to E_C) remain neutral for V_{GS} values up to V_T. These traps can not significantly affect SS and V_T, while they can only impact the high-current regime for $V_{GS}>V_T$.

2) Interface traps outside the bandgap are neglected for both uncapped and capped devices. Traps located above E_C are in particular expected to be acceptor-like. These traps can affect the device characteristics at gate voltages well above V_T, while having a negligible effect on SS and V_T (they are neutral until the Fermi level at the ZrO_2/InGaAs interface is raised above E_C).

On the other hand, at high V_{GS}, the drain current is strongly impacted by other parameters, such as interface mobility and source and drain series resistances. The errors introduced by the approximated modeling of these parameters can compensate that associated with the simplifying assumptions 1) and 2), allowing a good agreement between measurements and simulations to be achieved even in the high-current regime.

The main conclusions that we were able to draw from the I_D-V_{GS} fitting procedure (and that are not impacted by the approximations pointed out above) are as follows:

(i) D_{it} in the order of 10^{13} cm^{-2} eV^{-1} are required to match the SS in the devices under study;

(ii) adopting these D_{it} values automatically accounts for the negative V_T shift of uncapped MOSFETs with respect to capped ones, provided that dominant interface traps are assumed to be donor-like;

(iii) strong-inversion operation is allowed with $V_T<0.5$ V, owing to the assumed donor-like behavior of dominant interface traps.

In order to analyze the effect of interface traps more systematically, simplified, uniform interface-trap distributions have been adopted. This simplification does not limit generality of conclusions drawn, as far as the different effects of donor- and acceptor-like traps are concerned. Results are described in sections III.4.1 and III.4.2 for uncapped and capped MOSFET, respectively.

III.4.1 - Effects of Interface Traps in the MOSFETs Without Cap

Figure III.7 shows the simulated I_D-V_{GS} characteristics at V_{DS}= 0.05 V for a MOSFET without the $In_{0.2}Ga_{0.8}As$ cap for different densities of donor- (N_D) and acceptor-like (N_A) interface traps.

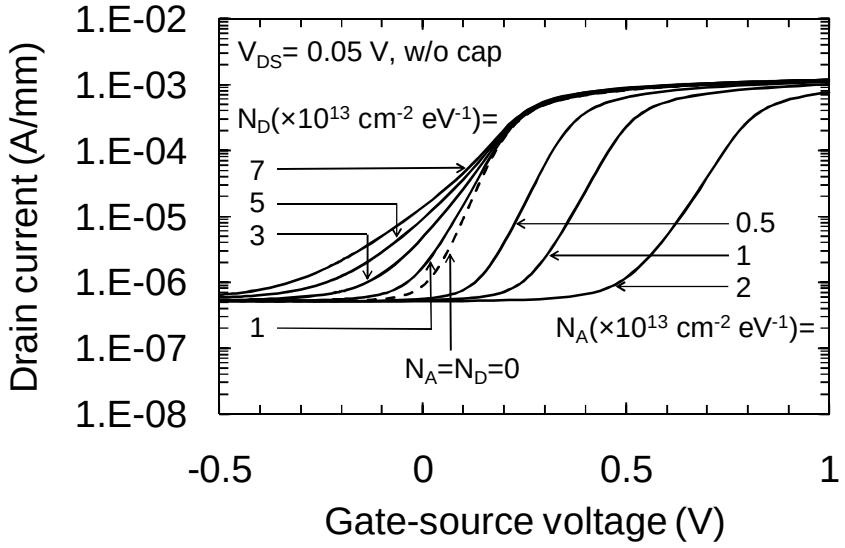

Fig. III.7: Simulated drain-current vs. gate-source-voltage characteristics at a drain-source voltage of 0.05 V for a MOSFETs without the $In_{0.2}Ga_{0.8}As$ cap for different, uniform donor-like (N_D) and acceptor-like (N_A) interface-trap distributions. The dashed curve refers the case of no interface traps.

As can be noted, donor-like traps impact the subthreshold characteristics by increasing SS. They instead leave V_T virtually unchanged. This can be understood with the aid of Figs. III.8 and III.9, showing the charged donor density along the $ZrO_2/In_{0.53}Ga_{0.47}As$ interface (Fig. III.8) and the electron density along a vertical cut in the middle of the gate (Fig. III.9) in the uncapped MOSFET for different V_{GS} values.Under strong-inversion conditions (V_{GS}≥0.15 V), the electron density is large (see Fig. III.9) and donor-like traps are almost all neutral (i.e., completely occupied) (see Fig. III.8**)**, so that they can not impact I_D. For this reason V_T does not change with increasing N_D, see Fig. III.7. The charged donor density is instead large for low V_{GS} (see Fig. 8), since the electron density in the channel is small (see Fig. III.9). Under these conditions, the larger N_D the larger the positive trapped charge and the higher I_D, this explaining the SS increase at increasing N_D shown in Fig. III.7.

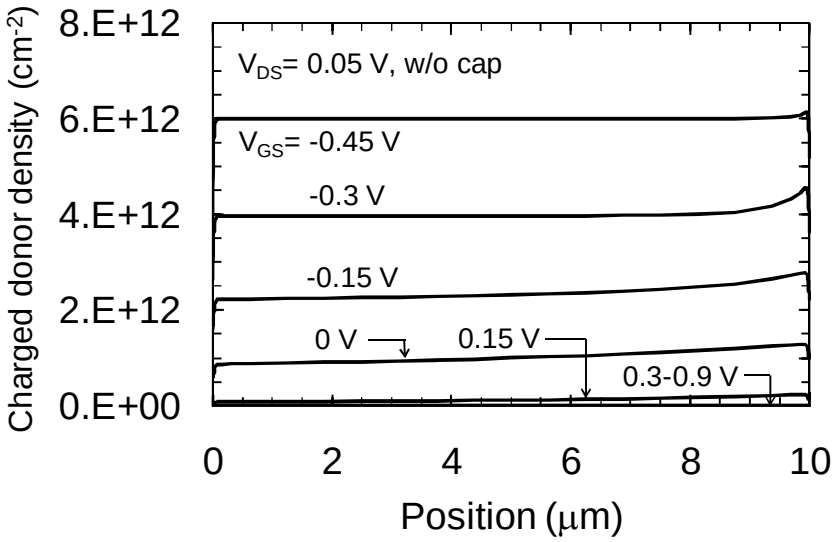

Fig. III.8: Charged donor density along the ZrO_2-$In_{0.53}Ga_{0.47}As$ interface in the MOSFET without the cap at a drain-source voltage of 0.05 V for different gate-source voltages.

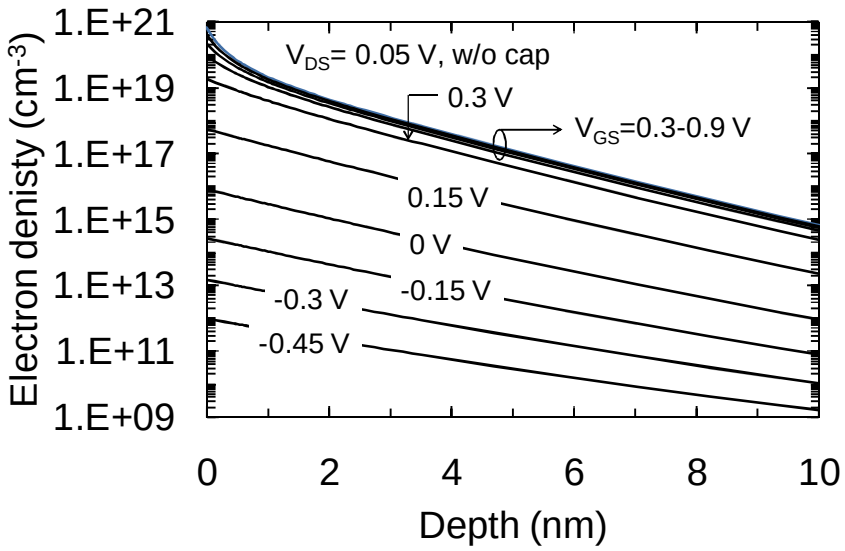

Fig. III.9: Electron density as a function of distance from the dielectric along a vertical cut in the middle of the gate in the MOSFET without the cap at a drain-source voltage of 0.05 V for different gate-source voltages.

On the other hand, increasing N_A increases SS and, at the same time, shifts V_T positively (see Fig. III.7). Acceptor-like traps are in fact neutral (unoccupied) under accumulation, this making I_D independent on their density. This regime is actually masked by the reverse leakage current in Fig. III.7, in the absence of which I_D curves for different N_A values would all tend to converge towards the same point at small V_{GS}. As V_{GS} is increased and the MOSFET is pushed towards inversion, acceptor-like traps charge up negatively. Under these conditions, the larger N_A, the larger the

negative trapped charge and the smaller I_D, thus explaining the positive V_T shift with increasing N_A. N_A values in the order of 10^{13} cm^{-2} eV^{-1} are required to reproduce measured SS values. As shown in Fig. III.7, these relatively-large N_A values would result in V_T values >0.5 V, that are much larger than the measured ones (see Fig. III.2).

III.4.2 - Effects of Interface Traps in the MOSFETs With Cap

Figure III.10 shows the simulated I_D-V_{GS} characteristics at V_{DS}= 0.05 V for a MOSFET with the $In_{0.2}Ga_{0.8}As$ cap for different densities of donor- (N_D) and acceptor-like (N_A) interface traps.

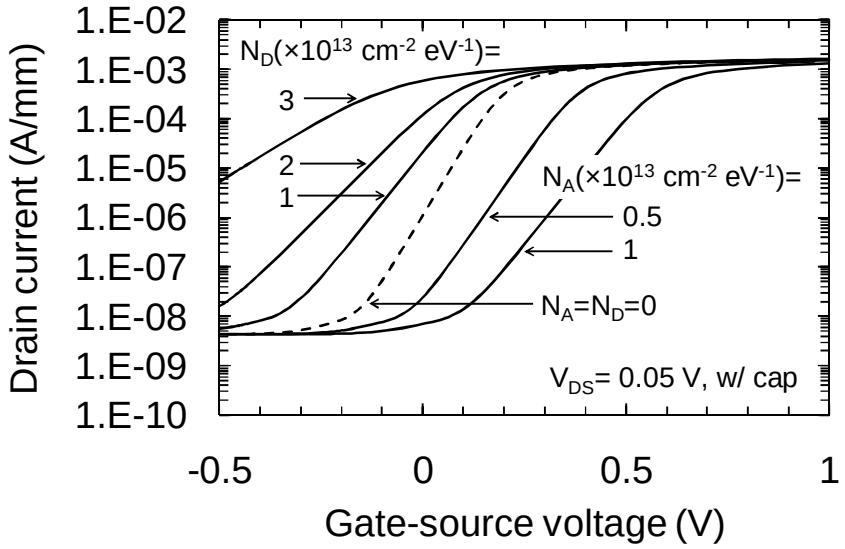

Fig. III.10: Simulated drain-current vs. gate-source-voltage characteristics at a drain-source voltage of 0.05 V for a MOSFETs with the $In_{0.2}Ga_{0.8}As$ cap for different, uniform donor-like (N_D) and acceptor-like (N_A) interface-trap distributions. The dashed curve refers to the case of no interface traps.

Differently from the case of uncapped MOSFETs, increasing N_D shifts V_T to smaller values (besides increasing SS like in uncapped devices). This effect can be explained with the aid of Figs. III.11 and III.12, showing the charged donor density along the $ZrO_2/In_{0.2}Ga_{0.8}As$ interface and the electron density along a vertical cut in the middle of the gate in the capped MOSFET for different V_{GS} values. As can be noted, traps that are located at the $ZrO_2/In_{0.2}Ga_{0.8}As$ interface continue, in this case, to be modulated by the V_{GS} change (see Fig.III.11) even when the channel at the $In_{0.53}Ga_{0.47}As/In_{0.2}Ga_{0.8}As$ interface has attained strong inversion (see Fig. III.12). This condition is illustrated by Fig. III.13, showing the simulated band diagram along the device depth under the gate for the two MOSFET types at the respective threshold voltages. As can be noted, the Fermi level (E_F) is close to E_C in the $In_{0.53}Ga_{0.47}As$ channel of the uncapped device, resulting in all neutralized donor-like interface traps. On the other hand, E_F is still ≈0.2 eV below E_C in the $In_{0.2}Ga_{0.8}As$ cap of

the capped MOSFET, this leading to residual positive trapped charge at the ZrO_2 interface. This mechanism explains the negative V_T shift observed experimentally in capped MOSFETs with respect to uncapped ones (see Fig. III.5).

From Fig. III.12, it can also be noted that the electron density at the $ZrO_2/In_{0.2}Ga_{0.8}As$ remains significantly smaller than that at the $In_{0.53}Ga_{0.47}As/In_{0.2}Ga_{0.8}As$ for V_{GS}<0.6 V. For higher V_{GS}, the electron-density values at the two interfaces become comparable. Owing to higher mobility, the electron current density continues to be higher at the $In_{0.53}Ga_{0.47}As/In_{0.2}Ga_{0.8}As$ interface, the latter thus functioning as the actual, buried channel of the device over the entire V_{GS} range considered.

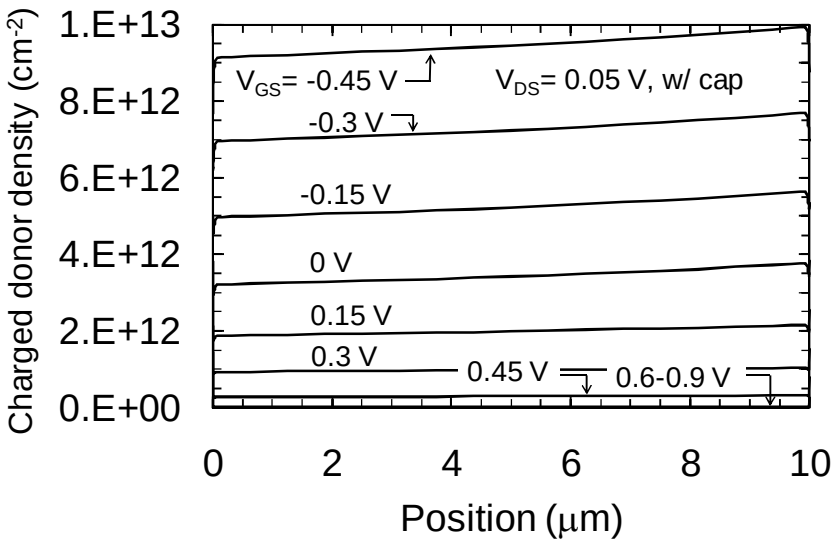

Fig. III.11: Charged donor density along the ZrO_2-$In_{0.2}Ga_{0.8}As$ interface in the MOSFET with the cap at a drain-source voltage of 0.05 V for different gate-source voltages.

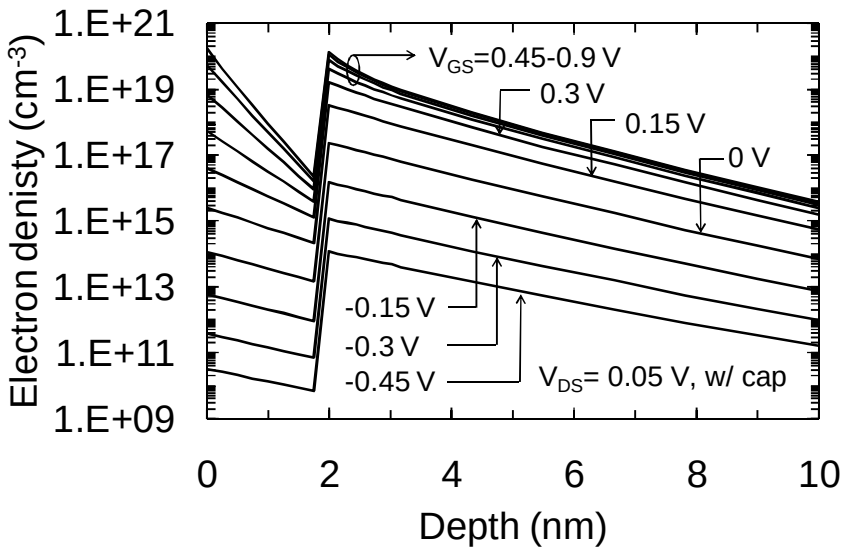

Fig. III.12: Electron density as a function of distance from the dielectric along a vertical cut in the middle of the gate in the MOSFET with the cap at a drain-source voltage of 0.05 V for different gate-source voltages.

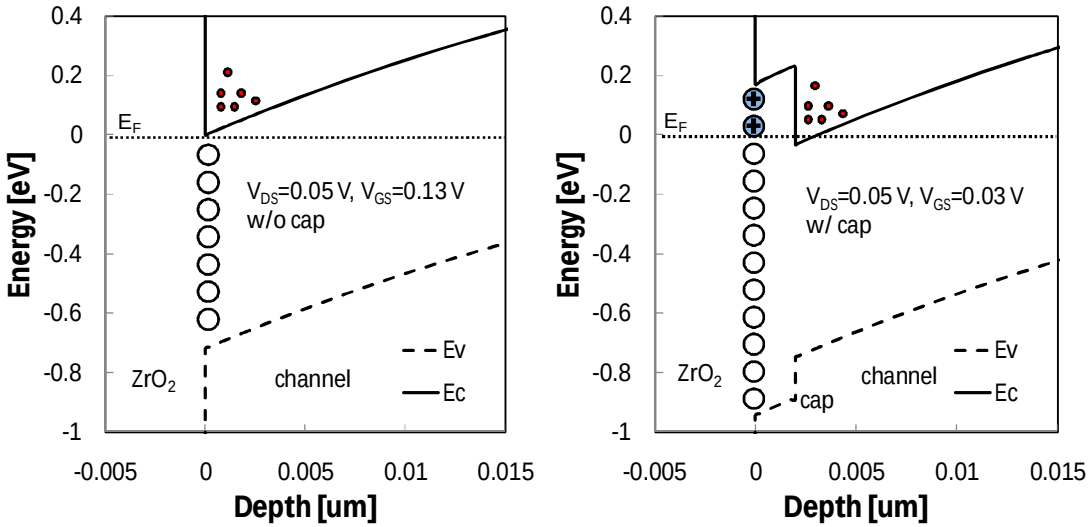

Fig. III.13: Simulated band diagram along device depth under the gate for the two MOSFET types (left: uncapped device, right: capped device) at the respective threshold voltages and sketch of corresponding charge state of the donor-like interface traps.

As far as acceptor-like traps are concerned, their behavior is similar to that exhibited in uncapped MOSFETs, i.e. both V_T and SS increase with increasing N_A. For the same N_A, the positive V_T shift is however larger than in the uncapped device (compare Figs. III.10 and III.7). This happens because traps located at the $In_{0.2}Ga_{0.8}As/ZrO_2$ interface continue to be modulated by the V_{GS} change, even when the channel at the $In_{0.53}Ga_{0.47}As/In_{0.2}Ga_{0.8}As$ interface has reached strong inversion (not shown for brevity). If (dominant) interface traps were acceptor-like traps in

the devices under consideration, inclusion of the $In_{0.2}Ga_{0.8}As$ cap would therefore shift V_T positively, which contrasts with what observed experimentally. On the contrary, as previously shown, donor-like interface traps can explain the experiments.

III.5 - Summary

We have analyzed the effects of interface traps in inversion-type n-channel InGaAs MOSFETs with ZrO_2 gate dielectric, by comparing measurements and numerical device simulations of the I_D-V_{GS} characteristics. Devices under consideration have two different epilayer structures, one with the ZrO_2 dielectric directly deposited onto the $In_{0.53}Ga_{0.47}As$ channel, the other with a 2-nm $In_{0.2}Ga_{0.8}As$ cap layer interposed.

Quantitative agreement between measurements and simulations has been achieved under the hypothesis that traps at the ZrO_2/InGaAs interface are donor-like. D_{it} values in the order of 10^{13} cm^{-2} eV^{-1} are in particular required to explain the measured subthreshold slopes. For these D_{it} values, donor-like interface traps can explain V_T values in the 0-0.15 V range as those measured in these devices, whereas acceptor-like traps would result in much larger V_T values (> 0.5 V).

The influence of donor-like and acceptor-like interface traps have systematically been analyzed for both uncapped and capped devices. Interface-trap effects in MOSFETs with the thin $In_{0.2}Ga_{0.8}As$ cap layer have been shown to be qualitatively different from those observed in standard MOSFETs (without cap layer). More specifically, increasing the donor-like trap density shifts V_T negatively in capped devices, while it leaves V_T unchanged in uncapped ones. As a result of this, donor-like interface traps can explain the V_T difference observed in MOSFETs with and without the cap.

Chapter IV: Semiconductor Stack Optimization for InGaAs Quantum Well MOSFETs Scaling

Properties of InGaAs buried channel quantum well MOSFETs affected by the barrier and buffer layers are analyzed in this chapter by numerical simulations to assist device engineering and optimization. The interplay between the charge neutrality level position at the barrier/dielectric interface and conduction band discontinuity at the barrier/channel interface is shown to critically impact the achievement of an enhancement mode device with full turn-on. A p-doped buffer is found to be a more suitable option than the standard unintentionally doped buffers to control short-channel effects.

Besides standard inversion-type MOSFET structures with a surface channel, implanted source and drain regions, and p-doped body [20],[67],[22],[68], buried channel quantum well MOSFETs have been proposed [15],[69],[28] to mitigate the degradation in channel mobility induced by the proximity to the gate dielectric [70].

The epilayer structure of these devices resembles that of typical InP HEMTs for which an InGaAs channel with a high In concentration is sandwiched between the higher bandgap barrier and buffer layers that confine channel electrons and physically separate them from the gate dielectric and substrate, respectively. Similar to Si MOSFETs, the gate stack structure exhibits a high-k gate dielectric grown, for instance, using ALD. However, the following two characteristics make InGaAs quantum well MOSFETs different from Si MOSFETs and InP HEMTs, respectively: (i) the presence of a barrier layer interposed between the high-k dielectric and the InGaAs channel, making the effects of interface traps on device behavior different from those characteristic of surface-channel MOSFETs; (ii) the stringent requirements of enhancement-mode operation and short-channel-effect control, making the unintentionally-doped InAlAs buffer typically adopted in InP HEMTs inadequate for the intended, digital applications of InGaAs MOSFETs. In this study, we use numerical device simulations to investigate aspects (i) and (ii), with the aim of providing

indications for device engineering and optimization. Devices used in this study were fabricated by University of Texas (Austin, TX, USA).

(i) In surface channel MOSFETs, the conducting channel is adjacent to the interface with the gate dielectric. When the interface trap densities are relatively high, which is typical of III.V MOSFETs, the interface charge neutrality level (E_{CNL}) should be as close to the semiconductor conduction band edge (E_C) as possible or even above it. In this case, a negative charge starts to build up at the interface only when the Fermi level rises above E_{CNL}, which occurs at a high gate bias when the conducting channel is already formed. In other words, the Fermi level is not pinned in the upper part of the channel bandgap and full turn-on is feasible. This is actually the case in inversion-type, surface channel MOSFETs with a high In mole fraction InGaAs channel [71]. In quantum well MOSFETs, however, the semiconductor materials of the barrier and channel are different, with the barrier material having a larger bandgap and, specifically, a higher conduction band edge than the channel material, so that the electrons are confined within the channel by the resulting conduction band discontinuity (ΔE_C). As shown below, the barrier layer, interposed between the gate dielectric and the channel, modifies the way interface traps influence the device characteristics, modifying the criteria for optimal barrier materials.

(ii) Unintentionally doped (UID) InAlAs buffers are typically adopted in InP HEMTs. Most reported InGaAs MOSFETs exhibit UID buffers similar to those of the InP HEMTs. The buffer impacts device parameters such us threshold voltage (V_T), subthreshold slope (SS), and off-state current (I_{OFF}). These parameters are of critical significance in InGaAs MOSFETs, which are intended for digital circuits. While the UID buffer is adequate for long channel MOSFETs, it is unclear whether it can still be an option for scaled devices. Our analysis suggests that a p-doped buffer (either uniformly or delta doped) can provide a better control over the short-channel effects, thus helping to achieve enhancement mode operation.

IV.1 - Device Structures

The baseline device structure adopted for this study is an InGaAs buried channel quantum well MOSFET with the following vertical structure: (i) ALD Al_2O_3 gate dielectric (4 nm), (ii) InP barrier (5 nm), (iii) $In_{0.7}Ga_{0.3}As$ channel (10 nm), (iv) $In_{0.52}Al_{0.48}As$ buffer (300 nm), and (v) semi-insulating InP substrate. Heavily doped (Si, $3x10^{19}cm^{-3}$) $In_{0.53}Ga_{0.47}As$ cap layers (20 nm), selectively removed from the gate region before Al_2O_3 deposition, act as carrier supply and source/drain contact layers. Channel, barrier, and buffer layers were not intentionally doped. The gate length (L_G) and width (W_G) are 20 μm and 600 μm, respectively. Fig. IV.1 is a sketch of the device cross section (UID buffer). More details about device fabrication are in reference [23].

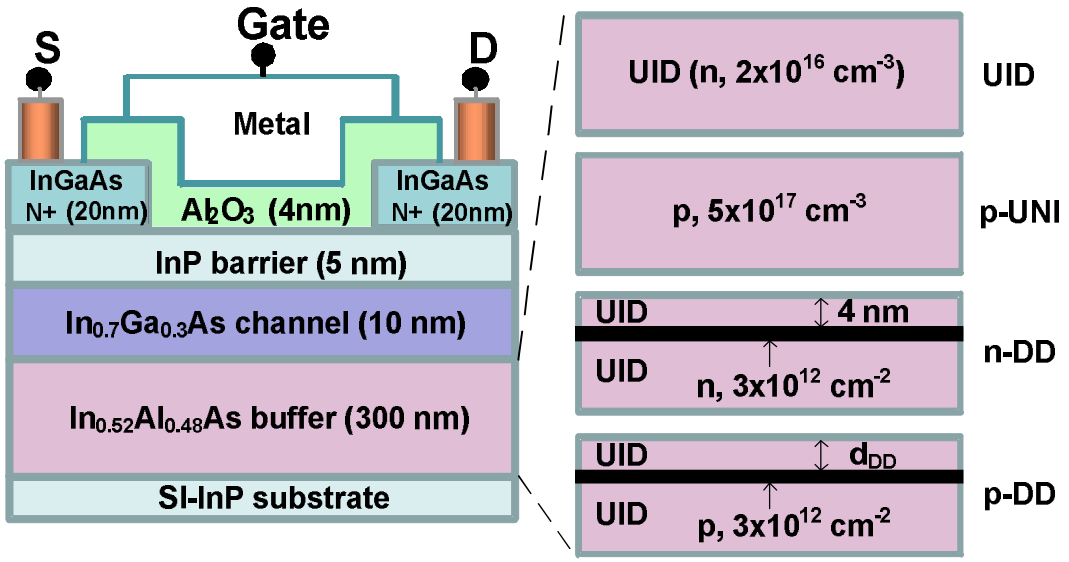

Fig. IV.1: Schematic cross section of InGaAs buried channel quantum well MOSFETs under study (not to scale).

Two-dimensional drift-diffusion numerical simulations were performed using the Sentaurus Device (Synopsys Inc.) [63] simulator. The adopted calibration procedure can be summarized as follows. 1) The drain leakage current is found to be a sensitive function of the buffer conductivity only. The unintentional buffer doping density has thus been adjusted, in order to match the measured leakage current level at two different drain-source voltages. 2) V_T and SS depend on (i) gate-stack material parameters, (ii) band-structure parameters of the different semiconductor layers, (iii) unintentional doping in the buffer, (iv) interface traps. Once (i) and (ii) have been fixed to literature values [72] and (iii) is set according to point 1),V_T and SS remain sensitive functions of the interface-trap distribution, only. The parameters defining a simplified, box-like interface-trap distribution have therefore been tuned so as to reproduce the experimental V_T and SS. 3) Having fixed V_T, I_D under above-threshold conditions is mainly a function of channel mobility. Parameters in the interface mobility model have therefore been used as fitting parameters to reproduce I_D under above-threshold conditions. A more detailed description of the simulation calibration procedure and the resultant fitting parameters can be found in Chapter V along with a comparison of the experimental and simulated data using the baseline device.

Two types of simulations were carried out in this work.

1) The baseline device structure was simulated for different E_{CNL} positions. E_{CNL} is defined so that, when the Fermi level E_F equals E_{CNL}, the dielectric interface has no net charge, whereas when $E_F>E_{CNL}$ or $E_F<E_{CNL}$, it becomes negatively or positively charged, respectively. For simplicity, we defined all traps energetically located below and above E_{CNL} to be donor-like and acceptor-like, respectively. E_{CNL} is a material property, with reported E_C-E_{CNL} values for InP in the 0.3-0.4 eV range [58],[73]. Here, we varied E_C-E_{CNL} over a wider range (0.1-0.5 eV), to let the different effects

associated with small and large E_C-E_{CNL} values emerge more clearly and to make conclusions of this analysis more general and applicable even to different barrier materials.

2) Modified device structures were simulated with different L_G values (and correspondingly scaled source and drain access regions) and/or different buffer options. The latter, illustrated in Fig. IV.1, include the following: a) unintentionally doped buffer (UID); b) p-type, uniformly doped buffer (p-UNI); c) n-type, delta-doped buffer (n-DD); and d) p-type, delta-doped buffer (p-DD). For the UID buffer, a 2×10^{16} cm^{-3} n-type doping density has been assumed, which allowed the experimental I_{OFF} to be reproduced by simulating the baseline devices [72]. In the p-UNI buffer, the assumed uniform p-type doping density is 5×10^{17} cm^{-3}. In the n-DD buffer, delta-doping dose and depth are 3×10^{12} cm^{-2} and 4 nm, respectively. For the p-DD buffer option, the delta-doping dose is 3×10^{12} cm^{-2}, while different depths of the delta-doping layer (d_{DD}) are considered.

IV.2 - Barrier

For the baseline device, Fig. IV.2 shows the simulated DC drain-current (I_D) vs. gate-source-voltage (V_{GS}) curves at the drain-source voltages (V_{DS}) of 0.05 V and 1 V for different E_{CNL} positions. The latter are defined as the energetic distances from the InP conduction band edge ($E_{C,bar}$). The conduction band profiles through the device depth (perpendicular to the substrate plane) are shown in Fig. IV.3 for $I_D=10^{-3}$ A and V_{DS}=0.05 V, along with the corresponding trap charge densities at the Al_2O_3-InP interface. As seen in Figs. IV.3(a)-(c), regardless of the $E_{C,bar}$-E_{CNL} value, the Fermi level (E_F) is approximately aligned to the conduction band edge in the InGaAs channel at the bias that corresponds to a near-threshold condition.

Consider the case of $E_{C,bar}$-E_{CNL}=0.3 eV. Since ΔE_C=0.3 eV, then $E_F \approx E_{CNL}$ at the interface. Because of the small band bending of the barrier and channel layers, E_F actually lies slightly below E_{CNL}(see Fig. IV.3(b)). As shown in Fig. IV.3(e), this leads to a small positive charge associated with the charged donor traps and a much smaller negative charge due to charged acceptor traps.

For $E_{C,bar}$-E_{CNL}=0.5 eV, E_F tops E_{CNL} by ≈0.2 eV at the surface (see Fig. IV.3(c)). In this case, the acceptor charge density exceeds the donor one (see Fig. IV.3(f)). As shown in Fig. IV.2, this results in a more positive V_T compared to the previous case. Larger $E_{C,bar}$-E_{CNL} values can eventually prevent full turn-on by inducing Fermi-level pinning.

Finally, for $E_{C,bar}$-E_{CNL} =0.1 eV, E_F is ≈0.25 eV below E_{CNL} at the surface (see Fig. IV.3(a)), resulting in a high density of charged donor traps and a negligible density of charged acceptor traps (see Fig. IV.3(d)). As shown in Fig. IV.2, this shifts V_T towards negative values. If the $E_{C,bar}$-E_{CNL} values are too low, obtaining an enhancement mode device becomes difficult.

The E_C-E_{CNL} values reported for InP are in the 0.3-0.4 eV range [58],[73], which represents optimal trade-off values allowing for both complete device turn-on and positive V_T. This makes InP particularly suitable as a barrier material for InGaAs quantum well MOSFETs. Channel

confinement can be further improved by using a composite $InP/In_{0.52}Al_{0.48}As$ barrier, with beneficial effects on device mobility and drive current [23].

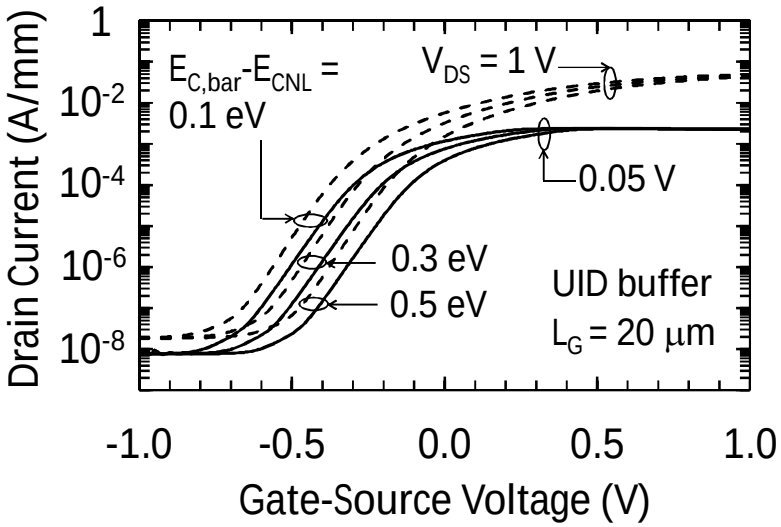

Fig. IV.2: Simulated DC drain current (I_D) vs. gate source voltage (V_{GS}) curves at a drain source voltage (V_{DS}) of 0.05 V (solid lines) and 1 V (dashed lines) for different charge neutrality level positions ($E_{C,bar}$-E_{CN}). The simulated device is the baseline MOSFET structure (UID buffer, L_G=20 μm).

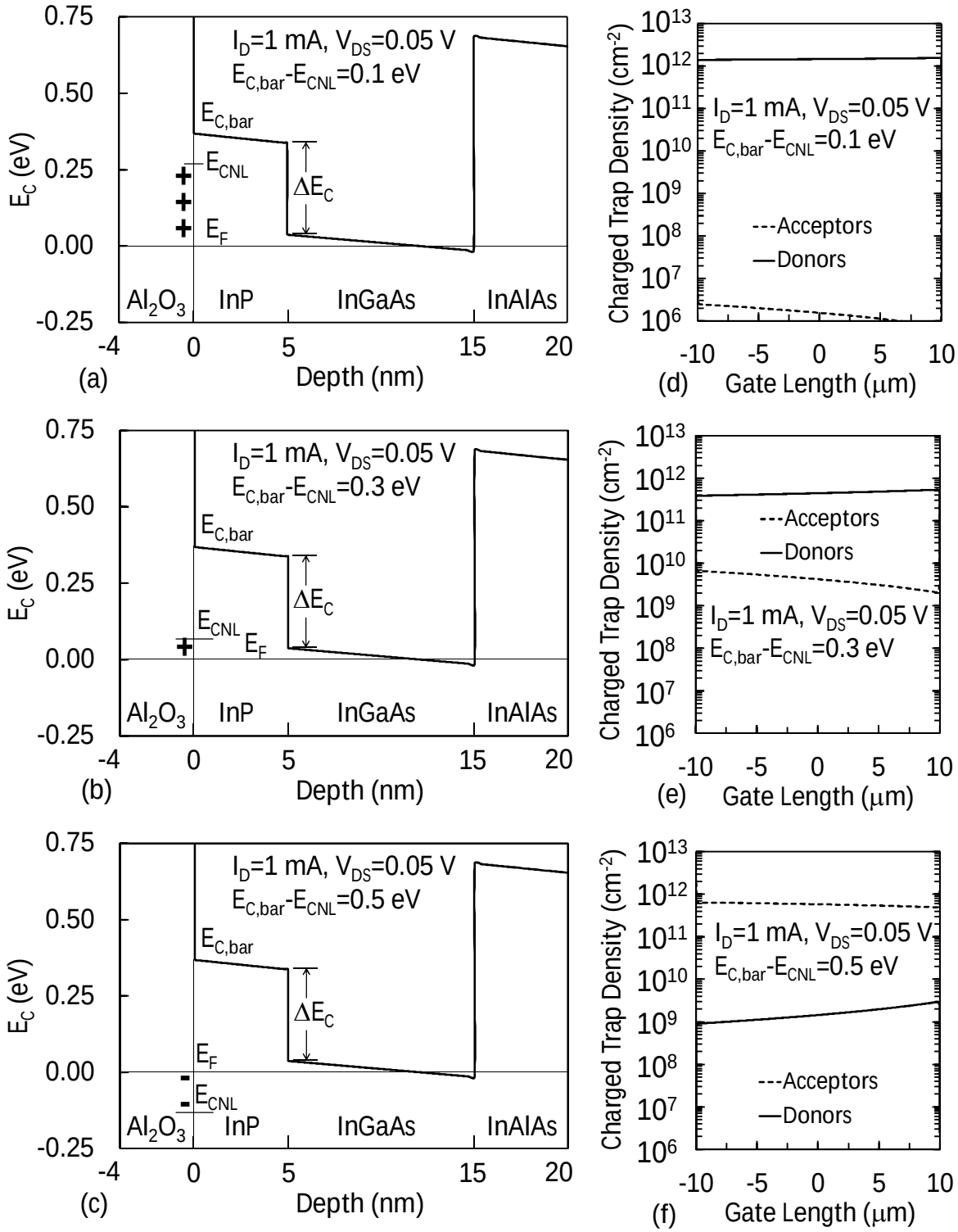

Fig. IV.3: Simulated conduction band edge (E_C) profile along device depth (left figures) in the middle of the gate and corresponding charge trap densities at the Al_2O_3-InP interface (right figures) for different charge neutrality level positions ($E_{C,bar}$-E_{CNL}) at I_D=1 mA and V_{DS}=0.05 V. The simulated device is the baseline MOSFET structure (UID buffer, L_G=20 μm).

IV.3 - Buffer

The I_D-V_{GS} characteristics of the baseline MOSFETs (Fig. IV.1) with different gate lengths were simulated first, Fig. IV.4. The minimum L_G is limited to 100 nm and the device structure is kept planar, so that adopted simulation models retain their validity for all presented data. For shorter L_G, ballistic transport starts playing a role. Moreover, in quantum-well FinFETs, the barrier layer is present beneath the top gate only, while the lateral channels are directly formed at the high-k/InGaAs interface [69]. Both InP/Al_2O_3 and InGaAs/Al_2O_3 interfaces would therefore influence channel transport. For these reasons, extending our analysis to planar devices with shorter L_G (100-10 nm) or to FinFET devices would require a dedicated calibration procedure using a sub-100-nm or FinFET device as the experimental reference device. In these and subsequent simulations, $E_{C,bar}$-E_{CNL} is set to 0.3 eV. As expected, when L_G decreases, the increase in I_{ON} is accompanied by detrimental side effects, such as negative V_T shift, higher SS, and DIBL. In fact V_T has a strong dependence on V_{DS} (≈54 mV/V) even for L_G=20 μm. Obviously, this cannot be ascribed to the short-channel effects. On the contrary, it is related to the combined effect of the interface trapped charge modulation and UID buffer depletion [74]. As L_G becomes shorter, the "classical" DIBL effect comes into play, enlarging the $\Delta V_{GS}/\Delta V_{DS}$ ratio in the subthreshold regime (see Fig. IV.4). The most critical aspect to consider, however, is the effect of L_G scaling on V_T. As seen in Fig. IV.4, scaling L_G down to 100 nm turns the MOSFET into a depletion mode device with a negative V_T of about -0.45 V.

Enhancement-mode behavior can be recovered by using a p-type doped buffer, which leads to an upward band shift in the buffer. This is shown in Fig. IV.5 comparing the I_D-V_{GS} characteristics of 100-nm MOSFETs with UID, n-DD, and p-UNI buffers (see Fig. IV.1). Note that the device with the p-UNI buffer has a positive V_T (≈0.2 V). Moreover, it shows the SS (from 120 to 90 mV/dec) and $\Delta V_{GS}/\Delta V_{DS}$ ratio (from 140 to 45 mV/V) are less than with UID buffer. The trade-off is a decrease in I_{ON} by a factor of ≈2. With the goal of maximizing I_{ON}, one might consider using an intentionally doped n-type buffer, such as the n-DD buffer shown in Fig. IV.1. However, as the results in Fig. IV.5 suggest, the negative V_T shift and degrading subthreshold behavior make this option impractical.

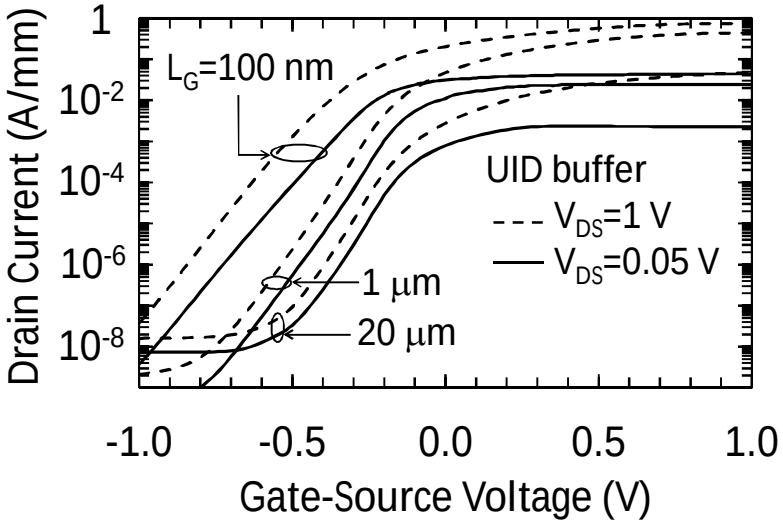

Fig. IV.4: Simulated DC drain current (I_D) vs. gate source voltage (V_{GS}) curves at a drain source voltage (V_{DS}) of 0.05 V (solid lines) and 1 V (dashed lines) for different gate lengths (L_G) in the UID-buffer device.

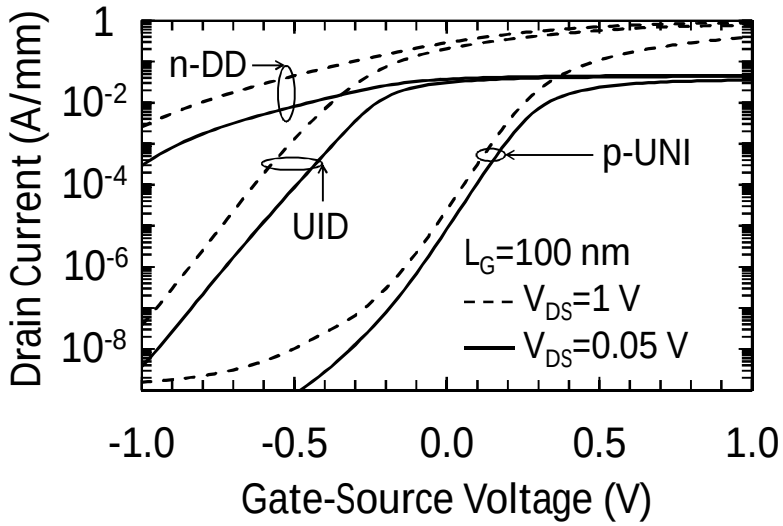

Fig. IV.5: Simulated DC drain current (I_D) vs. gate source voltage (V_{GS}) curves at a drain source voltage (V_{DS}) of 0.05 V (solid lines) and 1 V (dashed lines) for 100 nm MOSFETs having UID, p-UNI, and n-DD buffer.

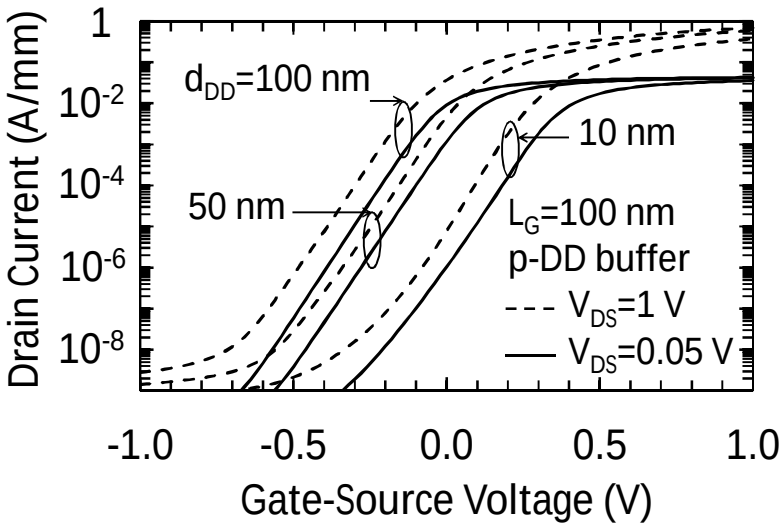

Fig. IV.6: Simulated DC drain current (I_D) vs. gate source voltage (V_{GS}) curves at a drain source voltage (V_{DS}) of 0.05 V (solid lines) and 1 V (dashed lines) for 100 nm MOSFETs having a p-DD buffer with different delta-doping depths (d_{DD}).

To minimize the expected degradation in channel mobility related to impurity scattering, a p-type delta doping can be adopted instead of a uniform p-type doping, which imparts the same beneficial effects on the V_T and sub-V_T characteristics by properly optimizing the delta-doping dose and distance from the channel (d_{DD}). This is illustrated in Fig. IV.6, which compares the I_D-V_{GS} characteristics of 100-nm MOSFETs with a p-DD buffer characterized by different d_{DD} values (and the same delta-doping dose of 3×10^{12} cm^{-2}).c Note that V_T increases with decreasing d_{DD}; this dependency can be tuned within the range of 0-0.25 V by changing d_{DD} in the 50-10 nm range while maintaining a similar SS (92-94 mV/dec), $\Delta V_{GS}/\Delta V_{DS}$ (65-90 mV/V), and I_{ON}.

IV.4 - Summary

Our numerical simulations point to specific features of barrier and buffer layers in InGaAs quantum well MOSFETs that distinguish these devices from surface channel MOSFETs and InP HEMTs. Unlike surface channel MOSFETs, quantum well MOSFETs can tolerate a dielectric/semiconductor interface with a relatively deep charge neutrality level E_{CNL} without jeopardizing full turn-on. On the other hand, a barrier material characterized by an extremely small $E_{C,bar}$-E_{CNL} difference can be detrimental to enhancement mode device operation. In short-channel devices, a p-doped buffer is found to provide better threshold voltage and short-channel effect control than a conventional unintentionally doped buffer derived from InP HEMTs.

Chapter V: Limitation in Split-CV Technique for Electron Mobility Extraction

The accuracy of the split-CV mobility extraction method is analyzed in buried-channel InGaAs MOSFETs with Al_2O_3 gate dielectric and InP barrier, through a "simulated experiment" procedure using two-dimensional numerical device simulations preliminarily calibrated against experimental IV and CV curves. The different error sources limiting the method accuracy are pointed out. It is suggested that, as a result of these errors, the split-CV method can appreciably underestimate the actual channel mobility in these devices, with an error >20% and >50% on peak and high-V_{GS} mobility, respectively. The method should therefore not be adopted for accurate mobility measurement in this operating regime, but only as a fast response technique providing a conservative estimation of channel mobility. Moreover, the method provides mobility values that rapidly drop below the peak value for decreasing V_{GS}. It is shown that this behavior can be an artifact of the extraction method, that may mask physical mechanisms causing real mobility drop with decreasing channel carrier density like Coulomb scattering mechanisms. This poses limitations to the adoption of split-CV mobility as a reference for mobility model assessment in this operating regime. The proposed methodology can be applied to other III-V field-effect transistors, including both heterostructure-based and inversion-mode devices.

The great interest in developing InGaAs MOSFETs is due to intrinsic InGaAs potential, if compared with Si, for larger drive current at same off-state current and power-supply voltage, enabled by the higher electron mobility and source injection velocity [6]. The enhanced surface-phonon and interface-charge scattering associated with the high-k/III-V interface [70] can however degrade mobility in actual InGaAs MOSFET structures, possibly jeopardizing the potential for logic performance improvement over Si-channel devices. Accurate mobility measurement is thus of great importance in InGaAs MOSFETs, to comparatively evaluate the different device concepts and/or processing options and to guide device design and optimization.

In this regard, buried-channel quantum-well MOSFETs [15],[69],[23],[75], where a thin semiconductor barrier layer is interposed between the high-k gate dielectric and the undoped InGaAs channel, are the device structures that can more effectively minimize mobility degradation with respect to values typically achievable in InP HEMTs developed for RF applications. The buried-channel concept has been applied to inversion-type MOSFETs as well, leading, also in this case, to mobility improvement over surface-channel devices [76].

The split-CV method is a fast and simple technique that has extensively been adopted to measure the effective mobility in Si MOSFETs [77]. Several error sources have however been shown to limit the method accuracy when applied to Si MOSFETs with ultrathin high-k dielectrics [78]. These include interface-trap charge, weak-inversion channel resistance, gate leakage current, and source and drain series resistances. On the other hand, state-of-the-art InGaAs MOSFETs are still characterized by significantly larger interface-trap densities and source/drain resistances compared to their Si counterparts. It is therefore expected that at least these two factors can affect the accuracy of the split-CV mobility extraction when applied to InGaAs MOSFETs. The impact of interface-trap charge and source/drain parasitic resistances have indeed been pointed out in InGaAs [79],[80] and Ge [81] inversion-type surface-channel MOSFETs. It is important to extend these studies on split-CV mobility extraction accuracy to buried-channel devices, where the presence of the thin barrier layer can in principle change the impact of errors already pointed out, as well as originate extra errors, by contributing an additional capacitance between gate and short-circuited source/drain terminals that is not taken into account by the mobility extraction method.

In this chapter, we analyze the impact of the different errors that limit the accuracy of split-CV mobility extraction in buried-channel InGaAs MOSFETs having Al_2O_3 gate dielectric and InP barrier. Devices used in this study were fabricated by University of Texas (Austin, TX, USA).

Two-dimensional (2D), drift-diffusion simulations preliminarily calibrated against experimental IV and CV curves are to this purpose adopted, providing a “consistency” test for the method. More specifically, the mobility obtained by applying the split-CV method to simulation outcomes “as they were measured data” is compared to that used as an input to simulations. Corrections to the method that are able to reduce the discrepancy between the above two quantities are searched for and applied. This allows the different error sources having a role for these devices to be pointed out and separated from each other. Only once suitable corrections are applied for all of the relevant error sources, consistency between extracted and input mobility is fully recovered.

The above methodology is general and can be applied to other III-V field-effect transistors, comprising both heterostructure-based devices with more complex layer structures and inversion-type MOSFETs. Errors identified by our analysis are related to (i) charge in non-channel semiconducting layers, (ii) access resistances, (iii) drift-diffusion channel transport and (iv) drain leakage current. All of these effects can potentially impact split-CV channel mobility extraction accuracy in any heterostructure-based field-effect transistor, whereas effects (ii)-(iv) can be present in surface-channel, inversion-type MOSFETs as well.

It will be shown that, as a result of these errors, the split-CV method can appreciably underestimate channel mobility under above-threshold conditions. The method can nevertheless be adopted within the device optimization loop as a fast response technique providing a conservative estimation for channel mobility. Second, the split-CV method provides mobility values that rapidly drop below the peak value for decreasing V_{GS}. This behavior can be an artifact of the extraction method, that may mask physical mechanisms causing real mobility drop with decreasing channel carrier density like Coulomb scattering mechanisms. This poses limitations to the adoption of split-CV mobility as a reference for mobility model assessment in this operating regime.

V.1 - Devices and Model Calibration

The proposed methodology for assessing split-CV mobility accuracy is mainly based on numerical device simulations and might in principle be applied to a MOSFET that is only simulated. Our analysis will however focus on a specific, real device structure. This will be described in this section along with the procedure adopted to fit experimental IV and CV curves. The purpose of reproducing the characteristics of actual devices as accurately as possible by means of simulations is to show that error sources that will subsequently be put into evidence and corresponding mobility inaccuracies are similar to those characterizing real devices.

Test devices adopted for this study are buried-channel InGaAs MOSFETs fabricated by University of Texas (Austin, TX, USA), having the following top-to-bottom structure under the TaN gate metal: (i) ALD-deposited, Al_2O_3 gate dielectric (4 nm), (ii) InP barrier (5 nm), (iii) $In_{0.7}Ga_{0.3}As$ channel (10 nm), (iv) $In_{0.52}Al_{0.48}As$ buffer (300 nm), (v) semi-insulating InP substrate. Heavily doped (Si, $3x10^{19}$ cm^{-3}) $In_{0.53}Ga_{0.47}As$ cap layers (20 nm), selectively removed from the gate region prior to Al_2O_3 deposition, act as carrier supply and source/drain contact layers. Channel, barrier, and buffer layers are undoped. Gate length (L_G) and width (W_G) are 20 μm and 600 μm, respectively. A sketch of the device cross section is shown in Fig. V.1. More details on device fabrication can be found in [23].

Figure V.2 shows, for a representative device, experimental static drain-current (I_D) vs. gate-source-voltage (V_{GS}) characteristics at a drain-source voltage (V_{DS}) of 0.05 V and 0.5 V. Figure V.3 shows the experimental high-frequency AC gate capacitance per unit area ($C_{G\text{-}SD}$) as a function of V_{GS}, as obtained by the split-CV method, i.e. with the source and drain contacts short-circuited to each other and the body contact left floating. Simulated curves reported in Figs. V.2 and V.3 (solid lines) will be commented below.

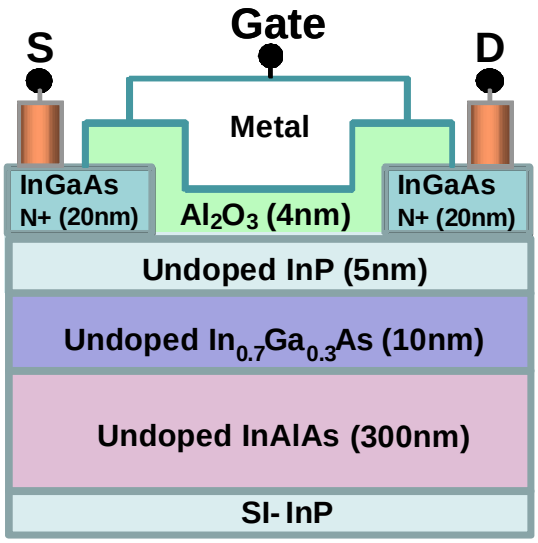

Fig. V.1: Schematic cross section of buried-channel InGaAs MOSFETs under study (not to scale).

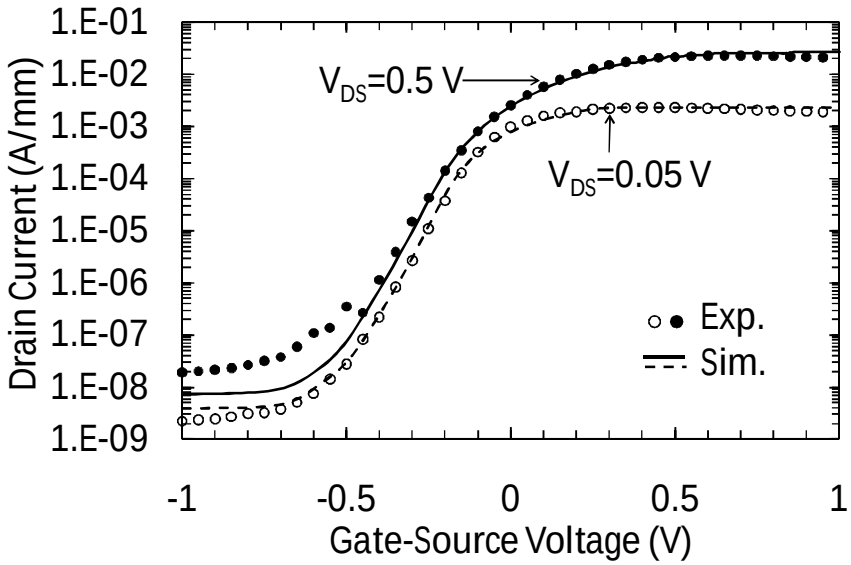

Fig. V.2: Experimental (symbols) and simulated (solid lines) DC drain-current (I_D) vs. gate-source-voltage (V_{GS}) curves for two drain-source voltages (V_{DS}).

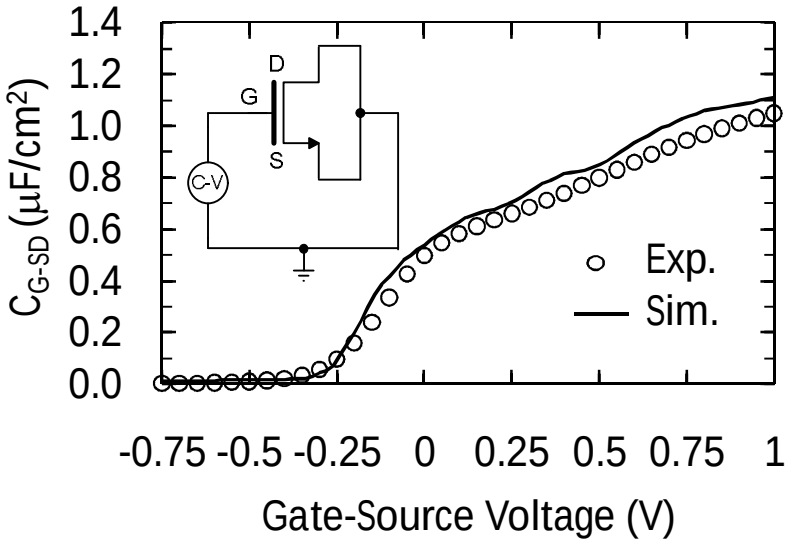

Fig. V.3: AC experimental (symbols) and simulated (solid line) gate-capacitance (C_{G-SD}) vs. gate-source-voltage (V_{GS}) curves at 1 MHz. Source and drain contacts are short-circuited to each other, while the body contact is left floating (see inset).

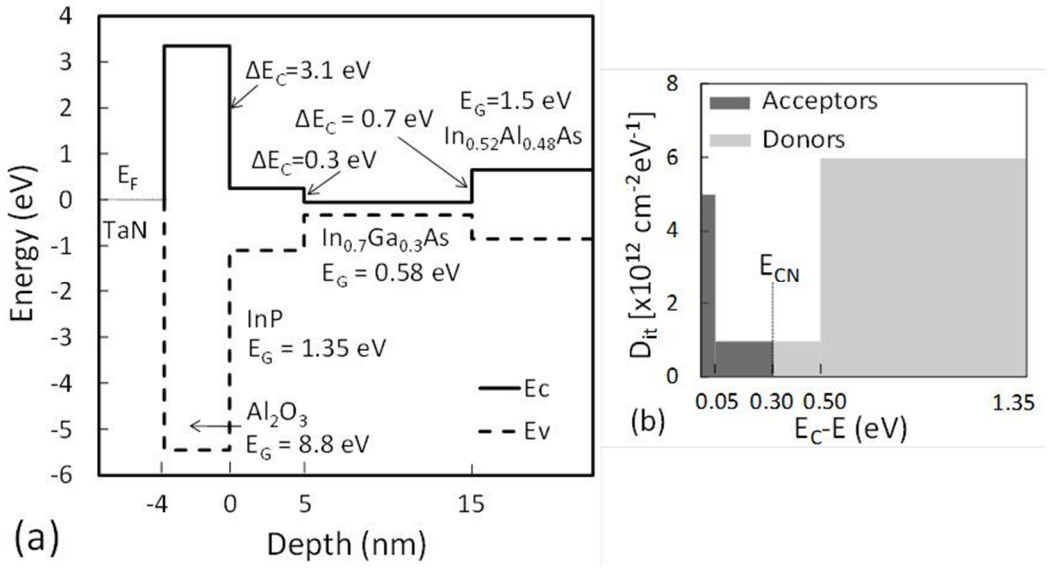

Fig. V.4: (a) Band alignment along the device depth. (b) Simplified energy distribution adopted for the interface-trap density (D_{it}) at the Al_2O_3/InP interface.

2D drift-diffusion numerical simulations have been carried out using the device simulator Sentaurus Device (Synopsys Inc.) [63]. Nominal values have been adopted for all geometrical dimensions. Literature values have been adopted for bandgap and electronic affinity of semiconductor layers [82], yielding the band alignment along the device depth illustrated in Fig. V.4(a). TaN work function (Φ_M) has been set to 0.65 eV [83]. The assumed Al_2O_3 relative

permittivity (ε_{ox}) is 7.8, deriving from the experimental EOT value of 2 nm [23] and corresponding to an oxide capacitance (C_{ox}) of 1.73 $\mu F/cm^2$ for an oxide thickness of 4 nm. It is worth pointing out that experimental and simulated CV curves in Fig. V.3 do not tend to C_{ox} at high V_{GS}, but to a lower value, corresponding to series connection of C_{ox} and barrier capacitance. Source and drain contact resistances (R_C) have been set in agreement with TLM measurements (R_C=0.85 Ωmm). A simplified, box-like energy distribution has been adopted for interface traps at the Al_2O_3/InP interface, see Fig. V.4(b). Traps are defined to be acceptor-like from the conduction-band edge (E_C) to the charge-neutrality level (E_{CNL}) and donor-like from E_{CNL} to the valence-band edge (E_V). The simulator's model for interface mobility degradation has been adopted to force a simplified, power-law dependence of channel mobility (μ_n) on transverse electric field (E_t), i.e.

$$\mu_n^{-1} = \mu_{peak}^{-1} + \left(a \cdot E_t^{-b}\right)^{-1}, \qquad (V.1)$$

where μ_{peak}, a, and b have been used as fitting parameters. The simple mobility model (V.1) was used to facilitate parameter extraction and analysis across the operating range. Drain leakage current is governed, in the device under study, by parallel conduction between source and drain through the InAlAs buffer; it has been modeled by assuming a weak n-type unintentional doping in the buffer (N_{DB}).

Simulation models have been calibrated against experimental IV curves shown in Fig. V.2. After a preliminary analysis of the IV curve sensitivity to model parameters, quantitative fitting has been achieved as follows.

1) The drain leakage current (V_{GS}<-0.5 V) is a sensitive function of the buffer conductivity only. N_{DB} has thus been adjusted, in order to approximately match the measured leakage current level at the two V_{DS} values.

2) Threshold voltage (V_T) and subthreshold slope (SS) depend on (i) gate-stack material parameters (Φ_M and ε_{OX}), (ii) band-structure parameters of the different semiconductor layers, (iii) unintentional doping in the buffer, (iv) interface traps. Once (i) and (ii) are fixed to literature values as stated above [23],[82],[83] and (iii) is set according to point 1), V_T and SS remain sensitive functions of the interface-trap distribution, only. The parameters defining the box-like interface-trap distribution shown in Fig. V.4(b) have therefore been tuned so as to reproduce experimental V_T and SS.

3) Having fixed V_T, I_D under on-state conditions is mainly a function of channel mobility. Peak channel mobility (μ_{peak}) and parameters a and b, controlling mobility degradation at increasing V_{GS}, have therefore been used as fitting parameters to reproduce I_D for V_{GS}>V_T.

As shown in Figs. V.2 and V.3, applying procedure 1)-3) above has allowed IV and CV characteristics of these devices to be reproduced with satisfactory accuracy. Values adopted for fitting parameters are listed in Table V.1.

Model	Parameters
Band alignment	See Fig. V.4(a)
Interface traps	See Fig. V.4(b)
Channel electron mobility	μ_{peak}=4900 $cm^2/(Vs)$ a=5x10^{50} $cm^2/(Vs)$ b=9.3
Buffer unintentional doping	N_{DB}=2x10^{16} cm^{-3}

Table V.1: Values for Fitting Parameters.

The above fitting procedure contains several approximations and does not lead to univocal determination of model parameters, especially in the subthreshold regime, where the roughness of the assumed interface-trap distribution has a major impact. However, it is important to point out that fitting the experimental characteristics is not strictly necessary to our goal and it has been pursued in order to make conclusions of our "simulated-experiment" approach as representative of actual devices as possible. As explained in the next section, mobility extraction accuracy will be tested by comparing mobility curves extracted from simulated data with that adopted as an input to simulations. Despite not strictly necessary to our goal, the fitting of the experimental characteristics has however been pursued in order to make conclusions of our "simulated-experiment" approach as representative of actual devices as possible.

V.2 - Test of Mobility Extraction Accuracy

Mobility values ($\mu_{EXT,exp}$) obtained by applying the split-CV method to experimental data are shown in Fig. V.5 as a function of $V_{GT}=V_{GS}-V_T$ (where V_T=0.09 V). Following [78], $\mu_{EXT,exp}$ is obtained as

$$\mu_{EXT,exp} = \frac{L_G}{W_G} \cdot \frac{I_{D,exp}}{V_{DS} Q_{CV,exp}}, \qquad (V.2)$$

where: V_{DS}=0.05 V, $I_{D,exp}$ is the measured drain current (Fig. V.2, experimental curve for V_{DS}=0.05 V), and $Q_{CV,exp}$ is the channel electron charge per unit area estimated by integrating the experimental CV curve (Fig. V.3, experimental curve). As can be noted, $\mu_{EXT,exp}$ exhibits a peak of ≈4200 cm^2/Vs at V_{GT}=0.15 V and maintains itself >1000 cm^2/Vs up to strong on-state conditions (V_{GT}≈1 V).

In Fig. V.5, other two mobility curves are plotted as a function of V_{GT}. One is the mobility ($\mu_{EXT,sim}$) obtained by applying the split-CV method to the simulated IV and CV data in place of the measured ones. $\mu_{EXT,sim}$ is specifically calculated as

$$\mu_{EXT,sim} = \frac{L_G}{W_G} \cdot \frac{I_{D,sim}}{V_{DS} Q_{CV,sim}}, \qquad (V.3)$$

where: V_{DS}=0.05 V, $I_{D,sim}$ is the simulated drain current (Fig. V.2, simulated curve for V_{DS}=0.05 V), and $Q_{CV,sim}$ is the channel electron charge per unit area estimated by integrating the simulated CV curve (Fig. V.3, simulated curve). Not surprisingly, owing to the good agreement between simulated and experimental IV and CV curves shown in Figs. V.2 and V.3, $\mu_{EXT,sim}$ and $\mu_{EXT,exp}$ are in good agreement with each other. A maximum deviation of about 30% is present in correspondence of the mobility peak, mainly due to the discrepancy between simulated and experimental I_D in the same V_{GT} range.

The last mobility curve $\mu_{IN,sim}$ shown in Fig. V.5 is obtained from the mobility μ_n adopted as input to simulations shown in Figs. V.2 and V.3. μ_n depends on the local transverse electric field according to (V.1); thus, in principle, it varies both along channel length and thickness. Position dependence along the channel length is negligible, owing to the small V_{DS} value adopted and long gate length (L_G=20 μm). Position dependence along the channel thickness has however to be accounted for, the usual sheet charge approximation not being applicable to the 10-nm-thick channel region. Plotted $\mu_{IN,sim}$ values have therefore been obtained, for each V_{GS}, by averaging μ_n with respect to channel thickness along a vertical cut in the middle of the channel. Electron density (n) has been used as a weight function, in order to weigh μ_n values in terms of their contribution to current density. $\mu_{IN,sim}$ has thus been calculated as

$$\mu_{IN,sim} = \frac{\int \mu_n n dy}{\int n dy}, \qquad (V.4)$$

where both integrals are extended over the channel thickness.

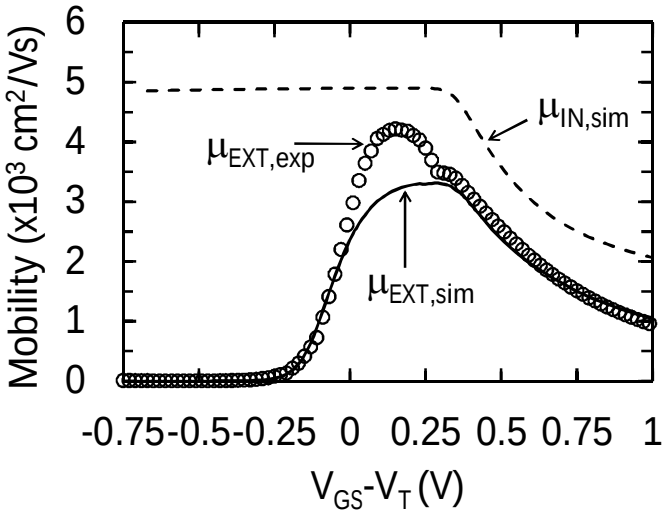

Fig. V.5: Mobility extracted by applying the split-CV method to experimental IV and CV curves ($\mu_{EXT,exp}$), compared to mobility extracted by applying the split-CV method to simulated IV and CV curves ($\mu_{EXT,sim}$) and mobility imposed as input to simulations ($\mu_{IN,sim}$).

As can be noted in Fig. V.5, $\mu_{IN,sim}$ deviates substantially from the mobility obtained with the split-CV method either applied to measured ($\mu_{EXT,exp}$) or simulated ($\mu_{EXT,sim}$) data. To our purposes, it is particularly noteworthy the fact that $\mu_{IN,sim}$ and $\mu_{EXT,sim}$ differ from each other. Regardless of whether simulations incorporating $\mu_{IN,sim}$ as an input are able to fit real device characteristics or not, a perfectly accurate extraction method, when applied to simulated IV and CV data, should provide mobility values that agree with those used as input of simulations themselves. The discrepancy between $\mu_{IN,sim}$ and $\mu_{EXT,sim}$ is, in other words, an indication of the different errors limiting the accuracy of the split-CV mobility. More specifically, the latter is found to underestimate the channel mobility $\mu_{IN,sim}$ by >20% and >50% at peak ($V_{GT}\approx0.15$ V) and high-V_{GT} ($V_{GT}=1$ V) conditions, respectively. It is also worth noting that, for $V_{GT}<0$ V, the split-CV method provides mobility values that rapidly decrease for decreasing V_{GT}. However, this behavior is not correlated with $\mu_{IN,sim}$ at all, the latter being constant in this V_{GT} range.

V.3 - Error Sources

In this section, the different errors affecting split-CV mobility are analyzed by means of simulations and corresponding corrections are looked for and applied to extracted mobility $\mu_{EXT,sim}$ until consistency with input mobility $\mu_{IN,sim}$ is fully recovered.

V.3.1 - Barrier, Buffer, and Interface Charge

A first quantity in (V.3) to look at, as it can contribute to mobility inaccuracy, is $Q_{CV,sim}$. It is intended to provide the electron charge in the channel per unit area (Q_{ch}) and it is obtained by integrating the simulated $C_{G\text{-}SD}(V_{GS})$ curve shown in Fig. V.3. $Q_{CV,sim}$ incorporates however spurious contributions that are not related to Q_{ch}. These come from the charge (per unit area) supplied by source/drain contacts to barrier (Q_{bar}) and buffer (Q_{buf}) layers, as well as to traps at the Al_2O_3/InP interface (Q_{tr}). The latter may not respond to the high-frequency AC stimulus applied during CV simulations (and measurements), but they do accumulate electrons in response to the quasi-static V_{GS} sweep [78]. $Q_{CV,sim}$ is plotted as a function of V_{GT} in Fig. V.6(a) and compared to quantities Q_{ch}, and Q_{bar}, as obtained from simulation outcomes by integrating the electron density over the channel and barrier thickness respectively. The difference ($Q_{CV,sim}$-Q_{ch}-Q_{bar}), also reported in Fig. V.6(a), must be ascribed to extra charge contributions associated with interface traps and, for V_{GT}<-0.4 V, with the buffer layer.

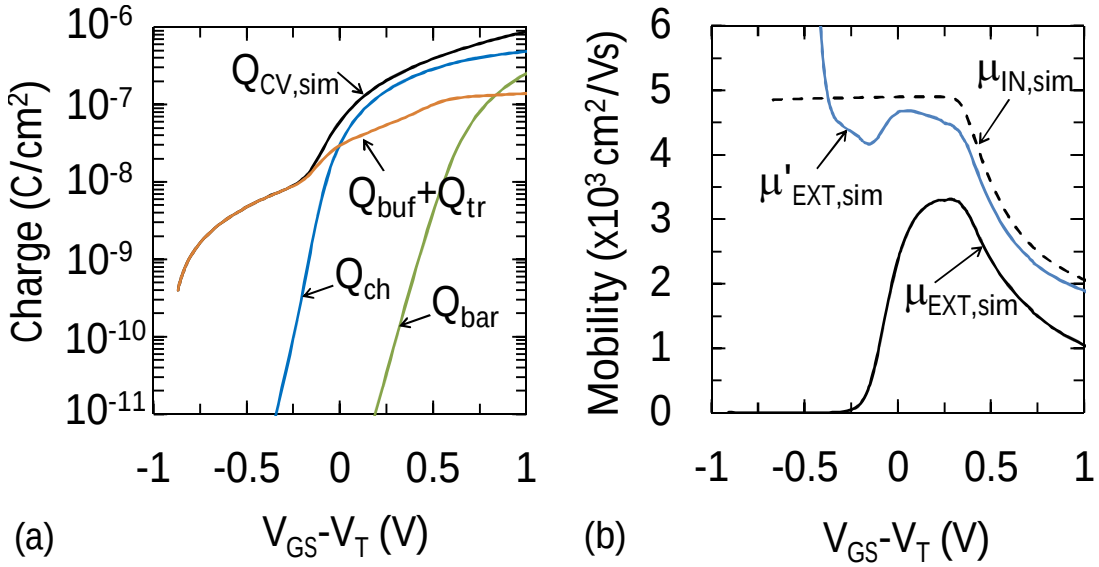

Fig. V.6: (a) Integral of the simulated CV curve ($Q_{CV,sim}$) as a function of $V_{GT}=V_{GS}-V_T$, compared to charge-per-unit-area contributions of channel (Q_{ch}), barrier (Q_{bar}), Al_2O_3/InP interface plus buffer ($Q_{tr}+Q_{buf}$). (b) Mobility imposed as input to simulations ($\mu_{IN,sim}$), compared to mobility extracted by applying the split-CV method to simulated IV and CV curves ($\mu_{EXT,sim}$) and to mobility corrected for the spurious charge contributions ($\mu'_{EXT,sim}$).

As can be noted from Fig. V.6(a), Q_{ch}<$Q_{CV,sim}$ over the entire V_{GT} range. $Q_{CV,sim}$ is a rough approximation for Q_{ch} for 0.1 V<V_{GT}<0.75 V, where, in fact, the discrepancy between $\mu_{EXT,sim}$ and $\mu_{IN,sim}$ remains <50% (see Fig. V.5). $Q_{CV,sim}$ is instead dominated by ($Q_{tr}+Q_{buf}$) for V_{GT}<-0.15 V. Moreover, Q_{bar} becomes comparable with Q_{ch} for V_{GT}>0.75 V, as the barrier layer begins to be populated by electrons. Simultaneous correction for errors associated with all spurious charge

contributions can be achieved by using the channel charge Q_{ch} in place of $Q_{CV,sim}$ in (V.3). Making this yields the corrected mobility

$$\mu'_{EXT,sim} = \frac{L_G}{W_G} \cdot \frac{I_{D,sim}}{V_{DS} Q_{ch}} . \qquad (V.5)$$

The effect of this correction is shown in Fig. V.6(b), where $\mu'_{EXT,sim}$ is compared to $\mu_{IN,sim}$ and $\mu_{EXT,sim}$. As can be noted, $\mu'_{EXT,sim} > \mu_{EXT,sim}$ since $Q_{ch} < Q_{CV,sim}$. However, the applied correction reduces the discrepancy from $\mu_{IN,sim}$ for $V_{GT} > -0.4$ V only. In particular, the steep $\mu_{EXT,sim}$ roll-off from its peak to almost zero for decreasing V_{GT} is almost completely removed, indicating that such behavior was induced by the spurious charge contributions to $Q_{CV,sim}$ not related to the channel, and in particular to Q_{trap} and Q_{buf} (Q_{bar} being negligible for $V_{GT} < 0.5$ V). For $V_{GT} < -0.4$ V, instead, $\mu'_{EXT,sim}$ largely overestimates $\mu_{IN,sim}$. This is due to the fact that, at these voltages, $I_{D,sim}$ stops decreasing for decreasing V_{GT} and saturates at the buffer leakage current floor (see Fig. V.2), while Q_{ch} still decreases rapidly (see Fig. V.6(a)). This discrepancy will be corrected lastly.

It is worth pointing out that charge contributions Q_{buf} and Q_{bar} are considered to produce "errors" in our analysis since our goal is to assess channel mobility. Parallel conducting channels through barrier and buffer layers can actually be important parasitic effects in buried-channel III-V MOSFETs. Ensemble device mobility, accounting for all possible charge conducting paths from source to drain, is the ultimate device transport metric. When interested in this quantity, transport through barrier and buffer should not be considered an "error"; rather, an undesirable side-effect of the layer structure which degrades the overall device mobility. Being able to extract channel mobility (by purifying it from Q_{buf} and Q_{bar} effects) is however crucial during the device/technology development phase, since it allows the effects of optimization efforts on channel charge confinement properties (e.g., as a result of barrier and buffer material choice, possible use of composite barrier, buffer doping, etc.) and on channel mobility (e.g., as a result of interface quality improvement, optimized surface-to-channel distance, etc.) to be separated from each other. In the final, optimized device, where non-channel parallel conduction has been minimized, the overall device mobility should be as close as possible to channel mobility.

V.3.2 - Series Resistances

A known, possible error source in mobility extraction is related to source and drain series resistances ($R_{S,D}$), reducing the drain-source voltage actually applied to the channel [78]. Moreover, R_S affects also the gate voltage used to calculate the total charge from the CV curve. The impact of $R_{S,D}$ can be corrected by replacing V_{DS} with the quantity ($V_{DS} - 2 \times R_{S,D} \times I_{D,sim}$) in (V.5). We actually used the contact resistance R_C ($R_C = 0.85\ \Omega$ mm) in place of the total series resistance $R_{S,D}$, since the

effect of the remaining part of $R_{S,D}$ (i.e. the access resistance between contact and intrinsic channel) is implicitly taken into account by the next correction step in section V.3.3. The corrected mobility ($\mu''_{EXT,sim}$) is therefore given by

$$\mu''_{EXT,sim} = \frac{L_G}{W_G} \cdot \frac{I_{D,sim}}{(V_{DS} - 2R_C I_{D,sim})Q_{ch}} . \qquad (V.6)$$

In (V.6), the effect of source resistance on V_{GS} values used for charge calculation is implicitly corrected, since $Q_{CV,sim}$ has already been replaced, at this stage of the correction procedure, by Q_{ch}, that is obtained from the actual charge in the channel provided by simulations. $V'_{DS}=V_{DS}-2\times R_C\times I_{D,sim}$ is compared to V_{DS} in Fig. V.7(a), while the effect of contact resistance correction is illustrated by Fig. V.7(b), showing $\mu''_{EXT,sim}$, $\mu'_{EXT,sim}$, and $\mu_{IN,sim}$ as a function of V_{GT}. As can be noted, thanks to contact resistance correction, consistency between $\mu''_{EXT,sim}$ and $\mu_{IN,sim}$ has almost completely been recovered for $V_{GT}>0$ V.

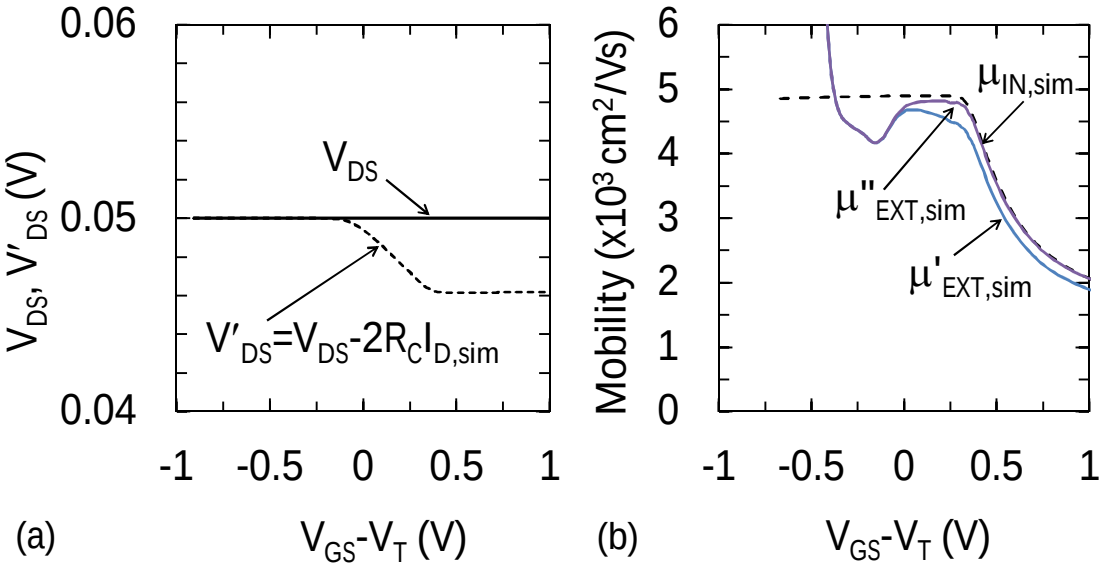

Fig. V.7: (a) Drain-source voltage externally applied to contacts (V_{DS}), compared to drain-source voltage corrected for contact-resistance voltage drop (V'_{DS}). (b) Mobility imposed as input to simulations ($\mu_{IN,sim}$), compared to mobility corrected for the spurious charge contributions ($\mu'_{EXT,sim}$) and to mobility corrected for both spurious charge contributions and contact resistances ($\mu''_{EXT,sim}$).

V.3.3 - Drift-Diffusion Transport

In Fig. V.7(b), $\mu''_{EXT,sim}$ still appreciably deviates from $\mu_{IN,sim}$ for $V_{GT}<0$ V, indicating that additional errors affect mobility extraction in this voltage range. Diffusion adds up to and progressively replaces drift transport as V_{GS} is decreased into sub-threshold regime [3]. All split-CV

mobility expressions reported up to this point (equations (V.2), (V.3), (V.5), and (V.6)) are valid under the assumption of pure drift transport and linear electric potential distribution over the channel length. The quantity V_{DS}/L_G approximates the channel electric field in (V.2), (V.3) and (V.5). The same applies to quantity $(V_{DS}-2\times R_C\times I_{D,sim})/L_G$ in (V.6). Drift-diffusion transport can be accounted for by formally replacing the electric field with the gradient of the electron quasi-Fermi potential ($d\varphi_n/dx$) [3]. $d\varphi_n/dx$ can in fact be expressed as $d\varphi_n/dx=d\varphi/dx+[(kT)/(qn)]\cdot dn/dx$ (where k is the Boltzmann constant, q is the elementary charge, and all quantities are given in absolute value), incorporating both drift and diffusive transport contributions. Mobility expression (V.6) can in particular be corrected for diffusion contribution to channel transport, by replacing the quantity $(V_{DS}-2\times R_C\times I_{D,sim})/L_G$ with $d\varphi_n/dx$. The mobility expression ($\mu'''_{EXT,sim}$) incorporating this further correction reads

$$\mu'''_{EXT,sim} = \frac{1}{W_G}\cdot\frac{I_{D,sim}}{\frac{d\varphi_n}{dx}Q_{ch}}\,. \qquad (V.7)$$

The impact of this correction is shown in Fig. V.8(b), comparing $\mu'''_{EXT,sim}$, $\mu''_{EXT,sim}$, and $\mu_{IN,sim}$. $d\varphi_n/dx$ has been extracted from simulations and is compared to the following quantities in Fig. V.8(a): (i) the approximated electric field $V'_{DS}/L_G=(V_{DS}-2\times R_C\times I_{D,sim})/L_G$, (ii) the electric field $d\varphi/dx$ obtained from simulations, and (iii) the diffusive term $[(kT)/(qn)]\cdot dn/dx$. As noted in Fig. V.8(a), accurate drift-diffusion transport description can not be neglected for $V_{GT}<0$ V, where the quantity V'_{DS}/L_G ceases to be a good approximation for the driving field. In this V_{GT} range, V'_{DS}/L_G significantly exceeds both the electric field $d\varphi/dx$, that rapidly decreases for decreasing V_{GT} as a consequence of reduced current and associated voltage drop along the channel, and, to a lesser extent, the quasi-Fermi potential gradient $d\varphi_n/dx$, that includes the diffusion contribution to channel current. As a result, mobility obtained by the split-CV method using V'_{DS}/L_G as driving field underestimates the actual channel mobility. On the other hand, as shown in Fig. V.8(b), accounting for drift-diffusion transport extends the V_{GT} range, where corrected mobility $\mu'''_{EXT,sim}$ is agreement with $\mu_{IN,sim}$, down to -0.4 V.

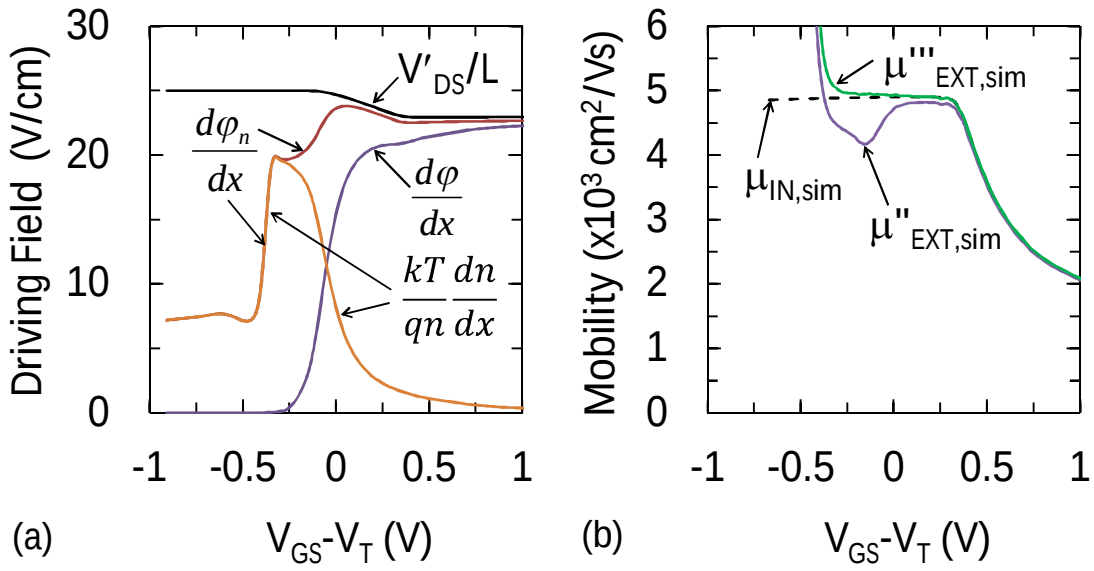

Fig. V.8: (a) Approximated channel electric field (V'_{DS}/L_G) compared to actual electric field ($d\varphi/dx$), diffusion-related effective driving field $[(kT)/(qn)]\cdot dn/dx$, and total driving field $d\varphi_n/dx=d\varphi/dx+[(kT)/(qn)]\cdot dn/dx$. (b) Mobility imposed as input to simulations ($\mu_{IN,sim}$), compared to mobility corrected for the spurious charge contributions and series resistances ($\mu''_{EXT,sim}$) and to mobility corrected for spurious charge contributions, series resistances, and drift-diffusion transport ($\mu'''_{EXT,sim}$).

V.3.4 - Buffer Conduction

Finally, buffer conduction strongly influences I_D at V_{GT}<-0.4 V. As a result, $I_{D,sim}$ does not scale down with decreasing V_{GS} (see Fig. V.2) as the channel charge Q_{ch} instead does (see Fig. V.6(a)). Application of the split-CV method in this operating region is not of practical interest if channel mobility is the parameter to be extracted. The method neither yields buffer mobility, since the drain current is dominated by buffer conduction but the total charge contains the contributions of both buffer (Q_{buf}) and interface traps (Q_{tr}) (see Fig. V.6(a)). As a result, mobility values extracted by means of either experimental ($\mu_{EXT,exp}$) or simulated method ($\mu_{EXT,sim}$) are close to zero in this bias regime (see Fig. V.5). On the other hand, as already mentioned in section V.3.1, correcting for actual channel charge Q_{ch} the denominator of mobility expressions (V.5)-(V.7), while keeping the terminal current $I_{D,sim}$ at the numerator leads to strong mobility overestimation in this V_{GT} range (see Figs. V.6(b), 7(b), and 8(b)). This inconsistency can be eliminated, by replacing the terminal drain current $I_{D,sim}$ in (V.7) with the integral of the electron current density over the channel thickness (I_{ch}). In this way, only the channel current is accounted for, while buffer leakage current, that is not related to Q_{ch}, is disregarded. The resulting mobility expression reads:

$$\mu^{*}_{EXT,sim} = \frac{1}{W_G} \cdot \frac{I_{ch}}{\frac{d\varphi_n}{dx} Q_{ch}} . \qquad (V.8)$$

I_{ch} is compared with $I_{D,sim}$ in Fig. V.9(a), while the effect of the applied correction is illustrated by Fig. V.9(b), showing $\mu^{*}_{EXT,sim}$, $\mu'''_{EXT,sim}$, and $\mu_{IN,sim}$ as a function of V_{GT}. As can be seen in Fig. V.9(a), I_{ch} continues to scale down with decreasing V_{GT} even for V_{GT}<-0.4 V similarly to Q_{ch} (see Fig. V.6(a)). As shown in Fig. V.9(b), $\mu^{*}_{EXT,sim}$ and $\mu_{IN,sim}$ are virtually superimposed to each other over the entire V_{GS} range considered, suggesting that no further error source appreciably affects mobility extraction in these devices.

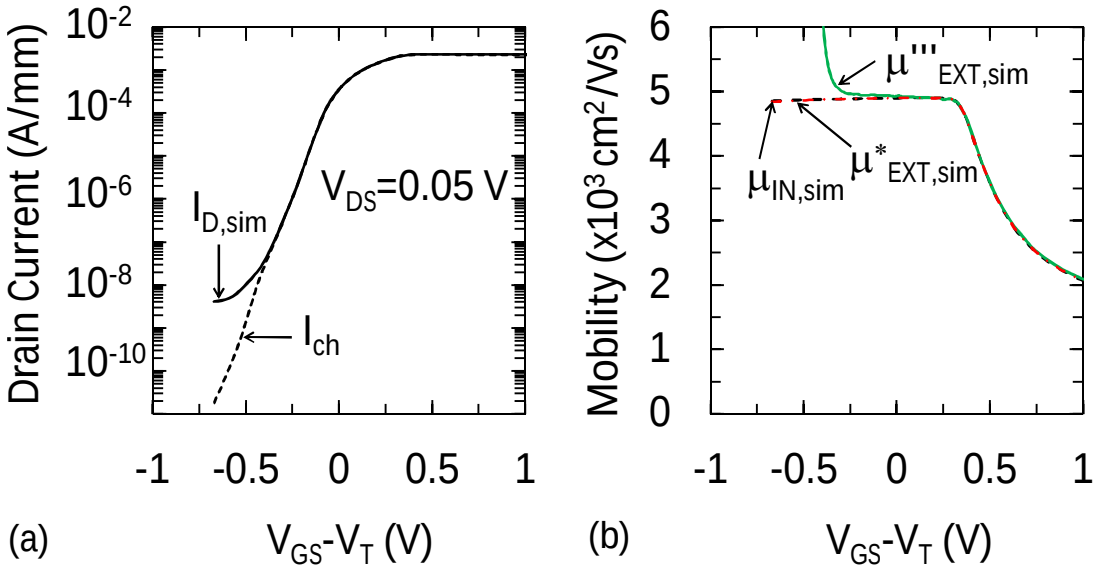

Fig. V.9: (a) Simulated terminal drain current ($I_{D,sim}$) compared to integral of electron current density over the channel thickness (I_{ch}). (b) Mobility imposed as input to simulations ($\mu_{IN,sim}$), compared to mobility corrected for spurious charge contributions, series resistances, and drift-diffusion transport ($\mu'''_{EXT,sim}$) and to mobility corrected for spurious charge contributions, series resistances, drift-diffusion transport, and buffer conduction ($\mu^{*}_{EXT,sim}$).

Another possible error source affecting mobility extraction is gate leakage current, leading to I_D [78] and gate capacitance roll-off [80] at high V_{GS} as a result of channel electron tunneling through the thin gate dielectric. In our devices gate current is still 3-order-of-magnitude smaller than I_D at the maximum V_{GT} of 1 V, but this may not be the case in different devices or technologies. Applying the proposed mobility accuracy analysis to these cases is however not straightforward, as it requires gate tunneling effects to be accounted for in simulations both for DC and small-signal AC calculations.

It is finally worth highlighting that all corrections applied to the split-CV method in the above analysis rely on quantities obtained from device simulations, except for correction of contact

source/drain resistances that can be extracted from measurements. At this stage we are not able to propose a correction procedure based on all-measurable quantities. Corrections have nevertheless been applied because they serve as steps of the method consistency test, allowing the different error sources and their impact on extracted mobility to be pointed out.

V.5 - Summary

We have tested the consistency of the split-CV mobility measurement method in implant-free, buried-channel InGaAs MOSFETs with Al_2O_3 gate dielectric and InP barrier, through the following "simulated experiment" procedure: 1) the mobility has been calculated starting from the simulated IV and CV curves "as they were experimental data"; 2) the so-obtained mobility has been compared to the mobility assumed as an input to simulations; 3) the discrepancy between these two quantities can be attributed to the inaccuracies of the extraction method, and corrections have been looked for and applied to the mobility extraction formula, till consistency between input and extracted mobility has been obtained.

Preliminarily to applying the above procedure, simulations have been calibrated against measured characteristics, so that the outcomes of the accuracy test can be regarded as indicative (also quantitatively) of mobility measurements from real devices.

Errors that have been found to affect the split-CV mobility extraction method are associated with (i) spurious electron charge contributions in the barrier, at the Al_2O_3/InP interface, and in the buffer, (ii) source and drain series resistances, (iii) inaccurate channel transport description, (iv) buffer drain leakage current.

As a result of these errors, it is suggested that the split-CV mobility method can appreciably underestimate the actual channel mobility even under above threshold conditions, where it is typically regarded as a reliable measurement technique. The error is in our case >20% and >50% on peak mobility ($V_{GT}\approx0.15$ V) and high-V_{GS} mobility ($V_{GT}=1$ V), respectively. It can be adopted within the device optimization loop as a fast response technique providing a conservative mobility estimation.

For $V_{GT}<0.15$ V, the split-CV method provides mobility values that rapidly decrease for decreasing V_{GS}. According to our simulated split-CV experiment, this behavior is an artifact of the extraction method, mainly related to error (i) above. In actual split-CV experiments, this effect can mask physical mechanisms causing real mobility drop with decreasing channel carrier density, like Coulomb scattering mechanisms. This poses limitations to the adoption of split-CV extracted mobility values as a reference for mobility model assessment in this operating regime.

Chapter VI: Interface Trap Characterization

This chapter is organized in two main sections. In the first section a new generalized technique for interface-trap extraction is presented. The new method combines together theory of two well known methods, Terman and high-low frequency, and helps to overcome limitations of each method itself. More specifically has been developed a fitting procedure. that automatically extracts the interface-trap profile in the bandgap and determines the value of the oxide capacitance along with the fitting of the measured capacitance. The method has been applied to Si/SiO_2 and InGaAs/$Al2O_3$ capacitors showing reliable results in terms of interface traps densities, oxide capacitance and CV curves fitting.

In the second section we studied the electrical properties of traps in the interfacial layer that inevitably results between the silicon substrate and the high-k material in the fabrication of the gate stack of high-k based Si-logic devices. Devices under study were grown on a wafer processed with a slant etch technique that provides a continuously scaled SiO_2 interfacial layer. Once verified the good quality of slant etch process, trap have been characterized by means of charge pumping and by trap spectroscopy by charge injection and sensing. Moreover an independent validation of the trap parameters is provided by gate-leakage simulation reproducing the experimental characteristics.

Section A: Generalized High-Low Frequency CV Technique for Interface-Trap Characterization

Historically, the poor quality of the dielectric interface has been the major obstacle to the development of III-V MOSFETs [55]. High interface trap densities (D_{it}) cause Fermi-level pinning preventing control on the charge carriers in the channel and degrade metrics of MOSFETs such as mobility, threshold voltage and sub-threshold slope [35],[15],[36],[37],[38],[39],[23],[40], [41],[42],[43], [44],[45],[46],[20],[47],[48],[52],[53],[16],[56].

Method	**Terman** *Measure D_{it} by stretch-out in high frequency CV curve*	**High-low frequency** *Difference in high and low frequency CV curves attributed to C_{it}*	**Conductance** *Evaluate the conductive losses due to traps interaction with bands*	***Equivalent admittance*** *Fitting CV and GV using equivalent circuit*
Pros	Requires only one CV curves	Straightforward	Most sensitive and reliable	Large energy range at a single temperature
Cons	Need true high frequency CV Require simulated ideal CV Large error in $E_T(V_G)$	Need true high low frequency CVs $E_T(V_G)$ very sensitive to C_{ox}	Cumbersome Energy range limited to conductance peak movement $E_T(V_G)$ depends on traps cross section	Minority carriers generation-recombination, border traps and tunnel conductance not known (fitting parameters)

Table VI.1: Summary of the main CV based D_{it} extraction techniques.

Many techniques for D_{it} characterization, are based on the analysis of the discrepancy between experimental and ideal capacitance as a function of the applied bias (CV characteristic) of the MOS structure [84],[85],[86]. However, several factors make the interpretation of extracted D_{it} ambiguous including: (i) low DOS in the conduction band (comparable with D_{it} or even lower), leading to difficulties in oxide capacitance (C_{ox}) estimation; (ii) typically narrow bandgap of high mobility semiconductors, which results in shorter minority carrier response time; (iii) typically large parasitics, Recently, several D_{it} extraction techniques [80],[87],[88],[89],[90], based on extraction of the equivalent small-signal circuit parameters, have been introduced. These techniques allow effects of minority carriers generation recombination, border traps and tunnel conductance to be accounted for. The circuit elements responsible for above effects cannot however be easily calculated, and, therefore, are treated as fitting parameters. This introduces uncertainties in the extracted D_{it}.

Summarizing, the most common issues in characterization of III-V/high-k interface common to all admittance methods are: (i) determination of the real C_{ox} value, and (ii) separation of true inversion response from D_{it} response [87],[88],[91],[92]. Table VI.1 shows a summary of main the CV based D_{it} extraction techniques along with strengths and limitations of each method.

In this section we present a new generalized high-low frequency CV technique for interface trap extraction at III-V interfaces. Since the technique is based on reproducing and fitting the

experimental CV characteristics, we start showing the model used to calculate the ideal capacitance. Then the model for interface trap extraction is discussed together with the characterization of $Si/SiO_2/HfZrO_2$ and $InGaAs/Al_2O_3$ interfaces in MOS Capacitors (MOSCAPs).

VI.1 - CV Calculation

The ideal CV curve for III-V/high-k interface can not be calculated in the "classical" approximation based on electron distribution calculated by the Boltzmann statistics. The Boltzmann statistics approximation, used for example for Si, ceases its validity in III-V devices because the Fermi level moves into the conduction band due to the low conduction band density of states. Moreover, nonparabolicity approximation and population of the Γ together with higher valleys X and L must be considered to calculate the semiconductor capacitance [93].

The substrate capacitance is given by:

$$C_s(\Psi_s) = -\frac{dQ_s(\Psi_s)}{d\Psi_s}. \qquad (VI.1)$$

The total charge for unit area is obtained from the electrostatic potential:

$$\varphi(x) = \frac{(E_F - E_I)}{q}. \qquad (VI.2)$$

where E_F is the extrinsic Fermi level and E_I the intrinsic energy level in the semiconductor.

The electrostatic potential is calculated from the charge density ρ(x) through the Poisson's equation:

$$\frac{d^2\varphi(x)}{dx^2} = -\frac{\rho(x)}{\varepsilon_s} = \frac{q\{p[\varphi(x)] - n[\varphi(x)] + N_D - N_A\}}{\varepsilon_s}, \qquad (VI.3)$$

N_D and N_A are donor and acceptor concentrations respectively. ε_s is the semiconductor dielectric constant. n[φ(x)] and p[φ(x)] that represent the electron and hole concentrations as a function of the electrostatic potential are given by:

$$n[\varphi(x)] = \frac{4}{\sqrt{\pi}}\left(\frac{2\pi k_B T}{h^2}\right)^{3/2} \sum_{i=\Gamma,L,X} {m_i}^{*3/2} \times \int_0^{\infty} \frac{\sqrt{\eta_i}(1+\alpha_i\eta_i)^{\frac{1}{2}}(1+2\alpha_i\eta_i)}{exp\left[\eta_i - \frac{q\varphi(x)}{k_B T} + \delta_i\right] + 1} d\eta_i , \qquad (VI.4)$$

where α_i is the nonparabolicity factor of the valley i, $\eta_i=(E-E_i)/k_BT$ the normalized electron kinetic energy, and $\delta_i=(E_i-E_I)/k_BT$ the reduced energy band offset with respect to E_I. The effective DOS

mass in valley i is m_i and E_i the correspondent energy. Electric field is calculated integrating equation (IV.3) and by means of Gauss's law we obtain the total charge per unit area Q_s:

$$Q_s(\Psi_s) = \varepsilon_s E[\varphi(x = 0)]$$
$$= -Sign(\Psi_s)\sqrt{2\int_{\varphi_b}^{\varphi_b+\Psi_s} -q\varepsilon_s\{N_D - N_A + p[\varphi(x)] - n[\varphi(x)]\}d\varphi(x)}\,, \qquad (VI.5)$$

Ψ_s is the total band bending into the semiconductor, calculated as the difference of surface potential φ_s and the bulk potential φ_b.

Once calculated $C_s(\Psi_s)$ the total capacitance of the metal-oxide-semiconductor structure is given by:

$$\frac{1}{C_{tot}} = \frac{1}{C_{ox}} + \frac{1}{C_s(\Psi_s)}\,. \qquad (VI.6)$$

The gate voltage for a certain bandbending Ψ_s is given by the following:

$$V_G = \Psi_s + \Phi_{ms} - \frac{Q_s(\Psi_s)}{C_{ox}}, \qquad (VI.7)$$

where Φ_{ms} is the metal gate semiconductor-work function difference.

Figure VI.1 and Fig.VI.2 show the calculated ideal capacitance (VI.6) and the population of holes and electrons (VI.4) for the Γ valley in different band approximations.

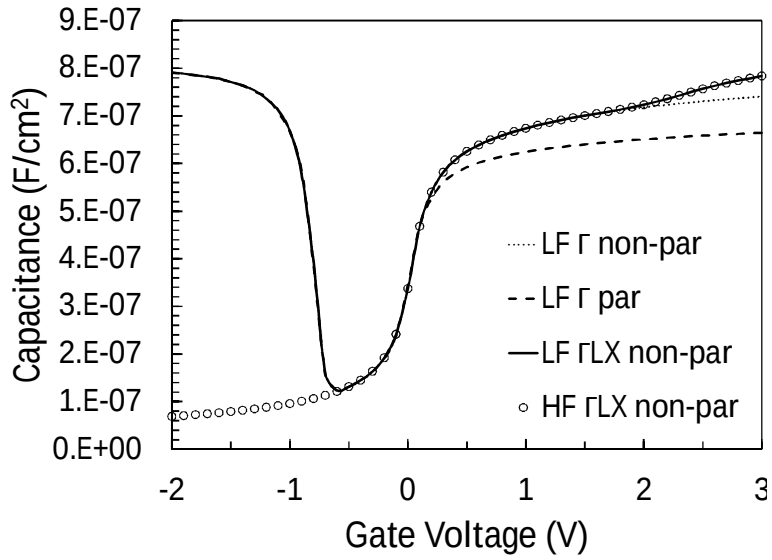

Fig. VI.1: Calculated ideal high and low frequency CV curves for different conduction band approximations.

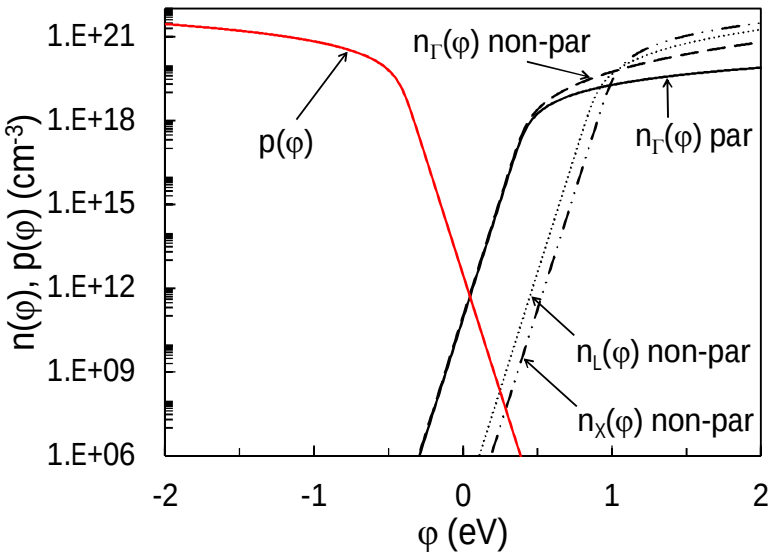

Fig. VI.2: Calculated electron and hole population for different conduction band approximations.

VI.2 - Extraction Method

The implemented method combines the theory of two classic method for D_{it} extraction: Terman [84] and high-low frequency [85],[86] methods.

The Terman method is based on the measurement of the high frequency CV characteristic of a metal-oxide semiconductor capacitor. Applying a gate bias results in a change of trap occupancy at

the interface and consequently in a stretch-out of the CV curve. The stretch-out is obtained from comparison with an ideal CV curve (simulated with no D_{it}) and allows for quantification of D_{it} with the following:

$$D_{it}(\Psi_s) = \frac{C_{ox}}{q}\left[\left(\frac{d\Psi_s}{dV_G}\right)^{-1} - 1\right] - C_s(\Psi_s)\,, \qquad (VI.8)$$

Main limitations of the method are: (i) the method requires to determine the real value of C_{ox} which is not known a priori, (ii) the trap density as a function of energy ($D_{it}(E_T)$) is limited in a narrow energy range, from weak accumulation to the beginning of depletion (where the stretch-out is appreciable).

On the other hand, high-low frequency method allows to determine D_{it} by assuming that the discrepancy between experimental high and low frequency CV is due to the presence of interface traps. D_{it} is given by the following:

$$D_{it}(V_G) = \frac{C_{ox}}{q}\left(\frac{C_{lf}}{C_{ox} - C_{lf}} - \frac{C_{hf}}{C_{ox} - C_{hf}}\right), \qquad (VI.9)$$

As for the Terman method the estimation of C_{ox} is source of uncertainty in the extracted D_{it}. Moreover, D_{it} is obtained as a function of the applied gate bias (V_G) and to obtain the correlation with the respective position in energy it is necessary to pass through the Berglund integral, whose accuracy for III-V devices is questionable.

Our method works as follows.

The experimental high-frequency CV curve is measured at low temperature (freezing trap response in comparison with the probing frequency) to obtain a “true” high frequency CV curve. Moreover, the low-frequency CV curve is measured at high temperature to obtain a “true” low frequency CV curve with full trap response. The discrepancy between experimental and ideal capacitances (Fig. VI.3(a)) is attributed to the presence of a certain D_{it}. High- and low- frequency CV curves are simulated with the model explained in the previous section, and the impact of interface traps is included as follows: in the high-frequency CV curve, the interface traps result only in a stretch-out of the curve, while in the low-frequency CV curve an additional capacitance due to traps (C_{it}=qD_{it}) is also taken into account together with the stretch-out effect.

The presence of interface traps change equations (VI.6) and (VI.7) respectively into:

$$\frac{1}{C_{tot}} = \frac{1}{C_{ox}} + \frac{1}{C_s(\Psi_s) + C_{it}(\Psi_s)}, \qquad (VI.10)$$

$$V_G = \Psi_s + \Phi_{ms} - \frac{Q_s(\Psi_s)}{C_{OX}} - \frac{Q_{it}(\Psi_s)}{C_{OX}}. \qquad (VI.11)$$

We have demonstrated that fitting simultaneously both high- and low-frequency CV curves (Fig. VI.3(c)) allows the D_{it} to be determined as a function of energy and C_{ox} to be estimated self-consistently.

Frequency dispersion observed in accumulation cannot be explained in the frame of classical interfacial traps' models that foresee a cut-off frequency forC_{it}much higher than the maximum frequency applicable during CV measurement. Frequency dispersion can be associated with the presence of border traps in the high-k. Since our model does not distinguish border traps from the interfacial ones, the extracted D_{it} includes the border traps effectively projected to the interface (the equivalent D_{it} responsible for stretch-out and C_{it} contribution).

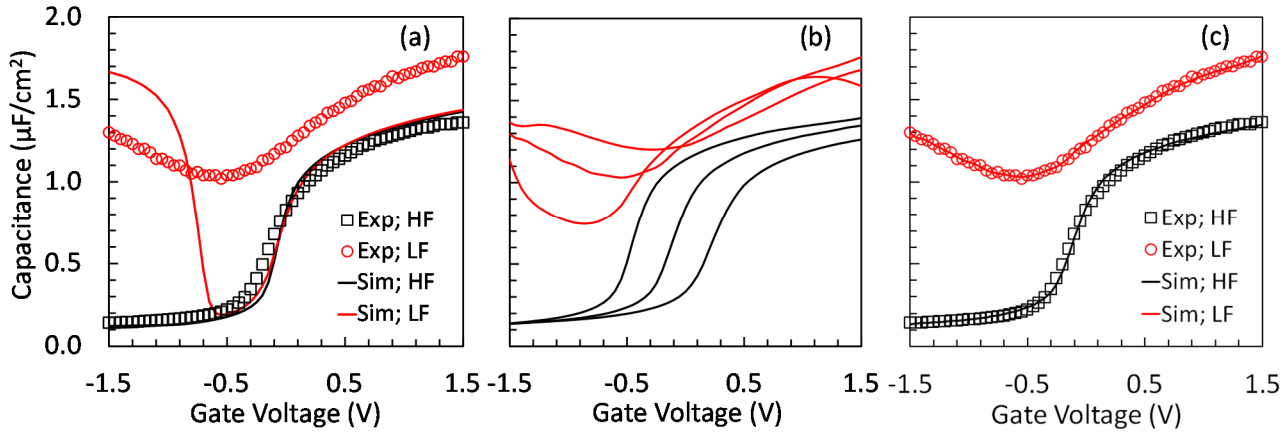

Fig. VI.3: $In_{0.53}Ga_{0.47}As$ /Al_2O_3 n-type sample; (a) comparison between experimental and ideal CV curves, (b) impact of different D_{it} distributions considered during the automatic fitting procedure, (c) fitting obtained with a proper D_{it} distribution.

Moreover, this method has been extended by including a fitting procedure, see Fig. VI.4 , reproducing automatically experimental high- and low-frequency CV curves by simulation. Here are some details of how the procedure works. A set of i-values for the substrate doping (N_{DOP}) and for the EOT is created. Also an initial set of D_{it} can be defined. This set allows to explore different starting points for the fitting problem and consequently it increases the possibilities to find the optimum solution. Starting from the ideal CV characteristics (Fig. VI.3(a)), simulated with the i-th set of N_{DOP}, EOT and D_{it}, the automatic fitting procedure searches the best D_{it} profile matching both high- and low-CV curves (Fig. VI.3(b)). During the automatic fitting, the values of N_{DOP} and EOT are also "adjusted" in an interval centered on the i-th value to provide the most reliable value of C_{ox}.

Once all the i-th starting points are considered, the procedure provides as an outcome the best CV curves fit obtained (Fig. VI.3(c)) together with the corresponding D_{it} and C_{ox}.

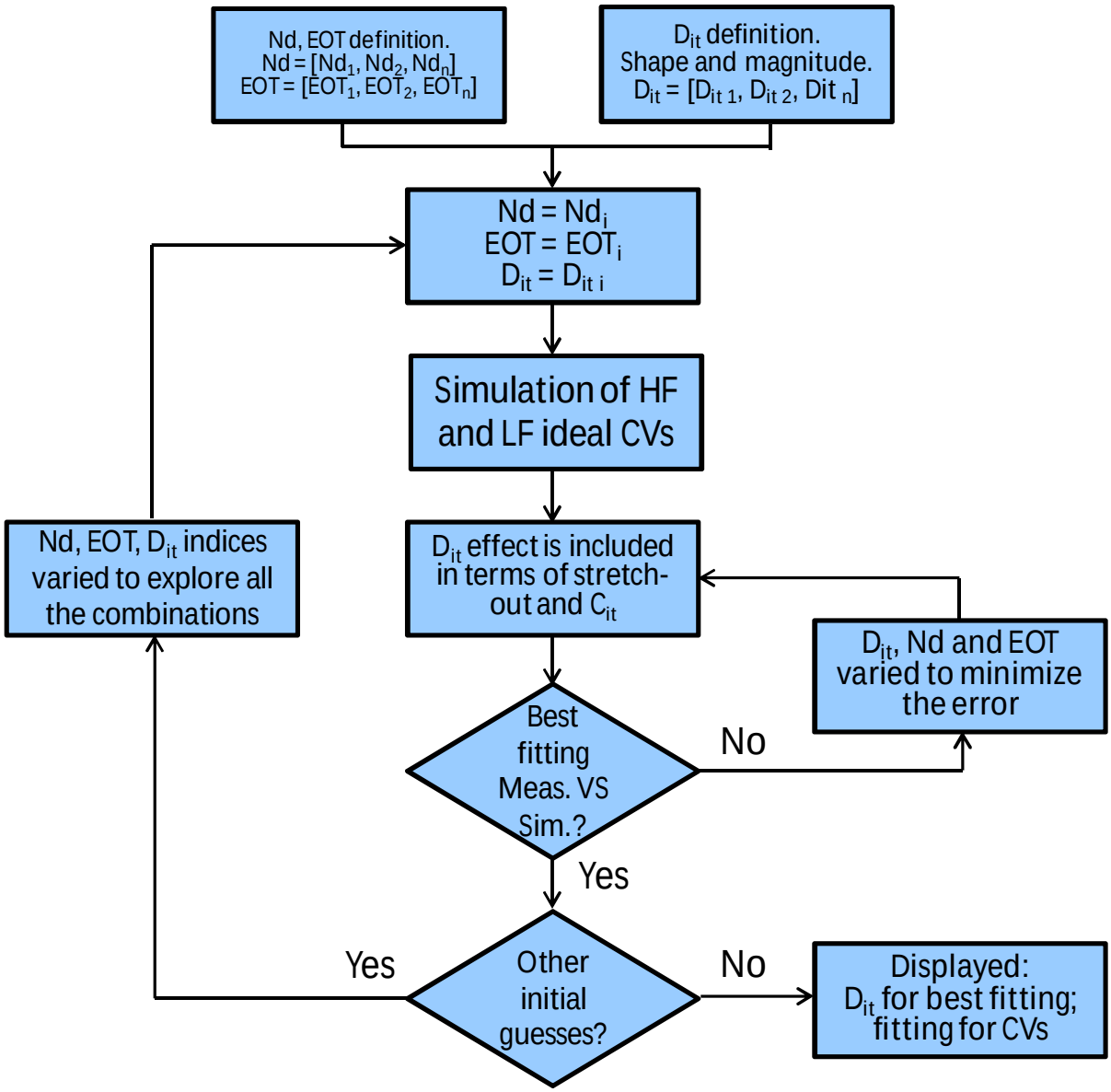

Fig. VI.4: Block diagram of the automatic fitting procedure.

VI.3 - Results

The proposed technique has firstly been tested for D_{it} extraction in a $Si/SiO_2/HfZrO_2$ MOSCAP and then it has been applied to $In_{0.53}Ga_{0.47}As/Al_2O_3$ MOSCAPs.

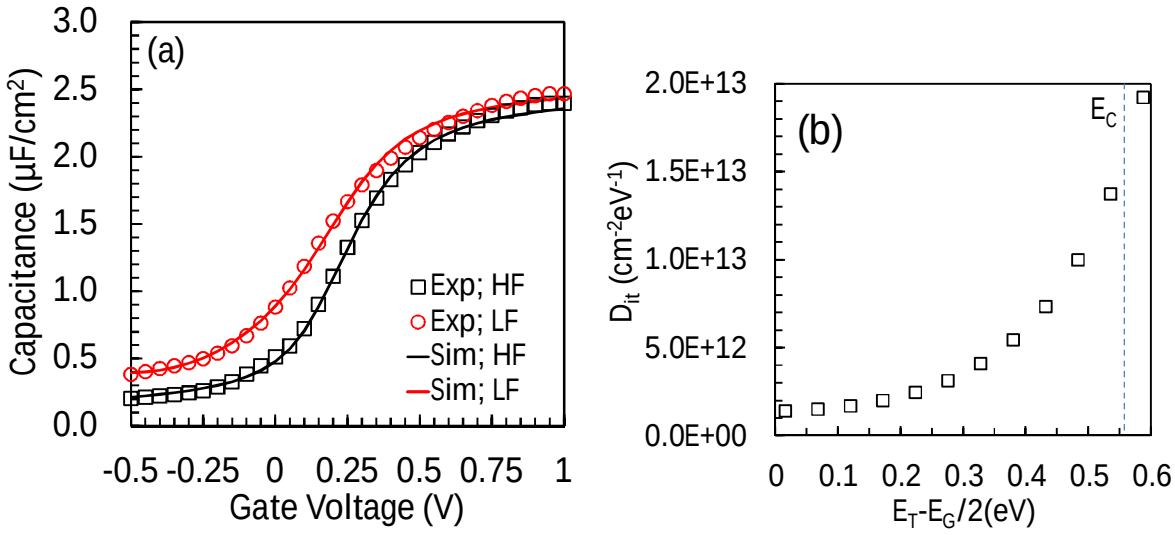

Fig. VI.5: (a) Experimental (symbols) and simulated (lines) CV characteristics for true low and high frequency for Si/SiO_2/$HfZrO_2$ MOSCAPs. (b) Extracted interface traps density.

A Si/SiO_2/$HfZrO_2$ sample has been chosen for testing the technique because, due to the high DOS of Si, the capacitance in accumulation should approach the C_{ox} value. This allows to compare the value of C_{ox} estimated from the CV curve in accumulation with the C_{ox} value extracted from our generalized method. In Fig. VI.5(a) are shown the experimental CV curves along with the fitting obtained by extracting a proper D_{it}. High-low CV curves have been measured at 1 MHz (300 K) and 1 KHz (475 K) respectively. Experimental high-frequency CV curve in accumulation suggests a C_{ox} value of ≈2.45 μF/cm^2, while the value extracted from the automatic fitting is 2.7 μF/cm^2. C_{ox} extracted from the CV curve in accumulation is a good approximation only in the case that the total capacitance has reached its maximum value, which it may be not the case if an high density of interface traps is present near the conduction band. Figure VI.5(b) showing the extracted D_{it}, confirms this assumption: a D_{it}≈1.5×10^{13} cm^{-2}eV^{-1} is calculated at the edge of the conduction band. High interface trap density can effectively explain: (i) the difference between high and low frequency CV curves in accumulation, that otherwise would be superimposed, (ii) underestimation of C_{ox} calculated from high frequency CV in accumulation because due Fermi level pinning the total capacitance has not reached its maximum value. Moreover, D_{it} shows its minimum of 1.5×10^{12} cm^{-2}eV^{-1} energy located at midgap.

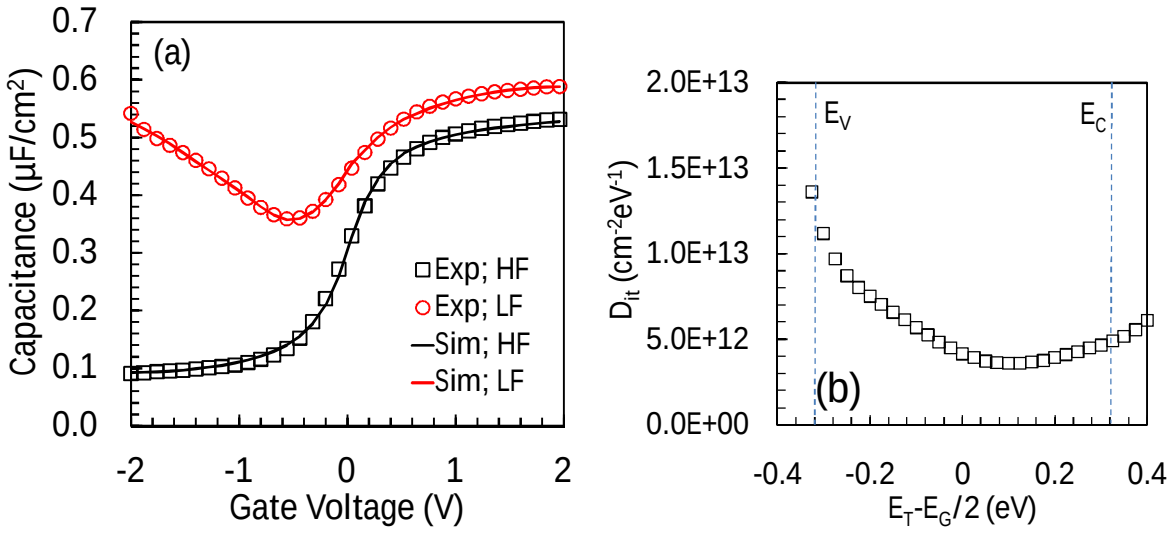

Fig. VI.6: (a) Experimental (symbols) and simulated (lines) CV characteristics for true Low and High frequency for $In_{0.53}Ga_{0.47}As/Al_2O_3$ MOSCAPs. (b) Extracted interface traps density.

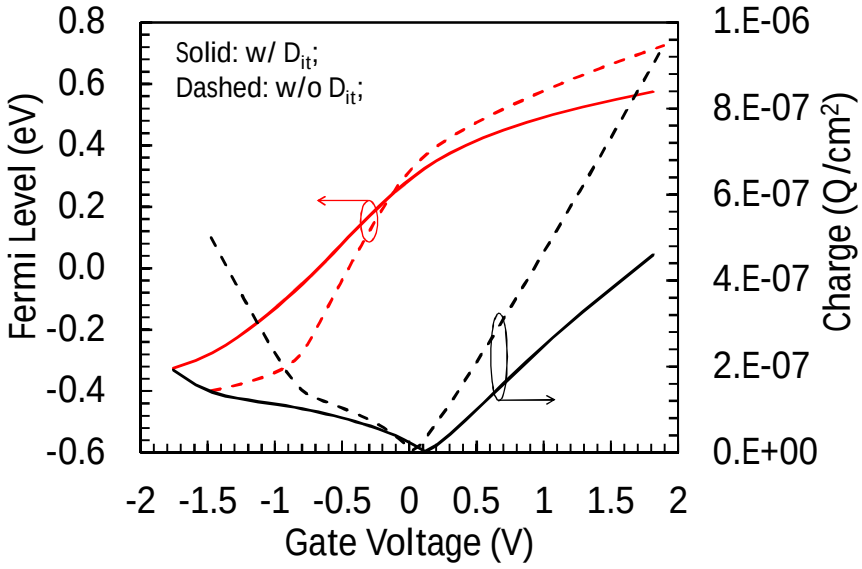

Fig. VI.7: Fermi level position and surface charge in InGaAs as a function of the applied gate voltage.

Simulations of CV curves for $In_{0.53}Ga_{0.47}As/Al_2O_3$ samples have been performed considering non-parabolic bands and multi-valley carrier distribution, leading to CV fitting and D_{it} extraction. The relative dielectric constant for the Al_2O_3 has been chosen equal to 8.

Figure VI.6(a) shows experimental and simulated CV curves for an $In_{0.53}Ga_{0.47}$ As/Al_2O_3 MOSCAP samples. High-low CV curves have been measured respectively at 1 MHz (300 K) and 1 KHz (375 K). The good agreement between experimental and simulated CV curves is obtained with

the D_{it} shown in Fig VI.6(b). D_{it} shows a parabolic shape with a minimum of 4×10^{12} $cm^{-2}eV^{-1}$ energy located 0.15 eV above the midgap. D_{it} at the valence band edge was found to be $\approx2\times10^{13}$ $cm^{-2}eV^{-1}$.

In Fig. VI.7 the impact of D_{it} on both the position of the Fermi level and the surface charge in InGaAs is shown as a function of the applied gate voltage. Moving towards the conduction band the D_{it} remains lower than 1×10^{13}. The Fermi level moves inside the conduction band allowing the accumulation of electrons at the surface, as suggested by the linear dependence of Q_S as a function of V_G for $V_G>0$ V. However, impact of D_{it} can not be neglected: for $V_G=2$ V the surface electronic charge is equal 5×10^{-7} Q/cm^2, with respect to 1×10^{-6} Q/cm^2 of the ideal case with no D_{it}. On the other hand, near the valence band, a D_{it} higher than 1×10^{13} causes pinning of the Fermi level that can not move inside the valence band. For $V_G=-2$ V the profile of the hole surface charge as a function of V_G is still not completely linear. This suggests that the low frequency capacitance for $V_G<0$ V is dominated by C_{it} rather than minority carrier response.

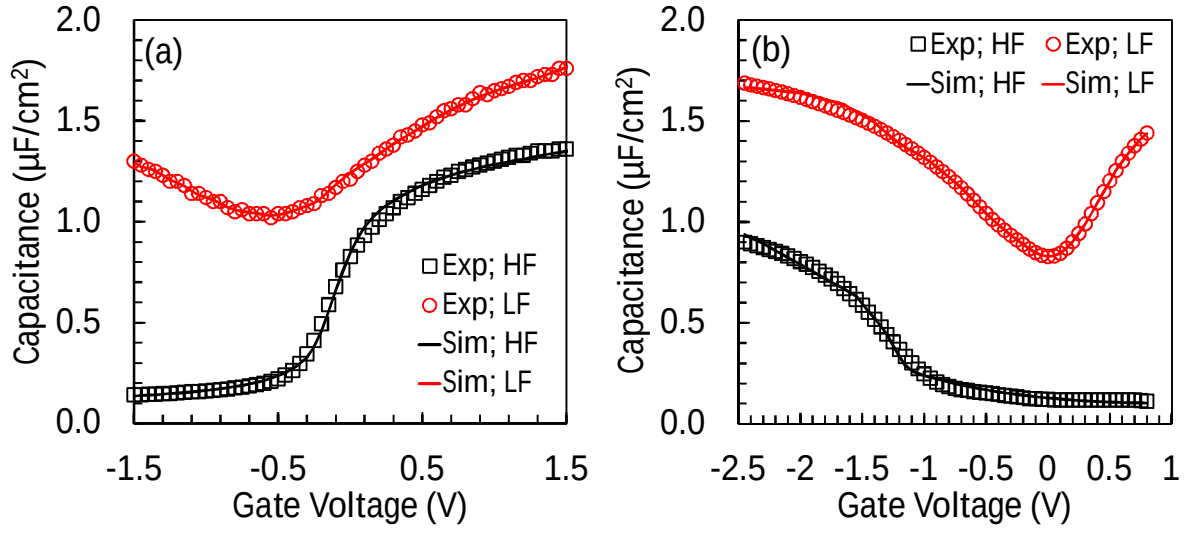

Fig. VI.8: (a) CV curve fitting obtained for a $In_{0.53}Ga_{0.47}As$ /Al_2O_3 n-type sample. (b) CV curve fitting obtained for a $In_{0.53}Ga_{0.47}As$ /Al_2O_3 p-type sample.

In Fig.VI.8(a) the method has been applied to an InGaAs/Al_2O_3 n-type MOSCAP sample. High-low CV curves were measured at 1 MHz (150 K) and 1 KHz (375 K) respectively. Extracted D_{it}, reproducing both CV curves, shows a parabolic shape with a minimum density of 9×10^{12} $cm^{-2}eV^{-1}$ located 0.25 eV above the midgap. D_{it} at the valence band edge was found to be $\approx2.5\times10^{13}$ $cm^{-2}eV^{-1}$, see Fig. VI.9(a).

Figure VI.8(b) illustrates the application of the method to InGaAs/Al_2O_3 p-type MOSCAP samples. High-low CV curves have been measured at 1 MHz (300 K) and 1 KHz (400 K) respectively. The minimum of D_{it} is located ≈0.20 eV above the midgap with a density of 9×10^{12}

$cm^{-2}eV^{-1}$, as for the n-type sample. For both n-type and p-type sample a severe Fermi level pinning, due to the large density of traps, has been observed moving toward the valence band. On the other hand, moving towards the conduction band, pinning does not occur and Fermi level moves inside the band. Experimental low frequency CV, measured at low temperature (150K) to freeze the traps response, have shown the response of minority carrier for the p-type sample. Therefore, the inversion contribution has to be included in the simulated low frequency CV curve for the p-type sample. Under these assumption, D_{it} extracted from the p-type sample agrees with the one extracted on n-type sample for the whole energy range considered (Fig. VI.9(a)). Neglecting minority carrier response would result in an overestimation of D_{it} at the conduction band edge for the p-type sample [88].

The method estimates the high-k thickness, and consequently C_{ox}, self-consistently with D_{it} distribution vs. trap energy. For the n-type MOSCAP sample the Al_2O_3 thickness was found to be equal to 3.4 nm. This value is really close to the expected Al_2O_3 thickness of 3.2 nm, suggesting a reliable estimation of C_{ox}.

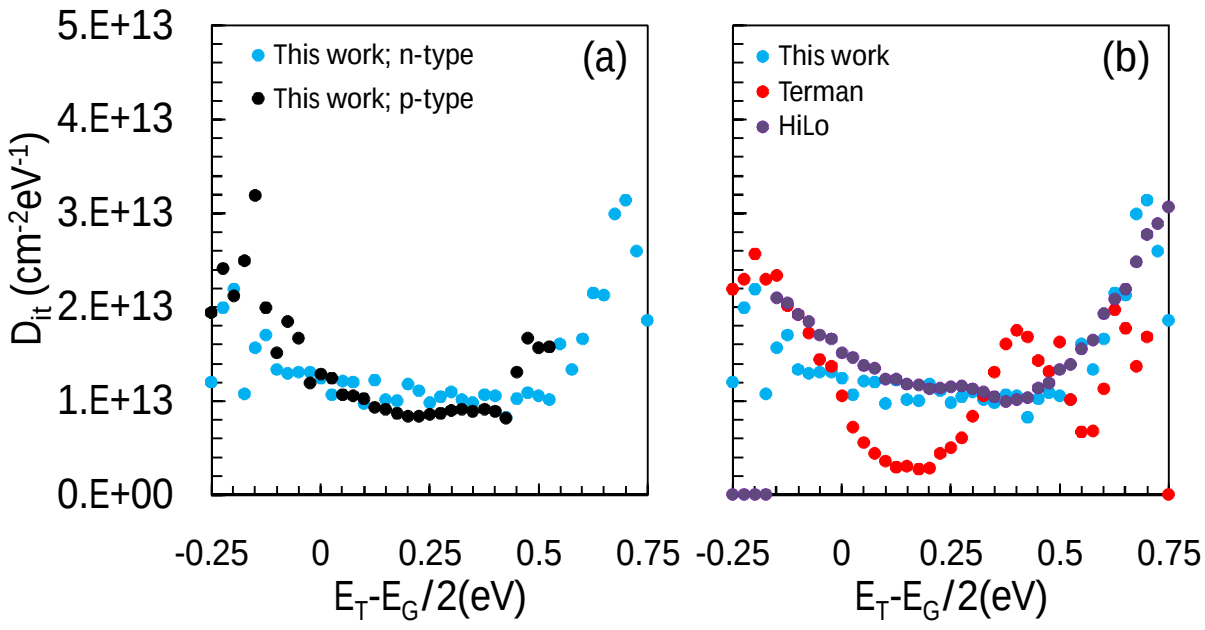

Fig. VI.9: (a) Comparison between D_{it} extracted from an n-type and a p-type sample. (b) D_{it} extracted from the n-type sample using different methods.

Figure VI.9(b) shows the good agreement of D_{it} extracted with our method if compared with: (i) Terman method, (ii) high-low frequency method. D_{it} extracted by these two methods strongly depends on the value of C_{ox} which is not known and has to be determined by the maximum value of the capacitance in accumulation. The agreement reached in accumulation (energies higher than 0.35 eV in Fig. VI.9(b)) by the three techniques is a further evidence of reliable C_{ox} estimation.

VI.4 - Summary

We proposed and implemented a novel generalized method for interface-trap characterization in high-k/III-V capacitors. The method exploits an automatic fitting procedure of the high and low frequency CV curves and allows to overcome two main difficulties in the extraction of D_{it}: uncertainty in the C_{ox} value, and separation of D_{it} and minority carriers response. The model accounts for the border traps as projected to the interface, thus, an equivalent D_{it} is extracted. We tested the C_{ox} estimation by our method in $Si/SiO_2/HfZrO_2$ MOSCAP where high density of state makes the extraction of C_{ox} from the accumulation region of CV curves more straightforward than in III-V semiconductor. C_{ox} was found to be slightly higher when extracted with our method. The underestimation of C_{ox} if calculated from its maximum value in high frequency CV curves in accumulation is due to the fact that interface-trap effects are neglected, which is not a good approximation. Indeed, a $D_{it} \approx 1.5\times10^{13}$ $cm^{-2}eV^{-1}$ near the conduction band edge can explain the underestimation of C_{ox} calculated from high frequency CV curves in accumulation because due to Fermi level pinning the total capacitance can not reach its maximum value. At the same time this D_{it} explains the difference between high and low frequency CV curves in accumulation, that otherwise would be superimposed.

We applied the method for interface trap characterization to two different $In_{0.53}Ga_{0.47}As/Al_2O_3$ MOSCAP samples. Both samples showed a U-shaped D_{it} with a minimum located between midgap and the conduction band edge and a maximum approaching the valence band edge. The latter is responsible for a severe Fermi level pinning moving toward the valence band preventing the inversion of the surface charge in the n-type samples. On the other hand moving towards the conduction band Fermi level pinning does not occur and for D_{it} extraction in p-type samples the contribution of minority carrier has to be included. Under this assumption we verified that D_{it} extracted from the n-type sample and the p-type sample are in a good agreement. Neglecting minority carrier response in p-type would overestimate D_{it} approaching the conduction band. Moreover, we compared the D_{it} extracted by our method with the Terman method and high-low frequency method. Since Terman and high-low frequency methods need to estimate C_{ox} we used the value extracted by our method. D_{it} agreement reached by the three techniques is a further evidence of reliable C_{ox} estimation.

Section B: Trap Characterization in $Si/SiO_2/Al_2O_3$ Stack

In the fabrication of the gate stack of Silicon and high-k based logic devices, an interfacial layer of SiO_2 inevitably results between the silicon substrate and the high-k material, since the different layers are deposited in oxidizing conditions. The presence of this layer strongly affects the behaviour of the devices increasing leakage current through the stack or reducing the carrier mobility performances. Controllability of thickness and quality of interfacial layer are very

important in order to evaluate the optimum combination of dielectric stack that will provide the best leakage and performances characteristics.

In the next sections we will study the electrical properties of traps at the SiO_2 interfacial layer by means of charge pumping (CP) [94],[95] and trap spectroscopy by charge injection and sensing (TSCIS) [96]. Moreover an independent validation of the traps parameter will be given by means of gate leakage simulation (I_{LEAK}) reproducing the experimental characteristics.

VI.5 - Devices Fabrication

Devices under investigation were grown on slant etch wafer. The slant etch is a technique developed to fabricate transistors, capacitors and other test devices using a continuously scaled SiO_2 interfacial layer between silicon substrate and high-k dielectric, on a single wafer. With this technique it is possible, for instance, to vary the thickness of SiO_2 from 1-nm to 4-nm on the same wafer without detrimental effects on the electrical characteristics of the fabricated devices. It is simple to understand that this technique provides a powerful tool in examining the effects of the interaction between SiO_2 and high-k materials on the devices performances, as a function of the SiO_2 thickness [97],[98],[99].

SiO_2 is selectively removed with a wet etching to result in a gradual thickness variation across a single 300-mm wafer. First of all, a 6-nm layer of high quality thermal SiO_2 was grown at 900 °C on wafer with shallow trench isolation. This is then etched back with a slant profile by slowly submerging the wafer in a 0.34% HF solution. The desired range of SiO_2 is obtained across the structure by adjusting the speed at which the wafer is submerged into the etch bath. The typical variation in thickness across the wafer, which is measured by spectroscopic ellipsometryis shown in Fig. VI.10, along with a schematic of the slant etched wafer. An ozonated–water rinse is performed after the wet etch process. The slant etched SiO_2 layer provide a thickness series on which a high-k layer of constant thickness can be easily deposited. Then, 12 nm of Al_2O_3 deposed by ALD. The needed thickness of the high-k can now be deposited on slant etch SiO_2. A post deposition annealing (PDA) is performed before the deposition by sputtering of a TaN gate electrode and finally a capping layer deposition. The electrode and dielectric stack patterning is performed by conventional dry etching. Junction activation is performed by spike annealing at 1030 °C, before a 520 °C 20-min-forming gas anneal [98].

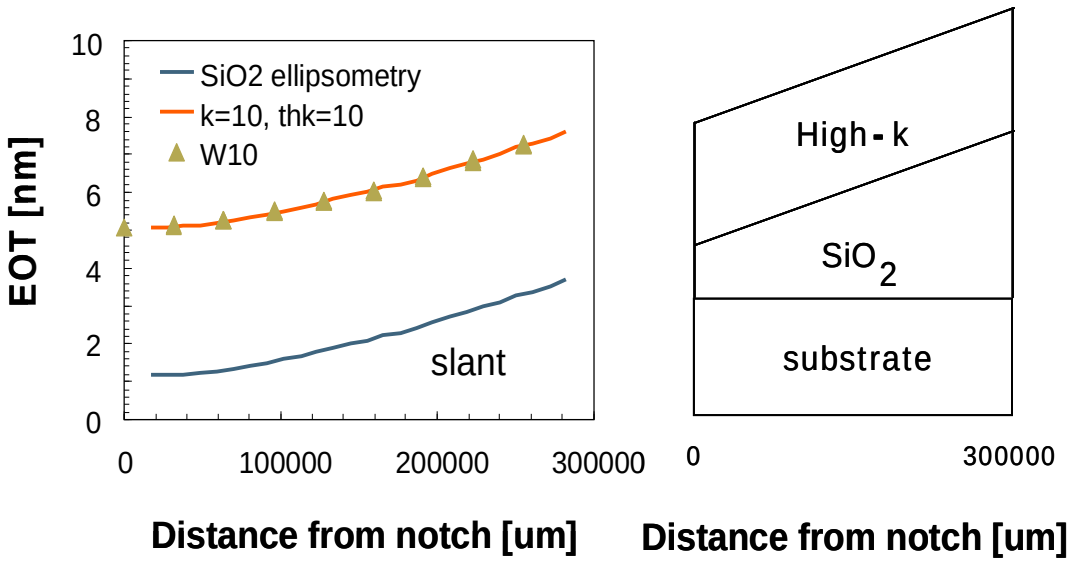

Fig. VI.10: EOT derived from CV measurements along the slant-etch wafer with SiO_2/Al_2O_3 stack. The schematic cross section of the wafer is shown on the right.

To measure the leakage current $I_G(V_G)$ and for TSCIS measure, were chosen n-mos transistors with area 1 um^2.

For charge pumping measure were chosen n-mos transistor with area 100 um^2. In this technique the density of traps is sensed measuring the recombination current of electron emitted from the interface traps. To reduce the effect of noise component we have chose the larger device that shows higher recombination current.

VI.6 - Slant Etch Validation

With slant etch technique the upper surface of SiO_2 has to be chemically etched before of the high-k dielectric deposition. This chemical attack definitively modifies the SiO_2/high-k interface, that results different compared to the same interface built on an in situ steam generated oxide (ISSG). Different processes lead to a different interfaces that in turn could lead to a different energy distribution and density of defects at the interface. To be sure the slant etch technique preserve the interface characteristic, the comparison of the SiO_2/high-k interface manufactured using standard uniform thermally growth oxide and slant-etch process is of a fundamental importance.

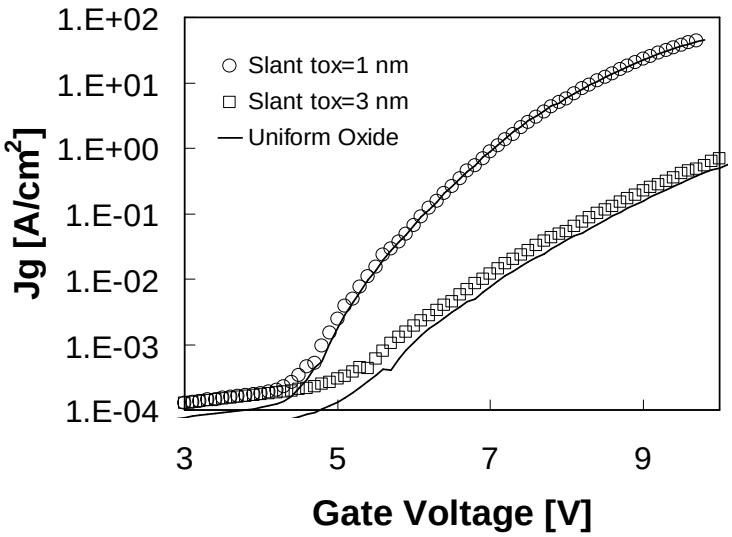

Fig. VI.11: Leakage currents measured on pure SiO_2 slant-etch wafer (symbols) and thermally grown oxides (lines). The very good agreement proves that the slant-etch technique does not degrade the oxide quality.

To compare the two different processes, $I_G(V_G)$ measures have been considered. Differences in terms of defect density and distribution in energy and space would lead the device to have different $I_G(V_G)$ curves.

$I_G(V_G)$ of n-mos transistors with thermally growth uniformSiO_2 layer, respectively 1 nm and 3 nm, have been compared with $I_G(V_G)$ of a slant etch wafer. The following voltages were applied to the structure, $V_B = V_S = 0V$, $V_D = 0.05$ V and a voltage sweep from 0 V to 10 V drove the gate. The weak bias at the drain was used to orientate the electrons flow in the channel. In Fig. VI.11 is shown the comparison between slant-etch and uniform oxide leakage current characteristics. The excellent agreement between leakage current measured across slant-etch and ISSG measure demonstrates the good quality of the oxide layer obtained with the slant-etch technique. In fact if this technique introduced a higher density of defects in the SiO_2/Al_2O_3 interface, a higher I_{LEAK} curve would be found. The perfect match between the two leakage characteristic means that not only the density of traps but also the energetic distribution is comparable. For the entire voltage sweep, thus for all the different electrical fields applied to the structure, the characteristics are equal, suggesting that the energetic distribution of the defect bands is the same for both slant-etch and ISSG oxides.

VI.7 - Intermixing Layer Characterization

In this section are shown the results of CP and TSCIS, made on slant-etch wafer, performed for different thickness of SiO_2 (from 1 nm to 3 nm).

CP have been conduct applying the following times and voltages. The $t_{DISCHARGE}$ in accumulation was 1 ms, enough to completely discharge the charge trapped during the cycle, and to allow a complete sense of the charged traps. The t_{CHARGE} was increased starting from 1 us to 1.2 ms with a multiplying factor of 1.2. V_{BASE} = -2 V is low enough to reach the accumulation condition in the channel during the discharge and V_{STOP}=5.5 V. Theoretically the knee of the curves occurs in correspondence of the SiO_2/high-k interface, thus the value of D_{ot} before of the knee is referable at the SiO_2. If we consider this assumption true, one interesting phenomenon appears in Fig. VI.12.

In this figure are compared four different characteristics in function of t_{ox} the thicknesses are the same of the previous case. For t_{ox}=1.2 nm we found a total density of trap (D_{ot}) $\approx 1.3\times10^{12}$ cm^{-2}, for t_{ox}=3.0 nm $D_{ot}\approx 0.3\times10^{12}$ cm^{-2}, passing through an intermediate thickness in which $D_{ot}\approx 0.6\times10^{12}$ cm^{-2}. The trend seems to be clear: interface and near interface state density decrease as we increase the SiO_2 thickness. This result suggests the presence of an intermixing layer between SiO_2 and the Al_2O_3. In fact the interface between the two dielectrics is not well defined and abrupt, but is a real intermediate layer. During the deposition and the following annealing the SiO_2 is contaminated by the Al_2O_3, ternary compound depending on thermal budget and oxygen availability tend to consume the interfacial layer of SiO_2. The traps density of the intermixing layer is clearly higher than the SiO_2 trap density. Of course this intermixing layer is easier to be pumped, during a CP measure, when the layer of SiO_2 is thin as shown in Fig. VI.13. The above listed interfacial variable D_{ot}, which depends on t_{ox} are explainable considering the following reasoning: the thinner the SiO_2, the closer to Si/SiO_2 the intermixing layer, the easier to pump this layer, the higher the interface layer traps density sensed.

In Fig. VI.13, TSCIS is applied on a stack composed by high-k dielectrics deposed on a layer of slant-etch SiO_2. with 10 nm of Al_2O_3 as high-k dielectrics. When the interfacial layer of SiO_2 is varied on the same wafer we can achieve a full defects spectroscopy of both interfacial (thick SiO_2) and bulk high-k defects (thin SiO_2). The figure shows two extreme interfacial layer thickness cases (1 nm and 3 nm of SiO_2) for both the materials. A defects density of 1×10^{20} cm^{-3} is observed in all the cases. Considering the Al_2O_3 cases, a typical defect band is observed between 2.7 eV and 2.2 eV below the conduction band of the SiO_2. When the 3 nm interfacial layer is considered note that defects are much closer to the Si interface than expected from the stack parameters, strongly suggesting the presence of a severe intermixing layer between SiO_2 and Al_2O_3. Note that defects in the SiO_2 observed for t_{ox}=3 nm have similar densities compared to bulk Al_2O_3 defects in the t_{ox}=1 nm case.

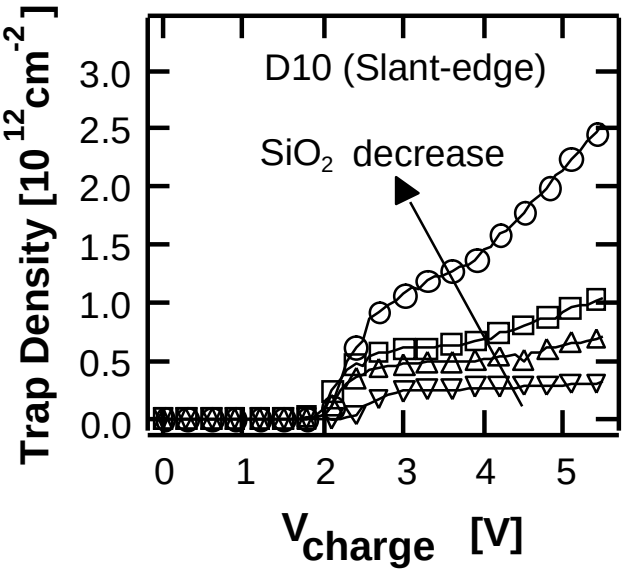

Fig. VI.12: Trap density vs. charging voltage derived using CP with $t_{DISCHARGE}$=t_{CHARGE}= 1 ms for different slanted SiO_2 thickness (from 1 nm to 3 nm SiO_2). More traps are sensed for thinner SiO_2.

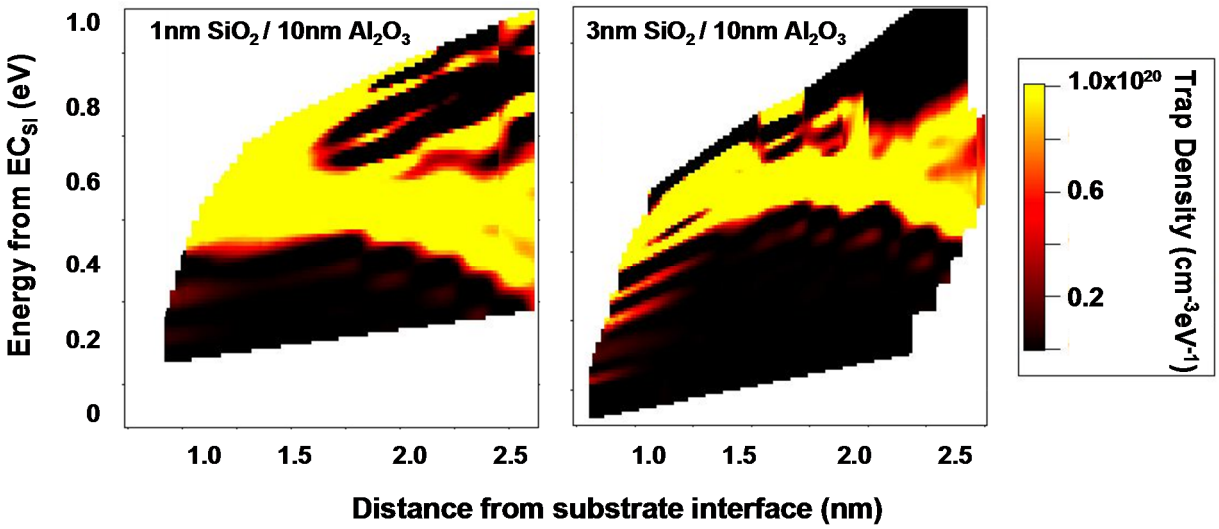

Fig. VI.13: Spatial-energy trap map obtained from TSCIS: thicker SiO_2 exhibit similar trap properties as thinner SiO_2, suggesting a severe intermixing.

VI.8 - Simulation of Leakage Current

In order to gain more quantitative insights, we derived defect densities and energies by using leakage current simulations performed with the statistical physic-based model presented in [100],[101]. This model assumes the multi-phonon trap assisted tunneling as the conduction mechanism. Moreover, it includes quantization effects and random defect generation inside SiO_2, intermixing and high-k layers, see Fig. VI.14.

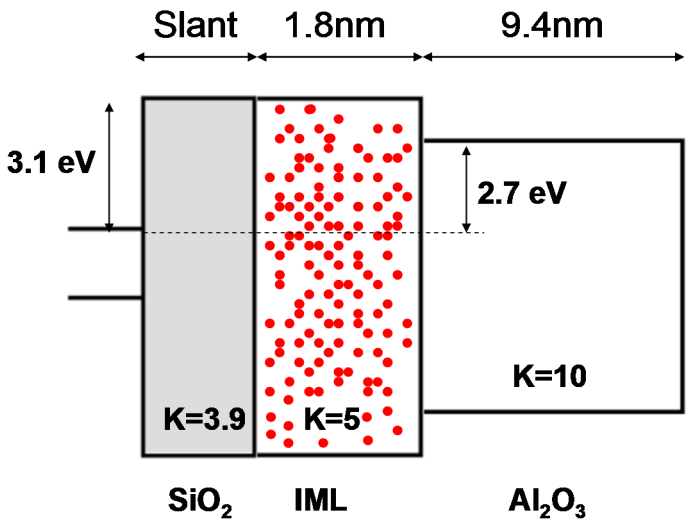

Fig. VI.14: Schematic band diagram of the simulated SiO_2/Al_2O_3 stack including intermixing layer. IML thickness was kept constant for all the slanted stacks.

	tox=1.22nm	tox=1.60nm	tox=1.96nm	tox=2.33nm	tox=2.70nm	tox=3.07nm
Et_ox [eV]	2.0-2.7	1.9-2.5	1.95-2.7	1.95-2.7	1.95-2.7	1.95-2.7
Nt_ox [cm^{-3}]	5.00E+19	4.00E+19	3.50E+19	3.40E+19	1.50E+19	1.00E+19
σ_ox [cm^2]	1.50E-14	1.20E-14	1.20E-14	1.20E-14	1.20E-14	1.00E-14
Et_int [eV]	1.95-2.6	1.9-2.6	1.85-2.4	1.8-2.1	1.65-2.2	1.4-2.2
Nt_int [cm^{-2}]	3.00E+12	3.00E+12	3.00E+12	3.00E+12	3.00E+12	3.00E+12
σ_int [cm^2]	5.00E-14	5.00E-14	5.00E-14	5.00E-14	5.00E-14	5.00E-14
Et_hk [eV]	1.1-1.6	1.1-1.6	1.1-1.6	1.1-1.6	1.1-1.6	1.1-1.6
Nt_hk [cm^{-3}]	9.00E+18	9.00E+18	9.00E+18	9.00E+18	9.00E+18	9.00E+18
σ_hk [cm^2]	1.00E-14	1.00E-14	1.00E-14	1.00E-14	1.00E-14	1.00E-14

Table VI.2: Traps parameters used to simulate the slant-etch/10 nm Al_2O_3 substrate injection leakage currents. In the yellow cells are collected the parameters that significantly vary during the simulations for different SiO_2 thicknesses, all the others can be kept almost constant.

During the simulations the following stack parameters were chosen: Φ_B=3.1 eV, Φ_{OFFSET}=2.7 eV (defined as difference between the bottom of high-k-CB and the Si-CB), WF_{GATE}=4.4 eV (defined as the difference between the energy Fermi level and the vacuum level) and k_{Al2O3}=10. In Table VI.2 we reported the main trap parameters as a function of t_{ox}. We consider three kind of traps: traps placed in SiO_2 bulk, traps placed at SiO_2/high-k interface and traps placed in Al_2O_3

bulk. For each of them the energy band (E_t), the density (N_t) and the capture cross section (σ_t) considered in simulations have been reported.

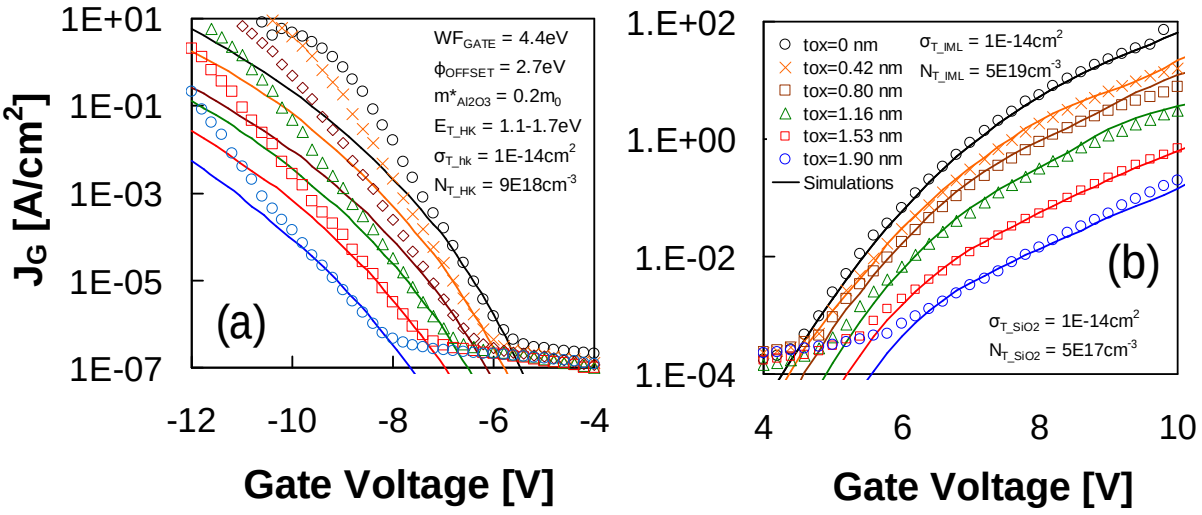

Fig. VI.15: Measured (symbols) and simulated (solid lines) $I_G(V_G)$ for $V_G<0$ (a) and $V_G>0$ (b) across SiO_2/Al_2O_3 stack. Simulation inputs are stack parameters (thicknesses and offset as defined as in Fig. VI.15) and the trap parameters (density, cross section, energy levels, see Table VI.2).

Let us start considering the case with 10 nm of Al_2O_3. The simulations have been made for both substrate and gate injections. In Fig. VI.15(b) is shown the case of substrate injection. An excellent fit is obtained for the thicknesses of SiO_2 considered. Since we are considering the substrate injection the conduction is dominated by the Φ_B barrier and by both SiO_2 and SiO_2/Al_2O_3 interface traps.

Traps in the high-k dielectric are not important. Further, due to the band bending, high-k bulk traps cannot be percept at high electrical field. High-k trap parameters have been kept constant, pointing out a low sensitivity of the substrate injection simulations respect these traps. Different considerations have to be made for traps in SiO_2 and at the interface between the two dielectrics. The traps density at the interface has been taken constant for all the different thicknesses, changing only the energy band. Increasing the t_{ox} shallower traps were considered. Anyway the most interesting result is related to the SiO_2 bulk traps: a strong density dependence on the SiO_2 thickness has been found. Decreasing the layer thickness of the interfacial oxide, the trap density has been increased to fit the experimental curve, $N_{t,ox}$ for t_{ox}=1.22 nm is five time higher than the t_{ox}=3.07 nm case. A possible explanation for this trend has to be searched in the presence of the intermixing layer between SiO_2 and Al_2O_3, a transition layer composed by a mix of the two different materials and characterized by higher density of defects than SiO_2. The simulator provide the possibility to define traps in between the two dielectrics, but with the interfacial traps only a 2D layer can be defined, not enough to simulate the intermixing that is a real 3D layer. $N_{t,ox}$ has to be increased for

thin SiO_2 in order to mimic the intermixing layer. When SiO_2 becomes so thin to be comparable with the penetration thickness of Al_2O_3, the intermixing layer is extended on almost all the SiO_2 layer. Increase $N_{t,ox}$ is a way to simulate this effect.

In Fig. VI.15(a) is shown the case of the gate injection for the same wafer considered before. Since the electrons are injected starting from the gate, transport is function of metal gate/Al_2O_3 barrier and traps density in the high-k. Al_2O_3 traps density was chosen $N_{t,Al2O3} \approx 10^{19}$ cm^{-3}according with the substrate injection case. At low electrical fields a good agreement is obtained between experimental results and simulations. On the contrary, the used model doesn't describe effectively the leakage conduction through the stack for medium and high fields. For all the different thicknesses of SiO_2 the simulate leakage currents are lower than the experimental curves, indicating that some other mechanisms of conduction occur.

VI.9 - Summary

We presented a methodology to quantify defects in SiO_2/high-k structures using independent experimental techniques and simulations coupled with a simple fabrication technique. We validated the slant-etch manufacturing process by means of experimental observations made on stack composed by SiO_2/Al_2O_3 with different SiO_2 thicknesses. Leakage currents characteristics of and capacitors realized on wafer slant-etch were compared with leakage of devices realized with an uniform thickness of thermally growth SiO_2. The perfect match obtained between leakage characteristics suggests that SiO_2/high-k interface, realized with slant-etch technique, has the same quality in terms of defect density of a normal uniform layer of SiO_2 thermally growth. Appling TSCIS on devices realized with both the above mentioned process we obtained a further confirmation of the slant etch technique. The presence and the impact of an intermixing layer in the stack SiO_2/Al_2O_3 has been studied by means of CP and TSCIS techniques. In the CP experiment, the charging time was gradually increased to explore both the near interface traps and trap deeper in the stack. We observed a dependence of the traps density in function of the SiO_2 thickness. A higher density of traps was sensed decreasing the SiO_2 thickness of the samples measured. This trend can be explained with the presence of the intermixing layer, that for thin SiO_2layers results closer to the Si/SiO_2 interface and thus easier to be pumped. TSCIS measures performed on the same SiO_2/Al_2O_3confirmed this observation showing that the typical SiO_2/high-k interface defects are much closer to the Si than expected. An independent confirmation of the defect density and distribution was obtained by means of simulations. Leakage currents were simulated on SiO_2/Al_2O_3stack with different SiO_2 thicknesses. Simulations made on SiO_2/Al_2O_3yield to the same defect densities and energy distributions extracted using experimental techniques. Even the defect density in the SiO_2, when thin interfacial layers were simulated, had to be increased to mimic the presence of the intermixing layer.

Chapter VII: Conclusions

This dissertation illustrated the work carried out during the three years of my Ph.D. in the XXV cycleof the International Doctorate School in Information and Communication Technologies at the University of Modena and Reggio Emilia, Italy.

My research activity focused on the study of InGaAs MOSFETs for CMOS technology extension beyond the 16-nm node.

I started studying MOSFET devices with InGaAs channel, ZrO_2 gate dielectric, and implanted source/drain regions. The impact of interfacial traps on the electrical characteristics such as threshold voltage, subthreshold slope and on/off currents has been analyzed in both standard MOSFETs and capped MOSFETs. A detailed analysis of the effects of both acceptor and donor traps has been carried out, together with the explanation of the non-trivial behaviour induced by donor-like interface traps in capped MOSFETs.

Another field of investigation has been the optimization of the semiconductor stack composing buried-channel, InGaAs quantum-well MOSFETs with Al_2O_3 gate dielectric. Buried channel, implant-free MOSFETs are an option currently being intensively developed as an alternative to standard MOSFET structures, minimizing the channel mobility degradation induced by surface scattering and avoiding high-k dielectric degradation due to thermal cycles required for doping activation. Since both doping concentration/type and thicknesses of the layers forming the buried channel device play a key role in the device performance, I evaluated the impact of different device concepts to provide guidelines for device design and optimization.

Since the high mobility is the main reason why III-V semiconductor are being studied for Si replacement in the channel of next generation CMOS devices, it is of fundamental importance to assess the accuracy limits that affect the experimental techniques for mobility extraction. In particular my work addressed the accuracy of split-CV measurements applied to quantum-well MOSFETs with InGaAs channel and Al_2O_3 gate dielectric. Simulating the split-CV experimental method has made it possible to find and partially correct all possible errors (interfacial traps, contact resistances and extra capacitance term associated with buried channel) affecting mobility extraction.

Finally, within the framework of interface-trap characterization and extraction at the III-V/high-k interface and Si/SiO_2/high-k interface, I developed a new generalized technique for interface trap

extraction in III-V devices. The technique is based on combining together two well-known methods: the Terman method and the high-low frequency method. The method has been applied to interface-trap characterization in InGaAs MOSCAPs with Al_2O_3 gate dielectric.

On the other hand, charge pumping and "Trap Spectroscopy by Charge Injection and Sensing" techniques have been adopted to extract trap parameters at Si/SiO_2/high-k interfaces. Results have been compared with trap parameters derived from current leakage simulations obtaining a good match with experimental data.

Table VII.1 summarizes topics of my research activity on InGaAs MOSFETs and the related state-of-the-art advancements.

	State of the Art Advancements
Interface-Trap Effects	Analized the impact of different D_{it} concentrations for donor-/acceptor-like traps in capped/uncapped devices. Highlighted the non-conventional effect of donor-like traps in buried channel InGaAs MOSFETs.
QW-MOSFET Scaling	Provided guidelines for device scaling in terms of buffer doping optimization.
Split-CV Errors	Highlighted errors occurring in mobility extraction. Underestimation of mobility at high-V_{GS} due to barrier layer capacitance. Mobility drop for low V_{GS} is an artifact of the method.
D_{it} Characterization and Extraction	Developed a generalized technique allowing a self consistent extraction of $D_{it}(E)$ and Cox estimation. Implemented an automatic fitting procedure in MatLab.

Table VII.1: State-of-the-art advancements obtained and discussed in this dissertation.

Bibliography

[1] 2011 International Technology Roadmap for Semiconductor. [Online]. http://www.itrs.net/

[2] Y Taur and T Ning, *Fundamentals of Modern VLSI Devices.*: Cambidge Univ. Press, 1998.

[3] Y. P. Tsividis, *Operation and modeling of the MOS transistor*.: McGraw-Hill Book Co-Singapore, 1988.

[4] S.E. Laux and M.V. Fischetti, "Monte-Carlo simulation of submicrometer Si n-MOSFETs at 77 and 300 K," *Electron Device Letters, IEEE*, vol. 9, no. 9, pp. 467-469, Sept. 1988.

[5] M.R. Pinto, E. Sangiorgi, and J. Bude, "Silicon MOS transconductance scaling into the overshoot regime," *Electron Device Letters, IEEE*, vol. 14, no. 8, pp. 375-378, Aug. 1993.

[6] M.S. Lundstrom, "On the mobility versus drain current relation for a nanoscale MOSFET," *IEEE Electr. Dev. Lett.*, vol. 22, no. 6, pp. 293-295, June 2001.

[7] M. Lundstrom, "Elementary scattering theory of the Si MOSFET," *Electron Device Letters, IEEE*, vol. 18, no. 7, pp. 361-363, July 1997.

[8] S. Tyagi et al., "An advanced low power, high performance, strained channel 65nm technology," in *Electron Devices Meeting. IEDM Technical Digest. IEEE International*, 2005, pp. 245-247.

[9] F. Andrieu, T. Ernst, F. Lime, F. Rochette, K. Romanjek, S. Barraud, C. Ravit, F. Boeuf, M. Jurczak, M. Casse, O. Weber, L. Brevard, G. Reimbold, G. Ghibaudo, and S. Deleonibus, "Experimental and comparative investigation of low and high field transport in substrate- and process-induced strained nanoscaled MOSFETs," in *VLSI Technology, 2005. Digest of Technical Papers. Symposium on*, 2005, pp. 176-177.

[10] A. Khakifirooz and D.A. Antoniadis, "MOSFET Performance Scaling—Part I: Historical Trends," *Electron Devices, IEEE Transactions on*, vol. 55, no. 6, pp. 1391-1400, June 2008.

[11] M.K. Hudait, G. Dewey, S. Datta, J.M. Fastenau, J. Kavalieros, W.K. Liu, D. Lubyshev, R. Pillarisetty, W. Rachmady, M. Radosavljevic, T. Rakshit, and R. Chau, "Heterogeneuous integration of enhancement mode In0.7Ga0.3As quantum well transistor on Silicon substrate using thin composite buffer architecture for high-speed and low-voltage logic applications," in *IEDM Tech. Dig.*, 2007, pp. 625-628.

[12] Y. Xuan, Y.Q. Wu, T. Shen, T. Yang, and P.D. Ye, "High performance submicron inversion-type enhancement-mode InGaAs MOSFETs with ALD Al2O3, HfO2 and HfAlO as gate dielectrics," in *Electron Devices Meeting, 2007. IEDM 2007. IEEE International*, 2007, pp. 637-640.

[13] Y. Xuan, Y.Q. Wu, H.C. Lin, T. Shen, and P.D. Ye, "Submicrometer Inversion-Type Enhancement-Mode InGaAs MOSFET With Atomic-Layer-Deposited Al2O3 as Gate Dielectric," *Electron Device Letters, IEEE*, vol. 28, no. 11, pp. 935-938, Nov. 2007.

[14] M. Passlack et al., "High Mobility III-V MOSFETs For RF and Digital Applications," in *Electron Devices Meeting, 2007. IEDM 2007. IEEE International*, 2007, pp. 621-624.

[15] R.J.W. Hill, D.A.J. Moran, Xu Li, Haiping Zhou, D. Macintyre, S. Thoms, A. Asenov, P. Zurcher, K. Rajagopalan, J. Abrokwah, R. Droopad, M. Passlack, and I.G. Thayne, "Enhancement-mode GaAs MOSFETs with In0.3Ga0.7As channel; a mobility of over 5000 cm2/Vs; and transconductance of over 475 uS/um," *IEEE Electr. Dev. Lett.*, vol. 28, no. 12, pp. 1080-1082, Dec. 2007.

[16] I. Ok, H. Kim, M. Zhang, F. Zhu, S. Park, J Yum, H. Zhao, Domingo Garcia, Prashant Majhi, N. Goel, Tsai W., C. K. Gaspe, M. B. Santos, and Jack C. Lee, "Self-aligned n-channel metal-oxide-semiconductor field effect transistor on high-indium-content In0.53Ga0.47As and InP using physical vapor deposition HfO2 and silicon interface passivation layer," *Appl. Phys. Lett.*, vol. 92, p. 202903, 2008.

[17] Y. Sun, E.W. Kiewra, J.P. De Souza, J.J. Bucchignano, K.E. Fogel, D.K. Sadana, and G.G. Shahidi, "High-Performance -Channel MOSFETs With High- Gate Dielectrics and -Si Passivation," *Electron Device Letters, IEEE*, vol. 30, no. 1, pp. 5-7, Jan. 2009.

[18] M. Yokoyama, T. Yasuda, H. Takagi, H. Yamada, N. Fukuhara, M. Hata, M. Sugiyama, Y. Nakano, M. Takenaka, and S. Takagi, "High mobility metal S/D III–V-On-Insulator MOSFETs on a Si substrate using direct wafer bonding," in *VLSI Technology, 2009 Symposium on*, 2009, pp. 242-243.

[19] Han Zhao, Yen-Ting Chen, Jung Hwan Yum, Yanzhen Wang, Niti Goel, and Jack C. Lee, "High performance In0.7Ga0.3As metal-oxide-semiconductor transistors with mobility >4400 cm2/V s using InP barrier layer," *Applied Physics Letters*, vol. 94, no. 19, p. 193592, 2009.

[20] D. Lin et al., "Enabling the high-performance InGaAs/Ge CMOS: a common gate stack solution," in *IEDM Tech. Dig.*, 2009, pp. 327-330.

[21] Han-Chung Lin, Wei-E. Wang, Guy Brammertz, Marc Meuris, and Marc Heyns, "Electrical study of sulfur passivated In0.53Ga0.47As MOS capacitor and transistor with ALD Al2O3 as gate insulator," *Journal Microelectronic Engineering*, vol. 86, no. 7-9, pp. 1554-1557, July 2009.

[22] R.J.W. Hill, C. Park, J. Barnett, J. Price, J. Huang, N. Goel, W.Y. Loh, J. Oh, C.E. Smith, P. Kirsch, P. Majhi, and R. Jammy, "Self-aligned III-V MOSFETs heterointegrated on a 200 nm Si substrate using an industry standard process flow," in *IEDM Tech. Dig.*, 2010, pp. 130-133.

[23] H. Zhao, Y.-T. Chen, J.W. Yum, Y. Wang, F. Zhou. F. Xue, and J.C. Lee, "Effects of barrier layers on device performance of high mobility In0.7Ga0.3As metal-oxide-semiconductor field-effect-transistors," *Appl. Phys. Lett.*, vol. 96, p. 102101, 2010.

[24] Hock-Chun Chin, Xinke Liu, Xiao Gong, and Yee-Chia Yeo, "Silane and Ammonia Surface Passivation Technology for High-Mobility MOSFETs," *Electron Devices, IEEE Transactions on*, vol. 57, no. 5, pp. 973-979, May57 2010.

[25] M. Yokoyama, R. Iida, Sanghyeon Kim, N. Taoka, Y. Urabe, H. Takagi, T. Yasuda, H. Yamada, N. Fukuhara, M. Hata, M. Sugiyama, Y. Nakano, M. Takenaka, and S. Takagi, "Sub-10-nm Extremely Thin Body InGaAs-on-Insulator MOSFETs on Si Wafers With Ultrathin Buried Oxide Layers," *Electron Device Letters, IEEE*, vol. 32, no. 9, pp. 1218-1220, Sept. 2011.

[26] Fei Xue, Han Zhao, Yen-Ting Chen, Yanzhen Wang, Fei Zhou, and Jack C. Lee, "High-k InGaAs metal-oxide-semiconductor field-effect-transistors with various barrier layer materials," *Applied Physics Letters*, vol. 99, no. 3, p. 033507, 2011.

[27] Y. Yonai, T. Kanazawa, S. Ikeda, and Y. Miyamoto, "High drain current (>2A/mm) InGaAs channel MOSFET at VD=0.5V with shrinkage of channel length by InP anisotropic etching," in *Electron Devices Meeting (IEDM), 2011 IEEE International*, 2011, pp. 13.3.1-13.3.4.

[28] F. Xue, A. Jiang, H. Zhao, Y.-T. Chen, Y. Wang, F. Zhou, and J.C. Lee, "Sub-50-nm

In0.7Ga0.3As MOSFETs with various barrier layer materials," *IEEE Electr. Dev. Lett.*, vol. 33, no. 1, pp. 32-34, Jan. 2012.

[29] S.A.B. Suleiman, Hoon-Jung Oh, and Sungjoo Lee, "Effects of Plasma- Passivation on Mobility Degradation Mechanisms of nMOSFETs," *Electron Devices, IEEE Transactions on* , vol. 59, no. 5, pp. 1377-1384, May 2012.

[30] M. Egard, L. Ohlsson, M. Arlelid, K.-M. Persson, B.M. Borg, F. Lenrick, R. Wallenberg, E. Lind, and L.-E. Wernersson, "High-Frequency Performance of Self-Aligned Gate-Last Surface Channel MOSFET," *Electron Device Letters, IEEE*, vol. 33, no. 3, pp. 369-371, March 2012.

[31] Qiang Li, Xiuju Zhou, Chak Wah Tang, and Kei May Lau, "High-Performance Inverted MOSHEMTs on a GaAs Substrate With Regrown Source/Drain by MOCVD," *Electron Device Letters, IEEE*, vol. 33, no. 9, pp. 1246-1248, Sept. 2012.

[32] Xiuju Zhou, Qiang Li, Chak Wah Tang, and Kei May Lau, "30-nm Inverted MOSHEMTs on Si Substrate Grown by MOCVD With Regrown Source/Drain," *Electron Device Letters, IEEE*, vol. 33, no. 10, pp. 1384-1386, Oct. 2012.

[33] T.-W. Kim, D.-H. Kim, and J. del Alamo, "30 nm In0.7Ga0.3As inverted-type HEMTs with reduced gate leakage current for logic applications," in *IEDM Tech. Dig.*, 2009, pp. 483-486.

[34] G. Deway, R. Kotlyar, R. Pillarisetty, M. Radosavljevic, T. Rakshit, H. Then, and R. Chau, "Logic performance evaluation and transport physics of Schottky-gate III-V compound semiconductor quantum well field effect transistors for power supply voltages ranging from 0.5V to 1.0V," in *IEDM Tech. Dig*, 2009, pp. 487-490.

[35] M. Passlack, K. Rajagopalan, J. Abrokwah, and R. Droopad, "Implant-free high-mobility flatband MOSFET: principles of operation," *IEEE Trans. Electr. Dev*, vol. 53, no. 10, pp. 2454-2459, Oct. 2006.

[36] Y. Sun, E.W. Kiewra, J.P. de Souza, J.J. Bucchignano, K.E. Fogel, D.K. Sadana, and G.G. Shahidi, "Scaling of In0.7Ga0.3As buried-channel MOSFETs," in *IEDM Tech. Dig.*, 2008, pp. 367-370.

[37] M. Passlack, R. Droopad, P. Fejes, and L. Wang, "Electrical properties of Ga2O3/GaAs interfaces and GdGaO dielectrics in GaAs-based MOSFETs," *IEEE Electr. Dev. Lett.*, vol. 30, no. 1, pp. 2-4, Jan. 2009.

[38] U. Singisetti et al., "InGaAs channel MOSFETs with self-aligned InAs source/drain formed by MEE regrowth," *IEEE Electr. Dev. Lett.*, vol. 30, no. 11, pp. 1128-1130, Nov.

2009.

[39] M. Radosavljevic, B. Chu-Kung, S. Corcoran, G. Dewey, M.K. Hudait, J.M. Fastenau, J. Kavalieros, W.K. Liu, D. Lubyshev, M. Metz, K. Millard, N. Mukherjee, W. Rachmady, U. Shah, and R. Chau, "Advanced high-k gate dielectric for high-performance short-channel In0.7Ga0.3As quantum well field effect transistors on Silicon substrate for low power logic applications," in *IEDM Tech. Dig.*, 2009, pp. 319-322.

[40] F. Ren, J.M. Kuo, M. Hong, W.S. Hobson, J.R. Lothian, J. Lin, H.S. Tsai, J.P. Mannaerts, J. Kwo, S.N.G. Chu, Y.K. Chen, and A.Y. Cho, "Ga2O3(Gd2O3)/InGaAs enhancement-mode n-channel MOSFET's," *IEEE Electr. Dev. Lett.*, vol. 19, no. 8, pp. 309-31, Aug. 1998.

[41] T.D. Lin, H.C. Chiu, P. Chang, L.T. Tung, C.P. Chen, and M. Hong, "High-performance self-aligned inversion-channel In0.53Ga0.47As metal-oxide-semiconductor field-effect-transistor with Al2O3/Ga2O3(Gd2O3) as gate dielectrics," *Appl. Phys. Lett.*, vol. 93, p. 033516, 2008.

[42] J. Q. Lin, S.J. Lee, H.J. Oh, G.Q. Lo, D.L. Kwong, D.Z. Chi, J. Kwo, W. Tsai, and Wang Y. C., "Inversion-mode self-aligned In0.53Ga0.47As n-channel metal-oxide-semiconductor field-effect transistor with HfAlO gate dielectric and TaN metal gate," *IEEE Electr. Dev. Lett.*, vol. 29, no. 9, pp. 977-980, Sept. 2008.

[43] Hock-Chun Chin, Ming Zhu, Zhi-Chien Lee, Xinke Liu, Kian-Ming Tan, Hock Koon Lee, Luping Shi, Lei-Jun Tang, Chih-Hang Tung, Guo-Qiang Lo, Leng-Seow Tan, and Yee-Chia Yeo, "A new silane-ammonia surface passivation technology for realiziang inversion-type surface-channel GaAs N-MOSFET with 160 gate length and high-quality metal-gate/high-k dielectric stack," in *IEDM Tech. Dig.*, 2008, pp. 383-386.

[44] Y.Q. Wu, W.K. Wang, O. Koybasi, D.N. Zakharov, E.A. Stach, S. Nakahara, J.C.M. Hwang, and P.D. Ye, "0.8-V supply voltage deep-submicrometer inversion-mode In0.75Ga0.25As MOSFET," *IEEE Electr. Dev. Lett.*, vol. 30, no. 7, pp. 700-702, July 2009.

[45] H.-C. Chin, X. Gong, X. Liu, and Y.-C. Yeo, "Lattice-mismatched In0.4Ga0.6As source/drain stressors with in situ doping for strained In0.53Ga0.47As channel n-MOSFETs," *IEEE Electr. Dev. Lett.*, vol. 30, no. 8, pp. 805-807, Aug. 2009.

[46] Y.Q. Wu, M. Xu, R.S. Wang, O. Koybasi, and P.D. Ye, "High performance deep-submicron inversion-mode InGaAs MOSFETs with maximum Gm exceeding 1.1 mS/um: new HBr pretreatment and channel engineering," in *IEDM Tech. Dig.*, 2009, pp. 323-326.

[47] J. Huang, N. Goel, H. Zhao, C.Y. Kang, K.S. Min, G. Bersuker, S. Oktyabrsky, C.K. Gaspe, M.B. Santos, P. Majhi, P.D. Kirsch, H.-H. Tseng, J.C. Lee, and R. Jammy, "InGaAs MOSFET performance and reliability improvement by simultaneous reduction of oxide and interface charge in ALD (La)AlOx/ZrO2 gate stack," in *IEDM Tech. Dig.*, 2009, pp. 335-338.

[48] H.J. Oh, J.Q. Lin, S.A.B. Suleiman, G.Q. Lo, D.L. Kwong, D.Z. Chi, and S.J. Lee, "Thermally robust phosphorous nitride interface passivation for InGaAs self-aligned gate-first n-MOSFET integrated with high-k dielectric," in *IEDM Tech. Dig.*, 2009, pp. 339-342.

[49] M.V. Fischetti, T.P. O'Regan, S. Narayanan, C. Sachs, S. Jin, J. Kim, and Y. Zhang, "Theoretical study of some physical aspects of electronic transport in nMOSFETs at the 10-nm gate-length," *IEEE Trans. Electr. Dev.*, vol. 54, no. 9, pp. 2116-2136, Sept. 2007.

[50] D. Jin, D. Kim, T. Kim, and J. del Alamo, "Quantum capacitance in scaled down III-V FETs," in *IEDM Tech. Dig.*, 2009, pp. 495-498.

[51] M.J.W. Rodwell et al., "III-V MOSFETs: scaling laws; scaling limit; fabrication processes," in *Proc. 2010 International Conference on Indium Phospide and Related Materials (IPRM)*, 2010, pp. 25-30.

[52] N. Goel et al., "Addressing the gate stack challenge for high mobility InxGa1-xAs channels for NFETs," in *IEDM Tech. Dig.*, 2008, pp. 363-366.

[53] S. Koveshnikov, N. Goel, P. Majhi, H. Wen, M.B. Santos, S. Oktyabrsky, V. Tokranov, R. Kambhampati, R. Moore, F. Zhu, J. Lee, and W. Tsai, "In0.53Ga0.47As based metal oxide semiconductor capacitors with atomic layer deposition ZrO2 gate oxide demonstrating low gate leakage current and equivalent oxide thickness less than 1 nm," *Appl. Phys. Lett.*, vol. 92, p. 222904, 2008.

[54] Neophytou, T. Rakshit, and M.S. Lundstrom, "Performance analysis of 60-nm gate-length III-V InGaAs HEMTs: simulations versus experiments," *IEEE Trans. Electr. Dev.*, vol. 56, no. 7, pp. 1377-1387, July 2009.

[55] T. Mimura and M. Fukuta, "Status of the GaAs metal-oxide-semiconductor technology," *IEEE Trans. Electr. Dev.*, vol. 55, no. 6, pp. 1147-1155, June 1908.

[56] M. Xu, K. Xu, R. Contreras, M. Milojevic, T. Shen, O. Koybasi, Y.Q. Wu, R.M. Wallace, and P.D. Ye, "New insight into Fermi-level unpinning on GaAs: impact of different surface orientations," in *IEDM Tech. Dig.*, 2009, pp. 865-868.

[57] D. Varghese, Y. Xuan, Y.Q. Wu, T. Shen, P.D. Ye, and M.A. Alam, "Multi-probe

interface characterization of In0.65Ga0.35As/Al2O3 MOSFET," in *IEDM Tech. Dig.*, 2008, pp. 379-382.

[58] J. Robertson, "Model of interface states at III-V oxide interfaces," *Appl. Phys. Lett.*, vol. 94, p. 152104, 2009.

[59] G. Brammertz, H.-C. Lin, M. Caymax, M. Meurius, M. Heyns, and M. Passlack, "On the interface state density at In0.53Ga0.47As/oxide interfaces," *Appl. Phys. Lett.*, vol. 92, p. 202109, 2009.

[60] N. Wrachien, A. Cester, E. Zanoni, G. Meneghesso, Y.Q. Wu, and P.D. Ye, "Degradation of III-V inversion-type enhancement-mode MOSFETs," in *Proc. of the 48th IEEE International Reliability Physics Symposium (IRPS)*, 2010, pp. 536-542.

[61] L. Morassi, G. Verzellesi, A. Padovani, L. Larcher, P. Pavan, D. Veksler, I. Ok, and G. Bersuker, "Analysis of interface-trap effects in inversion-type InGaAs/ZrO2 MOSFETs," in *Proc. of the 48th IEEE International Reliability Physics Symposium (IRPS)*, 2010, pp. 532-535.

[62] Synposys Inc., *Dessis-8.0 User Manual*.

[63] Synposys Inc., *Sentaurus User Manual*.

[64] P. Bhattacharya, *Properties of lattice-matched and strained Indium Gallium Arsenide.*: EMIS Data Reviews Series No. 8, 1993.

[65] W. Wang J. Deng, J.C.M Hwang, Y. Xuan, Y. Wu, and P.D. Ye, "Charge-pumping characterization of interface traps in Al2O3/In0.75Ga0.25As metal-oxide-semiconductor field-effect transistors," *Appl. Phys. Lett.*, vol. 96, p. 072102, 2010.

[66] T.H. Chiang, W.C. Lee, T.D. Lin, D. Lin, K.H. Shiu, J. Kwo, W.E. Wang, W. Tsai, and M. Hong, "Approaching Fermi level unpinning in oxide-In0.2Ga0.8As," in *IEDM Tech. Dig.*, 2008, pp. 375-378.

[67] Y.Q. Wu, M. Xu, R.S. Wang, O. Koybasi, and P.D. Ye, "High performance inversion-type enhancement-mode InGaAs MOSFET with maximum drain current exceeding 1 A/mm," *IEEE Electr. Dev. Lett.*, vol. 29, no. 4, pp. 294-296, Apr. 2008.

[68] Y.-T. Chen, Y. Wang, F. Xue, F. Zhou, and J.C. Lee, "Physical and electrical analysis of post-HfO2 flourine plasma treatment for the improvement of In0.53Ga0.47As MOSFETs' performance," *IEEE Trans. Electr. Dev.*, vol. 59, no. 1, pp. 139-144, Jan. 2012.

[69] M. Radosavljevic et al., "Non-planar; multi-gate InGaAs quantum well field effect

transistors with high-k gate dielectric and ultra-scaled gate-to-drain/gate-to-source separation for low power logic applications," in *IEDM Tech. Dig.*, 2010, pp. 126-129.

[70] T.P. O'Regan, M.V. Fischetti, B. Sorée, S. Jin, W. Magnus, and M. Meuris, "Calculation of the electron mobility in III-V inversion layers with high-k dielectrics," *Journal of Applied Physics*, vol. 108, p. 103705, 2010.

[71] Y. Xuan, P. Ye, and T. Shen, "Substrate engineering for high-performance surface-channel III-V metal-oxide-semiconductor field-effect transistors," *Appl. Phys. Lett.*, vol. 91, p. 232107, 2007.

[72] L. Morassi, G. Verzellesi, H. Zhao, J.C. Lee, D. Veksler, and G. Bersuker, "Errors Limiting Split-CV Mobility Extraction Accuracy in Buried-Channel InGaAs MOSFETs," *IEEE Trans. Electr. Dev.*, vol. 59, no. 4, pp. 1068-1075, Apr. 2012.

[73] T. Sawada, K. Numata, S. Tohdoh, and T. Saitoh, "In-situ characterization of compound semiconductor surfaces by novel photoluminescence surface state spectroscopy," *Journal of Applied Physics*, vol. 32, pp. 511-517, 1993.

[74] L. Morassi, G. Verzellesi, P. Pavan, D. Veksler, I. Ok, H. Zhao, J.C. Lee, and G. Bersuker, "Experimental/numerical investigation of buried-channel InGaAs MOS-HEMTs with Al2O3 gate dielectric," in *Proc. of the 23th International Conference on Indium Phosphide and Related Materials (IPRM 2011)*, 2011, pp. 103-105.

[75] S.J. Bentley, M. Holland, X. Li, G.W. Paterson, H. Zhou, O. Ignatova, D. Macintyre, S. Thoms, A. Asenov, B. Shin, J. Ahn, P.C. McIntry, and I.G. Thaine, "Electron mobility in surface- and buried-channel flatband In0.53Ga0.47As MOSFETs with ALD Al2O3 gate dielectric," *IEEE Electr. Dev. Lett.*, vol. 32, no. 4, pp. 494-496, April 2011.

[76] L. Morassi, A. Padovani, G. Verzellesi, D. Veksler, I. Ok, and G. Bersuker, "Interface-trap effects in inversion-type enhancement-mode InGaAs/ZrO2 n-channel MOSFETs," *IEEE Trans. Electr. Dev.*, vol. 58, no. 1, pp. 107-114, Jan. 2011.

[77] C.G. Sodini, T.W. Ekstedt, and J.L. Moll, "Charge accumulation and mobility in thin dielectric MOS transistors," *Solid-State Electronics*, vol. 25, no. 9, pp. 833-841, 1982.

[78] W. Zhu, J.-P. Han, and T.P. Ma, "Mobility measurement and degradation mechanisms of MOSFETs made with ultrathin high-k dielectrics," *IEEE Trans. Electr. Dev.*, vol. 51, no. 1, pp. 98-105, Jan. 2004.

[79] C.L. Hinkle, A.M. Sonnet, R.A. Chapman, and E.M. Vogel, "Extraction of the effective mobility of In0.53Ga0.47As MOSFETs," *IEEE Electr. Dev. Lett.*, vol. 30, no. 4, pp. 316-318, April 2009.

[80] A. Ali, H. Madan, S. Koveshnikov, S. Oktyabrsky, R. Kambhampati, T. Heeg, D. Schlom, and S. Datta, "Small-signal response of inversion layers in high-mobility In0.53Ga0.47As MOSFETs made with thin high-k dielectrics," *IEEE Trans. Electr. Dev.*, vol. 57, no. 4, pp. 742-748, April 2010.

[81] D. Kuzum, T. Krishnamohan, A. Nainani, Y. Sun, P.A. Pianetta, H.-S.P. Wong, and K.C. Saraswat, "High-mobility Ge N-MOSFETs and mobility degradation mechanisms," *IEEE Trans. Electr. Dev.*, vol. 58, no. 1, pp. 59-66, Jan. 2011.

[82] Ioffe Institute. New Semiconductor Materials Characteristics and Properties. [Online]. http://www.ioffe.ru/SVA/NSM/

[83] K. Choi, H. N. Alshareef, H. C. Wen, H. Harris, H. Luan, Y. Senzaki, P. Lysaght, P. Majhi, and B. H. Leef, "Effective work function modification of atomic-layer-deposited-TaN film by capping layer," *Appl. Phys. Lett.*, vol. 89, p. 032113, 2006.

[84] L. M. Terman, *Solid State Electrons*, vol. 5, p. 285, 1962.

[85] C. N. Berglund, *IEEE Trans. Electron Devices*, vol. 13, p. 701, 1966.

[86] R. Castagnè and A. Vapaille, *Surf. Sci.*, vol. 28, p. 157, 1971.

[87] G. Brammertz, A. Alian, D.H.-C. Lin, M. Meuris, M. Caymax, and W.-E. Wang, "A Combined Interface and Border Trap Model for High-Mobility Substrate Metal–Oxide–Semiconductor Devices Applied to and InP Capacitors," *Electron Devices, IEEE Transactions on*, vol. 58, no. 11, pp. 3890-3897, Nov. 2011.

[88] K. Martens, Chi On Chui, G. Brammertz, B. De Jaeger, D. Kuzum, M. Meuris, M. Heyns, T. Krishnamohan, K. Saraswat, H.E. Maes, and G. Groeseneken, "On the Correct Extraction of Interface Trap Density of MOS Devices With High-Mobility Semiconductor Substrates," *Electron Devices, IEEE Transactions on*, vol. 55, no. 2, pp. 547-556, Feb. 2008.

[89] H. Madan, D. Veksler, Y. T. Chen, J. Huang, N. Goel, G. Bersuker, and S. Datta, "Interface states at high-κ/InGaAs interface: H2O vs. O3 based ALD dielectric," in *Device Research Conference (DRC)*, 2011, pp. 117-118.

[90] Yu Yuan, Lingquan Wang, Bo Yu, Byungha Shin, Jaesoo Ahn, P.C. McIntyre, P.M. Asbeck, M.J.W. Rodwell, and Yuan Taur, "A Distributed Model for Border Traps in MOS Devices," *Electron Device Letters, IEEE*, vol. 32, no. 4, pp. 485-487, April 2011.

[91] R. Engel-Herbert, Y.e Hwang, and S. Stemmer, "Comparison of methods to quantify interface trap densities at dielectric/III-V semiconductor interfaces," *Journal of Applied*

Physics, vol. 108, p. 124101, 2010.

[92] I. Krylov, L. Kornblum, A. Gavrilov, D. Ritter, and M. Eizenberg, "Experimental evidence for the correlation between the weak inversion hump and near midgap states in dielectric/InGaAs interfaces," *Appl. Phys. Lett*, vol. 100, p. 173508, 2012.

[93] R. Engel-Herbert, Y.e Hwang, and S. Stemmer, "Quantification of trap densities at dielectric/III–V semiconductor interfaces," *Appl. Phys. Lett.*, vol. 97, p. 062905, 2010.

[94] J.S. Brugler and P.G.A. Jespers, "Charge pumping in MOS devices," *Electron Devices, IEEE Transactions on*, vol. 16, no. 3, pp. 297- 302, Mar. 1969.

[95] M.B. Zahid, R. Degraeve, M. Cho, L. Pantisano, D.R. Aguado, J. Van Houdt, G. Groeseneken, and M. Jurczak, "Defect profiling in the SiO2/ Al2O3 interface using Variable Tcharge-Tdischarge Amplitude Charge Pumping (VT2ACP)," in *Reliability Physics Symposium, 2009 IEEE International*, 2009, pp. 21-25.

[96] R. Degraeve, M. Cho, B. Govoreanu, B. Kaczer, M.B. Zahid, J. Van Houdt, M. Jurczak, and G. Groeseneken, "Trap Spectroscopy by Charge Injection and Sensing (TSCIS): A quantitative electrical technique for studying defects in dielectric stacks," in *Electron Devices Meeting IEDM*, 2008, pp. 1-4.

[97] B.J. O'Sullivan, V.S. Kaushik, L.-A. Ragnarsson, L. Trojman, B. Onsia, N. Van Hoornick, E. Rohr, S. DeGendt, and M. Heyns, "Cross-wafer controlled interface layer thickness variation, and its application to SiO2 / high-κ stack characterisation," in *Proceeding of the 36th European Device Research Conference ESSDERC*, 2006, pp. 395-398.

[98] B.J. O'Sullivan, V.S. Kaushik, L.-A. Ragnarsson, B. Onsia, N. Van Hoornick, E. Rohr, S. DeGendt, and M. Heyns, "Device performance of transistors with high-κ dielectrics using cross-wafer-scaled interface-layer thickness," *Electron Device Letters, IEEE*, vol. 27, no. 7, pp. 546- 548, July 2006.

[99] V.S. Kaushik, B.J. O'Sullivan, G. Pourtois, N. Van Hoornick, A. Delabie, S. Van Elshocht, W. Deweerd, T. Schram, L. Pantisano, E. Rohr, L.-A. Ragnarsson, S. De Gendt, and M. Heyns, "Estimation of fixed charge densities in hafnium-silicate gate dielectrics," *Electron Devices, IEEE Transactions on*, vol. 53, no. 10, pp. 2627-2633, Oct. 2006.

[100] L Larcher, "Statistical simulation of leakage currents in MOS and flash memory devices with a new multiphonon trap-assisted tunneling model," *Electron Devices, IEEE Transactions on*, vol. 50, no. 5, pp. 1246- 1253, May 2003.

[101] A. Padovani, L. Larcher, S. Verma, P. Pavan, P. Majhi, P. Kapur, K. Parat, G. Bersuker, and K. Saraswat, "Statistical Modeling of Leakage Currents Through SiO2/High-κ Dielectrics Stacks for Non-Volatile Memory Applications," in *IEEE International Reliability Physics Symposium IRPS* , 2008, pp. 616-620.

[102] D.-H. Kim and J. del Alamo, "Lateral and vertical scaling of In0.7Ga0.3As HEMTs for post-Si-CMOS logic applications," *IEEE Trans. Electr. Dev.*, vol. 55, no. 10, pp. 2546-2553, Oct. 2008.

[103] Dae-Hyun Kim, J.A. del Alamo, Jae-Hak Lee, and Kwang-Seok Seo, "Logic Suitability of 50-nm In0.7 Ga0.3As HEMTs for Beyond-CMOS Applications," *Electron Devices, IEEE Transactions on*, vol. 54, no. 10, pp. 2606-2613, Oct. 2007.

[104] K. Kalna, N. Seoane, A.J. Garcia-Loureiro, I.G. Thayne, and A. Asenov, "Benchmarking of Scaled InGaAs Implant-Free NanoMOSFETs," *Electron Devices, IEEE Transactions on*, vol. 55, no. 9, pp. 2297-2306, Sept. 2008.

[105] Dae-Hyun Kim and J.A. del Alamo, "Lateral and Vertical Scaling of HEMTs for Post-Si-CMOS Logic Applications," *Electron Devices, IEEE Transactions on*, vol. 55, no. 10, pp. 2546-2553, Oct. 2008.

[106] M.J.W. Rodwell et al., "III-V MOSFETs: Scaling laws, scaling limits, fabrication processes," in *Indium Phosphide & Related Materials (IPRM), International Conference on*, 2010, pp. 1-6.

[107] Dae-Hyun Kim and J.A. del Alamo, "Scalability of Sub-100 nm InAs HEMTs on InP Substrate for Future Logic Applications," *Electron Devices, IEEE Transactions on*, vol. 57, no. 7, pp. 1504-1511, July 2010.

[108] G. Doornbos and M. Passlack, "Benchmarking of III–V n-MOSFET Maturity and Feasibility for Future CMOS," *Electron Device Letters, IEEE*, vol. 31, no. 10, pp. 1110-1112, Oct. 2010.

[109] A. Khakifirooz and D.A. Antoniadis, "MOSFET Performance Scaling—Part II: Future Directions," *Electron Devices, IEEE Transactions on*, vol. 55, no. 6, pp. 1401-1408, June 2008.

[110] H. Tsuchiya and S. Takagi, "Influence of Elastic and Inelastic Phonon Scattering on the Drive Current of Quasi-Ballistic MOSFETs," *Electron Devices, IEEE Transactions on*, vol. 55, no. 9, pp. 2397-2402, Sept. 2008.

[111] Hang Hu, J.B. Jacobs, L.T. Su, and D.A. Antoniadis, "A study of deep-submicron MOSFET scaling based on experiment and simulation," *Electron Devices, IEEE*

Transactions on, vol. 42, no. 4, pp. 669-677, Apr. 1995.

[112] Kenji Natori, "Ballistic metal-oxide-semiconductor field effect transistor," *Journal of Applied Physics*, vol. 76, p. 4879, 1994.

[113] Y Tsvidis, *Operation and Modeling of the MOS Transistor*, 2nd ed.: WCB/Mc-Graw-Hill, 1999.

Author's Publications

Journals

[J1] A. Padovani, L. Morassi, N. Raghavan, L. Larcher, Liu Wenhu, Kin Leong Pey,G. Bersuker, "A Physical Model for Post-Breakdown Digital Gate Current Noise," *Electron Device Letters, IEEE* , vol.31, no.9, pp.1032-1034, Sept. 2010.

[J2] L. Morassi, A. Padovani, G. Verzellesi, D. Veksler, Ok Injo G. Bersuker, "Interface-Trap Effects in Inversion-Type Enhancement-Mode N-Channel MOSFETs," *Electron Devices, IEEE Transactions on* , vol.58, no.1, pp.107-114, Jan. 2011.

[J3] G. Bersuker, D. Veksler, C. D. Young, H. Park, W. Taylor, P. Kirsch, R.Jammy, L. Morassi, A. Padovani, L. Larcher, "Connecting electrical and structural dielectric characteristics," *International Journal of High Speed Electronics and Systems (IJHSES)*, vol. 20(1), pp. 65-79, 2011.

[J4] L. Morassi, G.Verzellesi, H. Zhao, J. C. Lee, D. Veksler, G. Bersuker, "Errors Limiting Split-CV Mobility Extraction Accuracy in Buried-Channel InGaAs MOSFETs," *Electron Devices, IEEE Transactions on* , vol.59, no.4, pp.1068-1075, April 2012.

[J5] L. Morassi, G. Verzellesi, H. Zhao, J. C. Lee, D. Veksler, G. Bersuker, "Engineering Barrier and Buffer Layers in InGaAs Quantum-Well MOSFETs," *Electron Devices, IEEE Transactions on* , vol.59, no.12, pp.3651-3654, Dec. 2012.

Conference Proceedings

[C1] L. Morassi, L. Larcher, L. Pantisano, A. Padovani, R.Degreave, M. B.Zahid, B. J. O'Sullivan, "Advanced high-k materials and electrical analysis for memories: the role of SiO2-high-k dielectric intermixing," *41th International Conference on Solid State Devices and Materials (SSDM2009)*, 2009.

[C2] G. Bersuker, D.Heh, C. D. Young, L. Morassi, A. Padovani, L. Larcher, K. S. Yew, Y. C. Ong, D. S Ang, K. L. Pey, W. Taylor, "Mechanism of high-k dielectric-induced breakdown of the interfacial SiO2 layer," *Reliability Physics Symposium (IRPS), 2010*

IEEE International, vol., no., pp.373-378, 2-6 May 2010.

[C3] G. Bersuker, D.Veksler, C. D. Young, H. Park, L. Morassi, A. Padovani, L.Larcher, W. Taylor, P. D. Kirsch, R. Jammy, "Connecting electrical and structural dielectric characteristics," *Advanced Workshop on 'Frontiers in Electronics' (WOFE 2009)*, Dec. 13-16, 2009.

[C4] L. Morassi, G. Verzellesi, A. Padovani, L. Larcher, P. Pavan, D. Veksler, Ok Injo, G. Bersuker, "Analysis of interface-trap effects in inversion-type InGaAs/ZrO2 MOSFETs," *Reliability Physics Symposium (IRPS), 2010 IEEE International*, vol., no., pp.532-535, 2-6 May 2010.

[C5] L. Morassi, A.Padovani, G. Verzellesi, D. Veksler, Ok Injo, G. Bersuker, "Study of the Impact of Interface Traps on the Electrical Characteristics of InGaAs-based MOSFETs and MOSHEMTs with high-k Gate Dielectrics", *19th European Workshop on Heterostructure Technology (HETEC2010)*, Oct. 18-20, 2010.

[C6] L. Morassi, G. Verzellesi, P. Pavan, D.Veksler, Ok Injo, Han Zhao, J. C. Lee, G. Bersuker, "Experimental/numerical investigation of buried-channel InGaA MOS-HEMTs with Al2O3 gate dielectric," *Compound Semiconductor Week (CSW/IPRM), 2011 and 23rd International Conference on Indium Phosphide and Related Materials*, vol., no., pp.1-3, 22-26 May 2011.

[C7] L. Morassi, G. Verzellesi, L. Larcher, Han Zhao, J. C. Lee, "Errors affecting split-CV mobility measurements in InGaAs MOS-HEMTs," *Compound Semiconductor Week (CSW/IPRM), 2011 and 23rd International Conference on Indium Phosphide and Related Materials*, vol., no., pp.1-3, 22-26 May 2011.

[C8] L. Morassi, D. Veksler, G. Bersuker, G. Verzellesi, "Generalized High-Low frequency CV technique for interface-trap characterization at III-V/high-k interface," *11th Expert Evaluation & Control of Compound Semiconductor Materials & Technologies (EXMATEC)*, May 30 - Jun 1, 2012.

[C9] M. Mohamad Isa, D. Saguatti, A.Chini, L. Morassi, G. Verzellesi, M. Missous, "Field-Plated InGaAs-InAlAspHEMTs with 18-V off-state breakdown voltage and 35-GHz fmax," *36th Workshop on Compound Semiconductor Devices and Integrated Circuits (WOCSDICE)*, May 28-30, 2012.

[C10] T.-W. Kim, R. J. W. Hill, C. D. Young, D. Veksler, L. Morassi, S. Oktyabrsky, J. Oh, C. Y. Kang, D.-H Kim, J. A. del Alamo, C. Hobbs, P. D. Kirsch, R. Jammy, "InAs quantum-well MOSFET (Lg = 100 nm) with record high gm, fT and fmax," *VLSI Technology (VLSIT), 2012 Symposium on*, vol., no., pp.179-180, 12-14 June 2012.

[C11] L. Morassi, D. Veksler, G. Bersuker, G. Verzellesi, " Interface-trap characterization at

III-V/high-k interface: a fast and generalized method based on High-Low frequency CV," *21st European Workshop on Heterostructure Technology (HETECH)*, Nov 5-7, 2012.