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Characterization of Wide-Band-Gap Semiconductor Power Devices

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Alla mia famiglia
e ai miei amici

Contents

Abstract

This thesis discusses the characterization of devices based on wide-bandgap semiconductors. Such devices are of particular interest for high-power and high-frequency applications, and to date there are already commercially available devices based on Silicon Carbide (SiC) and Gallium Nitride (GaN) that have the potential to provide performance well above conventional Silicon (Si) technology. Nevertheless, the presence of trapping and de-trapping phenomena occurring within SiC and GaN materials limit the performance of such devices well below expectations. For this reason, this dissertation focuses on the characterization of trapping and de-trapping phenomena occurring in these devices, with the aim of studying the physical underlying mechanisms. To do so, various characterization techniques such as pulsed measurements, current transients and on-the-fly characterization are used. Particularly, a new system is presented for the on-the-fly characterization of on-state resistance (R_{ON}) and threshold voltage (V_{TH}) drifts that occur during switching operations. This system was employed for the characterization of SiC and GaN devices, highlighting the V_{TH} instabilities in SiC (Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) and the R_{ON} degradation in GaN High Electron Mobility Transistors (HEMTs). In the former, traps at the SiC/SiO_2 interface are identified as the main cause of the instability, while in the latter case, acceptor traps in the buffer layer are considered as the main cause of the increase in on-resistance due to the Drain voltage applied in off-state. These traps are introduced by Carbon doping that is normally used to make the buffer semi-insulating and reduce leakage in GaN devices for power applications. In case of RF applications, this dopant can be replaced by a different dopant species such as Iron. Such doping, however, also introduces trap states into the GaN-buffer which are in turn responsible for drain current collapse. To study this type of trap states, both pulsed measurements and current transient measurements can be used. The first technique was applied to highlight the presence of trapping phenomena and investigate the effect of said deep levels on the breakdown voltage stability of tested devices. The second technique, on the other hand, was used to investigate the effect of the electric field and self-heating on the emission dynamics from such traps. In particular, it is shown how an increase in temperature in the device, due to self-heating, leads to an acceleration of the emission from such trap states. The observed correlation between temperature and the dynamics of traps allowed the implementation of a novel technique for estimating the temperature within GaN devices, the accuracy of which is in line with state-of-the-art techniques.

Sommario

In questa tesi viene discusso il tema della caratterizzazione di dispositivi basati su semiconduttori ad elevato gap energetico. Tali dispositivi sono di particolare interesse per applicazioni ad elevata potenza ed alta frequenza e ad oggi vi sono già in commercio dispositivi basati su Carburo di Silicio (SiC) e Nitruro di Gallio (GaN) che hanno il potenziale per fornire prestazioni ben al di sopra rispetto alla convenzionale tecnologia in Silicio (Si). Nonostante ciò, la presenza di fenomeni di trapping e de-trapping che si verificano all'interno di dispositivi in SiC e GaN, limitano le prestazioni di tali dispositivi ben al di sotto rispetto alle aspettative. Per tale ragione, questa dissertazione si concentra sulla caratterizzazione dei fenomeni di trapping e de-trapping che avvengono nei dispositivi in questione, con lo scopo di studiare i meccanismi fisici alla loro base. Per fare ciò, vengono utilizzate diverse tecniche di caratterizzazione come misure impulsate, transienti di corrente e caratterizzazione on-the-fly. In particolare, viene presentato un nuovo sistema per la caratterizzazione on-the-fly dei drift di resistenza di on-state (R_{ON}) e tensione di soglia (V_{TH}) che avvengono durante le operazioni in commutazione. Tale sistema è stato impiegato per la caratterizzazione di dispositivi SiC e GaN, mettendo in luce le instabilità della tensione di soglia nel caso SiC e della R_{ON} nel caso GaN. Nel primo caso, le trappole all'interfaccia SiC/SiO_2 vengono identificate come la principale causa d'instabilità, mentre nel secondo caso, le trappole di tipo accettore all'interno del buffer sono considerate come principale causa dell'aumento di resistenza dovuta alla tensione di Drain applicata in off-state. Ciò è dovuto al drogaggio Carbon che viene normalmente utilizzato per rendere il buffer semi-isolante e ridurre il leakage nei dispositivi GaN utilizzati per applicazioni di potenza. Nel caso di applicazioni RF, tale drogaggio può essere sostituito da una diversa specie drogante come il ferro. Anche tale drogaggio, però, introduce stati trappola nel GaN-buffer che sono a loro volta responsabili per il collasso della corrente di Drain. Per studiare questo tipo di stati trappola, è possibile utilizzare sia misure impulsate che i transienti di corrente. La prima tecnica è stata applicata per mettere in luce la presenza dei fenomeni di intrappolamento ed investigare l'effetto della dinamica di tali trappole sulla stabilità della tensione di breakdown dei dispositivi testati. La seconda tecnica, invece, è stata utilizzata per studiare l'effetto del campo elettrico e dell'auto-riscaldamento sulla dinamica di emissione da tali trappole. In particolare, viene mostrato come un aumento di temperatura nel dispositivo, dovuto all'auto-riscaldamento, porta ad un'accelerazione dell'emissione da tali stati trappola. La correlazione osservata tra temperatura e dinamica di tali stati trappola, ha permesso di implementare una nuova tecnica di stima della temperatura all'interno di dispositivi in GaN, la cui accuratezza è risultata in linea con le tecniche allo stato dell'arte.

1 Introduction

1.1 Wide-Bandgap Semiconductor Devices

Wide-Bandgap Semiconductors (WBGs) are semiconductor materials that present a large energy gap (E_G) between their valence band (E_V) and conduction band (E_C). This physical property yields many advantages for WBGs devices compared to conventional Silicon-based technology. Particularly, the wide-bandgap enables the device's operation at higher voltages, frequency and temperatures, which makes them particularly attractive for both radio-frequency (RF) and power applications [1-3]. In fact, the ability to withstand higher temperatures, allows the operation at relatively high power densities, or equivalently, it allows to decrease the chip size for the same peak power. At the same time, the large energy gap gives an increased critical electric field, which allows operations at higher voltage levels, thanks to an increased blocking capability.

Among the WBGs available at present, those that are currently dominating the market are Gallium Nitride and Silicon Carbide. In Table 1.1, the main physical parameters of these two WBG materials are compared with those featured by conventional Silicon technology.

Table 1.1: Main parameters related to high-frequency and power performances for Silicon (Si), Silicon Carbide (4H-SiC) and Gallium Nitride (GaN).

Parameter	**Si**	**4H-SiC**	**GaN**
Bandgap E_G (eV)	1.12	3.26	3.39
Critical Field E_{crit} (MV/cm)	0.23	3	3.3
Electron Mobility μ_n (cm^2/Vs)	1400	700	1400
Saturation Velocity v_{sat} (10^7 cm/s)	1	2	2.5
Permittivity ε_r	11.8	9.7	9
Thermal Conductivity λ (W/cmK)	1.5	3.8	1.3
Johnson's FOM	0.014	5.7	10.8
Baliga's FOM	126	6300	13000

Thanks to their large energy gap, GaN and SiC outperform Si in high temperature operation and achieve higher breakdown electric field values. In fact, the breakdown voltage is in first approximation determined by the electric field that yield to impact ionization, which mainly depends on the energy gap.

The Figure of Merit conventionally used for comparing semiconductor materials in terms of high-power and high-speed capabilities are the Johnson's and the Baliga's figure of merit [4,5]. These two key parameters depend on the critical electric field, carrier mobility (μ_n) and saturation velocity (v_{sat}) of the material.

In fact, the Jonson's figure of merit (JFOM) is defined as [4]:

$$JFOM = \frac{(v_{sat} \times E_{crit})^2}{2\pi} \tag{1.1}$$

Whereas the Baliga's figure of merit (BFOM) can be written as [5]:

$$BFOM = \mu_n \times E_{crit}^{\ 2} \tag{1.2}$$

As highlighted in table 1.1, these figure of merit are higher for both GaN and SiC compared to Silicon. This further confirms that these WBGs are particularly promising for both radio-frequency and power switching applications. Concerning the latter, it is of paramount importance to have devices experiencing low switching and conductions losses in order to obtain relatively high efficiency levels in switching converters [6]. In order to obtain both low switching and low conduction losses, devices presenting low R_{ON}xQ_G product are required.

1.1.1 On-state resistance (R_{ON}) and Gate Charge (Q_G)

While operating in power switching applications, devices are continuously switched between a high voltage off-state condition and a low voltage on-state one. Particularly, during the off-state conditions, the device should ideally behave as an open circuit at which the ability to withstand relatively high voltages can be achieved by devices presenting high breakdown voltages and low leakage currents. On the other hand, during the on-state phase, the device should ideally behave as a short circuit, presenting the lowest possible R_{ON} in order to reduce as much as possible the conduction losses. In the real case, it is clearly impossible to obtain a null on-state resistance. Particularly, in majority carrier devices, the specific on-resistance ($R_{ON,sp}$ = R_{ON} x Area) can be defined as:

$$R_{ON,sp} = \frac{W_{drift}}{q \times n \times \mu_n} \tag{1.3}$$

Where W_{drift} is the drift region's width, n is the carrier density and μ_n is the electron mobility.

The drift region width is directly proportional to the breakdown voltage according to the relation:

$$V_{BR} = \frac{1}{2} W_{drift} \times E_{crit} \tag{1.4}$$

On the other hand, the Poisson's equation can be used for defining the number of electrons between the two terminals:

$$q \times n = \varepsilon_0 \times \varepsilon_r \times \frac{E_{crit}}{W_{drift}} \tag{1.5}$$

By combining equations (1.3), (1.4) and (1.5), we can obtain a relationship linking the specific on-state resistance and the breakdown voltage as highlighted by equation (1.6):

$$R_{ON,sp} = \frac{4 \times V_{BR}^{\ 2}}{\varepsilon_0 \times \varepsilon_r \times \mu_n \times E_{crit}^{\ 3}} \tag{1.6}$$

This relation put in evidence a clear trade-off between breakdown voltage and $R_{ON,sp}$. Nevertheless, the inverse proportionality between $R_{ON,sp}$ and critical electric field, highlights the potential advantage offered by WBG semiconductor devices.

This can be better understood by looking at Fig. 1.1, in which equation (1.6) is plotted for Si, SiC and GaN technology by considering an ideal device structure.

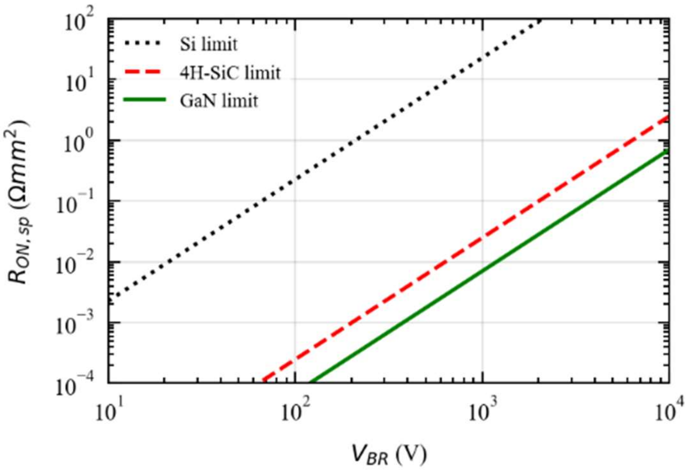

Figure 1.1: Theoretical $R_{ON,sp}$ vs V_{BR} limit for Si, SiC and GaN.

By looking at Fig. 1.1, it can be clearly seen that the theoretical limits for WBGs like SiC and GaN are well beyond the Silicon one. Particularly, Gallium Nitride is the one presenting the best theoretical limits among the considered technology, since it presents high critical electric field and high electron mobility at the same time. Nevertheless, this is a comparison based on ideal device structures, whereas real transistors may difficultly reach their theoretical limits.

Another important parameter to be considered is the Gate Charge (Q_G). In fact, the gate charge is proportional to the switching losses, since it is directly linked to the speed at which the device may be turned on and off. In fact, the Q_G measures the amount of charge that must be provided or removed to switch on and off the device.

Usually hard-switch circuit with inductive load, is used for gate charge measurement (see Fig. 1.2(a)).

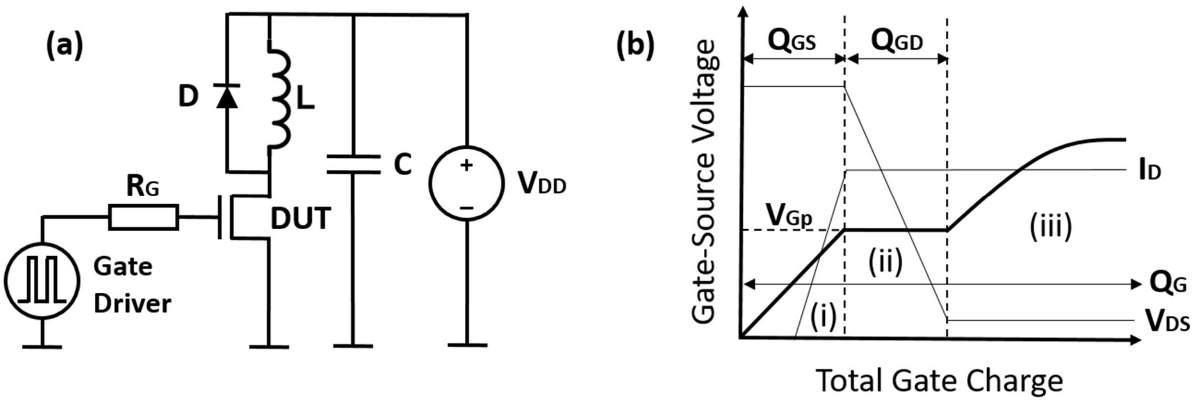

Figure 1.2: (a) Gate-charge measurement setup and (b) example of turn-on gate charge measurement results.

The device under test is switched-on and -off using gate pulses, while the V_{DS} and the drain current I_D are fixed respectively by the voltage power supply and by the inductor. The measurement is performed by applying two consecutive pulses to the device gate. The first one is used to load the inductor and its duration has to be set in order to match the desired current level. Then a second pulse is used to perform the measurement, and switch-on or -off waveforms are acquired. Figure 1.2(b) shows typical result obtained in switch-on gate charge measurement, where gate charge is evaluated by integrating the gate current over switching time. The turn-on transition is broken down into three regions. In region (i) the gate to source voltage rises from 0 V to its plateau voltage (V_{Gp}). When the gate rises from 0 V to its threshold voltage (V_{TH}), the MOSFET is still off with no drain current flows, and drain-source voltage remains clamped to V_{DD}. Once gate voltage reaches V_{TH}, the MOSFET starts conducting and I_D rises. V_{DS} is still clamped until all inductor current is being supplied by the MOSFET, and gate current charges the input capacitance (C_{ISS}) with $V_{DS}=V_{DD}$. Region (ii) is the region where V_{GS} is held at V_{Gp} and the flat plateau can be observed. I_D is fixed by the inductor current and V_{DS} starts to drop. In this region, the gate current is used to charge the reverse transfer capacitance (C_{RSS}), while V_{DS} is decreasing from V_{DD} to I_D x R_{ON}. In the last region, (iii), the MOSFET enters into linear region. V_{GS} rises from V_{Gp} to driver supply voltage, and I_D is still clamped by the inductor current. In this region the gate

driver continues to charge the input capacitance C_{ISS}, but in this case at low V_{DS} voltages. Similarly, the device behaves during the switch-off transient. The gate driver starts to discharge the gate voltage with V_{DS} and I_D clamped, until it reaches the plateau voltage V_{Gp}. At that point C_{RSS} is charged and the drain to source voltage grows until it reaches V_{DD}. Once all the reverse capacitance has been discharge the current drops to zero.

The gate charge and the on-state resistance are in a trade-off relationship. In fact, the total gate charge can be reduced by reducing the surface area of the device, but this will result in a consequent increase in R_{ON}. This compromise can be mitigated by WBG semiconductors, since they present a reduced R_{ON} for the same device area, thus allowing to achieve the same performances of the Silicon counterpart with a significant advantage in terms of switching speed and dynamic losses. The ability to reduce the chip size with WBGs yields another important advantage. In fact, it directly translates in a reduction of the parasitic capacitances of the devices, that helps in increasing their switching speed.

These advantages make WBGs based on SiC and GaN particularly attractive for both RF and power applications. In the following, the main peculiarities of SiC and GaN technologies and related devices are briefly summarized.

1.2 Silicon Carbide (SiC)

1.2.1 Crystalline Structure

Silicon Carbide is a semiconductor consisting of silicon and carbon atoms. One C (or Si) atom is bound to four neighbouring Si (or C) atoms, which are placed in the corners of a tetrahedron. The Si-C bond is very strong due to its short bond length and its sp3 hybridization and it has a nearly covalent character. However, slightly different electronegativity values for C and Si imply a small ionic contribution to the SiC bond [7].

SiC has a layered crystal structure which can occur in a number of different forms [8]. There are three different arrangements of Si and C atoms in a SiC crystal layer, that are named as A, B and C. These arrangements are stacked in a sequence (see Fig. 1.3), giving rise to a large number of possible combinations. The combination of the three possible positions results in hundreds of different theoretically possible sequences. From the different stacking sequences in one direction (c-axis), different crystal modifications, labelled polytypes for SiC [9], are possible. The phenomenon of a material to exist in more than one crystal structure is known as polymorphism and for SiC the polymorphism is restricted to one dimension [10].

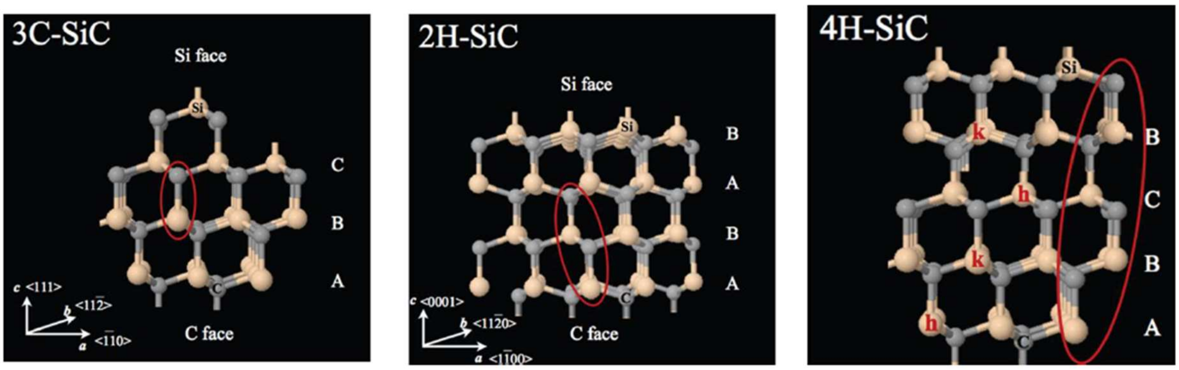

Figure 1.3: Structure of some SiC polytypes. The stacking sequence is displayed at right for all structures. A way of classifying polytypes labels each SiC bilayer according to its hexagonal (h) or cubic (k) character [8].

A common notation of all the polytypes is composed of a number and a letter [7]. The number stands for an amount of double layers in the unit cell and the letter represents structural information; C - cubic, H - hexagonal and R - rhombohedral.

With its zincblende structure, the lattice parameter of 3C-SiC is determined by the edge of the cube. 2HSiC, which is very difficult to synthesize as stand-alone crystals [11], has a wurtzite structure and all lattice sites have a pure hexagonal environment, labelled h. All the other polytypes have both lattice sites with a quasi-cubic environment and lattice sites with a local hexagonal environment. In case of a hexagonal structure (4H- and 6H-SiC), the lattice parameter corresponds to the edge of the basal plane.

1.2.2 SiC-based power MOSFETs

SiC Power MOSFET commercially available can present two main types of structure: (i) planar MOSFET structure and (ii) Trench structure [12]. These two structures are schematically depicted in Fig. 1.4. A part form this distinction, the main characteristic of commercial SiC devices is their vertical structure that allows supporting high voltages thanks to the thick low-doped drift layer. This is possible thanks to the availability of native SiC substrate.

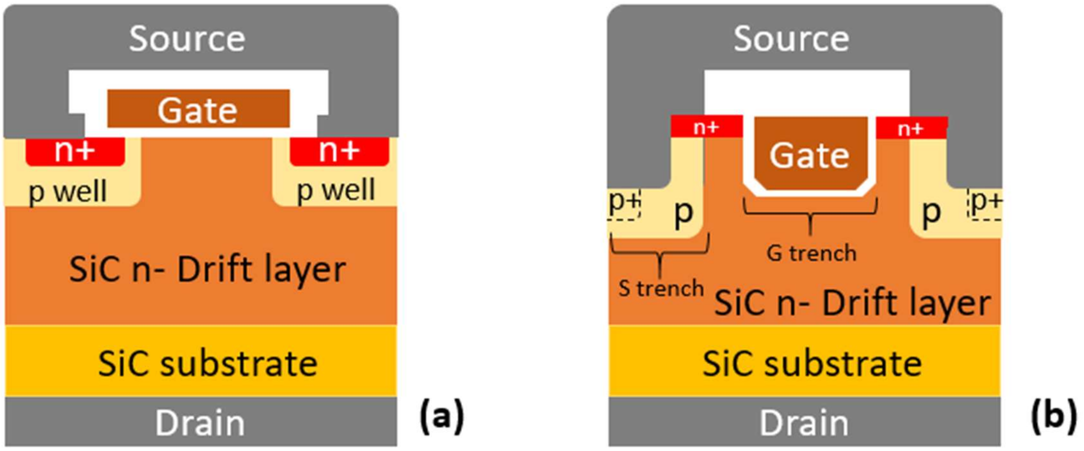

Figure 1.4: Cross sections of typical (a) SiC Planar MOSFET and (b) SiC Trench MOSFET [13]. A double trench is typically adopted in these devices, since the Source (S) trench allows to mitigate the electric field at the Gate (G) trench corner and prevent gate-oxide failure when the device operates at large drain voltages [14].

The cross section of the typical SiC planar MOSFET is depicted in Fig. 1.4(a). Starting from an n+ doped substrate, the n- drift layer is fabricated by epitaxial grown. P-type base (or body) and n+ source regions are then implanted and the channel length is defined by difference in lateral extension of these two regions. The total resistance of this structure is given by the sum of several components. To put these components in evidence, the half-cell is shown in Fig. 1.5.

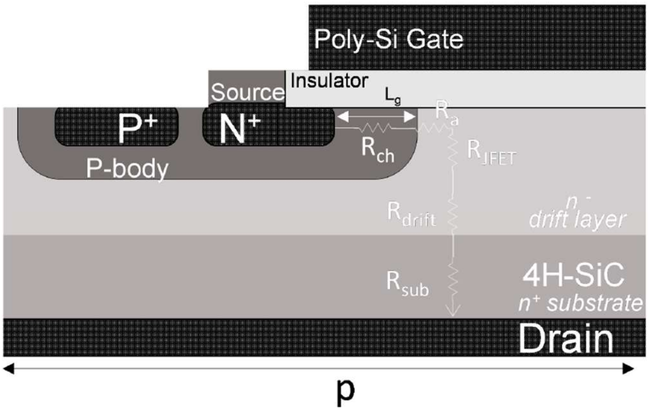

Figure 1.5: Cross sections of the SiC Planar MOSFET half-cell with the different components constituting the total on-state resistance [15].

R_{CH} is the resistance due to electron flowing in the channel, function of channel length and applied gate voltage. In SiC MOSFET this resistance is also affected by semiconductor/oxide interface roughness and defects. Electrons injected from the channel in the drift region spread in the JFET region. Two resistances are associated to this portion of the device: R_{JFET} that is dependent from n- doping concentration and body/drift depletion width and R_A that is given by the presence of an accumulation layer below the gate oxide, which is formed by the positive applied gate voltage. Then, electrons flowing in the epitaxial layer encounter resistance R_{DRIFT} of the low-doped drift region. Its value depends on the device blocking capability and strongly limits maximum rated voltage. In SiC MOSFETs, the drift layer doping concentration is much higher and its dimension lower compared to Silicon devices, thus it results in a reasonable value for R_{DRIFT} even when reaching high breakdown voltage. Finally, resistances of the heavily doped source and substrate regions, as well as contact resistances, can be neglected for high voltage devices.

While most of the components can be minimized by properly scaling the device layout, the channel component (R_{CH}) is more critical. The introduction of the Trench structure shown in Fig. 1.4(b) allows to reduce the total R_{ON} of SiC devices, thanks to a reduced channel resistance [12], that is due to an increased carrier's mobility [14]. In fact, R_{CH} can be expressed as [16]:

$$R_{CH} = \frac{L_{CH}}{W_G \times \mu \times C_{OX} \times \left(V_{GS} - V_{TH}\right)} \tag{1.7}$$

In which L_{CH} is channel length, p is the pitch of the MOSFET half-cell, μ is the channel mobility, C_{OX} is the gate oxide capacitance, V_{GS} is the applied gate-source voltage and V_{TH} is the device's threshold voltage. According to this formula, the channel resistance can be reduced, in principle, by decreasing the channel length. Nevertheless, a L_{CH} reduction could yield short channel effects when the device is biased in off-state, thus yielding undesired behaviours [17].

Accordingly, a reduction in the channel resistance can be obtained by increasing the carrier's mobility and/or the gate oxide capacitance. Both are influenced by the adopted gate insulator and the most robust gate insulation solution adopted so far for SiC power MOSFETs is Silicon Oxide (SiO_2). Accordingly, the behavior of the SiC power MOSFETs depends critically on the properties of the SiO_2/SiC MOS system. In particular, two critical regions can be identified. The first one is the SiO_2/SiC interface, which is characterized by the presence of a distribution of interface states (Dit), close either to the valence or conduction band edge [18, 19]. Then, a second region inside the gate insulator is characterized by the presence of slow near interface oxide traps (NIOTs) and bulk traps [20, 21]. The presence of these traps impact both the carrier's mobility and the device's V_{TH}, thus limiting the stability and performances of SiC power MOSFETs.

1.3 Gallium Nitride (GaN)

1.3.1 Crystalline Structure

Gallium Nitride is a III-V binary compound whose molecula is formed by a Gallium atom (III Group) and Nitrogen atom (V group). The crystalline structure can be either wurtzite or zincblende. The latter is rare because, being metastable, it tends to pass to the more stable wurtzite form. The elementary cell in the wurtzite form is hexagonal in symmetry where every Nitrogen atom is bound by four Gallium atoms arranged according to the vertices of a tetrahedron. This structure can be seen as the interpenetration of two hexagonal lattices, each consisting of two distinct elements. Thus, a hexagonal cell like the one in Fig. 1.6 is obtained, where we can distinguish plans formed by the same element.

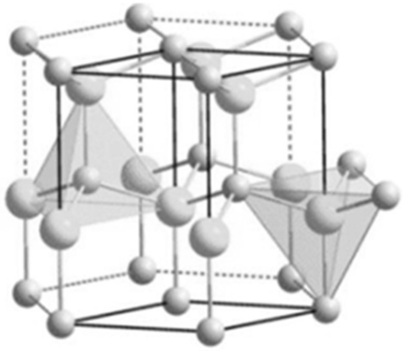

Figure 1.6: Wurtzite GaN crystalline structure [22].

One of the most important properties for wurtzite III-Nitrides group, like GaN, is that these materials exhibit an internal field caused by the spontaneous polarization [23]. Moreover, GaN is characterized by high piezoelectric constants, so that we can find also a piezoelectric polarization effect, that, together with the spontaneous one, is fundamental for GaN devices in order to let them work correctly. In fact, when GaN is put in contact with a material that shows a different lattice constant, the piezoelectric polarization effect appears: in this way the forces at the interface between the two materials, caused by the lattice mismatch, are transformed into piezoelectric polarization, that, depending on the type of strain (compressive or tensile), can be directed in one direction or in the opposite one. In heterostructure such as AlGaN/GaN for example, Aluminum Gallium Nitride (AlGaN) layer is subject to tensile stress. In case of tensile strain, the vectors of spontaneous and piezoelectric polarization are parallel and have the same direction, whereas they are opposed in case of compressive strain. These two types of polarization give birth to a quantum well on the low edge of the conduction band. The different magnitude of the polarization vector in the two materials leads to a high negative charge concentration at the interface; the difference of band gap between the two materials makes these electrons to be confined in GaN. In this way, the 2-Dimensional Electron Gas (2DEG) channel is created without doping and without applying positive voltage.

1.3.2 AlGaN/GaN HEMTs

As already mentioned, the AlGaN/GaN Heterostructure allows the formation of a 2DEG channel at the in the interface between the two material. The fact that no-doping is required to achieve this conditions is particularly important, since it allows high mobility levels in the semiconductor device. For this reason, the devices formed in this way are the so called High-Electron Mobility Transistors. The spontaneus formation of a conduction channel, without the application of any biasing voltage, gives rise to depletion-mode transistors.

The typical Band-Diagram of the AlGaN/GaN Heterostructure is reported in Fig. 1.7.

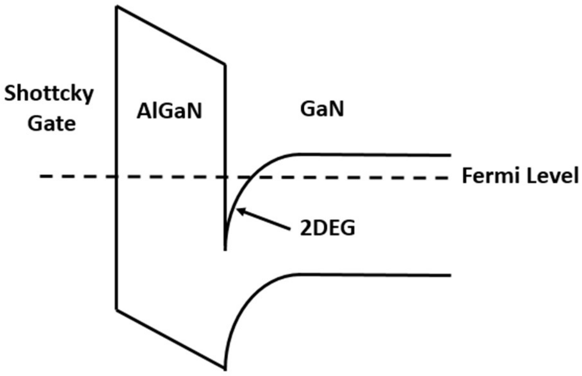

Figure 1.7: Band Diagram of the AlGaN/GaN HEMT structure (V_G=0 V).

As can be seen from Fig. 1.6, at $V_G = 0V$ (i.e., without bias on the gate terminal) the conduction band (E_C) in the GaN channel layer is below the Fermi level, thus giving rise to strong confinement for electrons. This confinement creates a so-called "quantum-well" that is generally few nanometres thick and is conventionally approximated as a two-dimensional layer in which electrons are able to move with high mobility (due to the absence of impurities in the channel). In this case, the threshold condition for the AlGaN/GaN HEMT is set as the gate voltage necessary to deplete completely the 2DEG below the gate. To do so a negative voltage must be applied at the Shottcky gate contact.

1.3.3 R_{ON} partitioning

The spontaneous formation of a 2DEG at the AlGaN/GaN interface allows to measure the 2DEG sheet resistance (R_{2DEG}) and the contact resistance (R_C) of the HEMT structure by means of simple structures employing Transmission Line Measurement (TLM) method. In fact, the resistance of normally-on GaN-based HEMTs can be divided in several components as schematically depicted in Fig. 1.8.

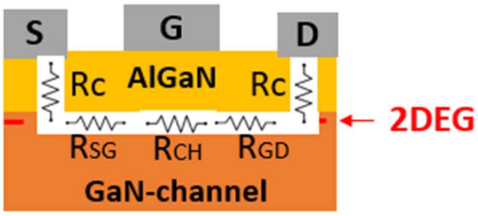

Figure 1.8: Basic components constituting the on-state resistance of normally-on AlGaN/GaN HEMTs.

According to this picture, the total R_{ON} of a normally-on AlGaN/GaN HEMT can be partitioned by following the formula:

$$R_{ON} = 2 \times R_C + R_{SG} + R_{GD} + R_{CH} \tag{1.8}$$

The Source and Drain Ohmic contacts are typically made by Ti/Al based metal schemes [24] and provide a non-null resistance (i.e., contact resistance R_C). This resistance can be reduced by recessed Ohmic contacts [25] or by optimization of the surface morphology after etching [26]. The remaining components are located at the AlGaN/GaN interface in the 2DEG region. The channel resistance R_{CH} is located beneath the Shottcky gate ad strictly depends on the Gate length (L_G). The remaining components are the Source-Gate (R_{SG}) resistance and the Gate-Drain resistance (R_{GD}). These are the access-regions resistances and strictly depends on the Source-Gate and Gate-Drain distances. Both can be estimated through the 2DEG sheet resistance (R_{2DEG}). In order to extract R_C and R_{2DEG}, Transmission Line Measurements are employed and the TLM structure shown in Fig. 1.9 is typically used.

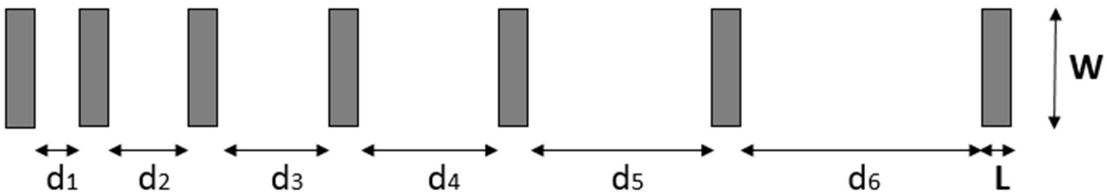

Figure 1.9: Typical TLM structures used for Sheet resistance and contact resistance extraction.

The structure consists on several pads placed at different distances and featuring equal width (W). By applying a constant voltage between two pads and measuring the resulting current, it is possible to extract the total resistance between them.

Since these structures do not present the Shottcky gate terminal, the resistance of this simplified structure (R_{TLM}) can be defined as:

$$R_{TLM} = 2 \times R_C + R_{2DEG} \tag{1.9}$$

From this formula, it is clear that, the 2DEG sheet resistance cannot be directly measured by eliminating the contact resistance, since the resistance of the pads will be always present. Nevertheless, by performing this measurement for all the pads (i.e., for a set of different distances (d_n)) it is possible to reconstruct the typical R-d plot shown in Fig. 1.10, from which both R_C and R_{2DEG} can be derived.

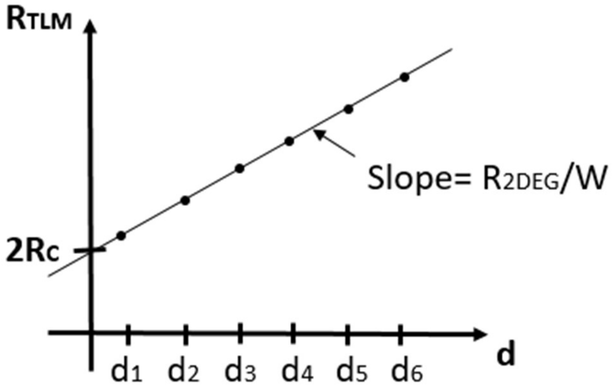

Figure 1.10: R-d plot used for the extraction of the on-state resistance components.

This allows to extract the contact resistance by considering the intercept with the y-axis, since at zero distance between the pads, the 2DEG sheet resistance is expected to be null. On the other hand, the 2DEG resistance can be extracted as the slope of the R-d curve, according to the Ohm's law. This allows to univocally determine R_C, R_{SG} and R_{GD}, whereas R_{CH} can be obtained from the partitioning by measuring the R_{ON} of the real device. These informations are extremely important during technology development, allowing to identify the point of weakness mainly affecting the R_{ON} in the device.

1.3.4 Normally-off devices

Till now, we have considered just the simple AlGaN/GaN heterostructure, which yields normally on-devices (i.e., depletion-mode transistors). However, in power conversion applications, depletion mode devices are inconvenient, while normally-off devices are usually preferred because they simplify the design of the gate driver circuit and improve the safety of the power switching converters in case of control circuitry failure.

In order to obtain normally-off operations for GaN-based HEMTs, several approaches have been adopted: (a) a cascode configuration combining a Si normally off MOSFET and a normally ON GaN HEMT [27-29], (b) the use of a HEMT with fluorine implantation under the gate [30-32], (c) a gate recessed MIS-HEMT (metal–insulator–semiconductor) [33, 34] and (d) a p-GaN-gated HEMT [35]. These different approaches are schematically depicted in Fig. 1.11.

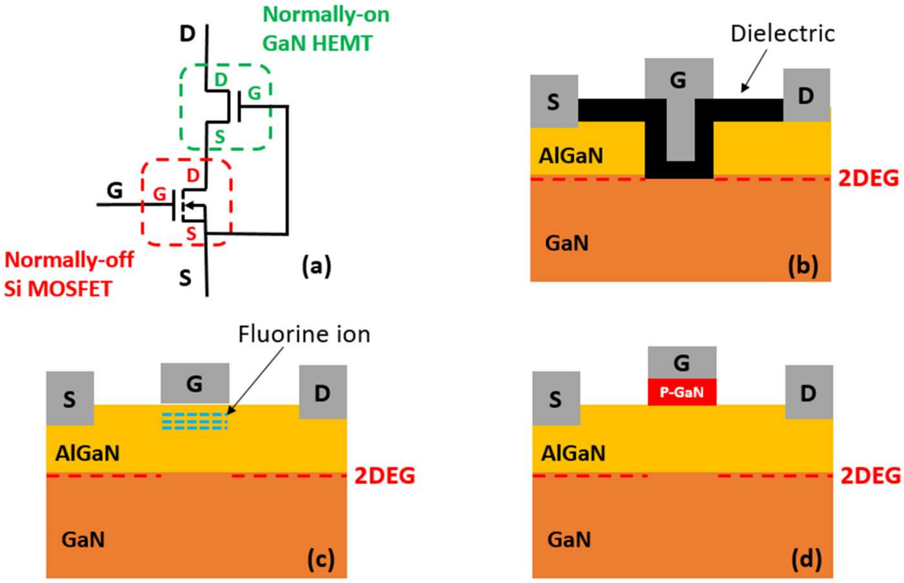

Figure 1.11: Different structures for obtaining normally-off GaN-based HEMTs. (a) Cascode configuration, (b) Recessed-gate GaN HEMT, (c) GaN HEMT with fluorine ions implantation and (d) P-GaN gate GaN HEMT.

(a) The cascode configuration exploits the connection between a high-voltage normally-on GaN HEMT and a low-voltage Si MOSFET (see Fig. 1.11(a)). The Si MOSFET controls the ON and OFF-state switching of the GaN HEMT. When the voltage applied to the cascaded device is higher than the threshold voltage of the Si MOSFET, the device is turned on, since the gate voltage of the GaN HEMT is close to zero. As the two devices are connected in series, the GaN HEMT and the Si MOSFET share the same current. Accordingly, when no gate voltage is applied to the MOSFET (i.e., the MOSFET is turned-off), no current can flow through the channel of the HEMT. Thus, the cascode configuration allows to take advantage of the positive threshold voltage of the MOSFET as well as the low ON-resistance of the 2DEG, together with the high breakdown field of the GaN HEMT in OFF-state conditions. However, the presence of the Si MOSFET limits the operation at high temperature. Moreover, the packaging complexity, parasitic inductances and size are increased, significantly impacting the switching performance of the device.

(b) Another approach consists in the so-called recessed-gate solution. In this case, the AlGaN barrier layer is fully etched under the gate area (Fig. 1.11(b)) and a dielectric insulating layer is deposited in the formed hole. This allows to have no channel under the gate contact at zero voltage and the presence of a thick gate dielectric enables a large maximum gate bias for the device turn-on. The deposited dielectric directly impacts V_{TH} stability [36] and the 2DEG mobility [37], making this solution difficult to be optimized.

(c) Another option exploits fluorine ions implanted into the AlGaN layer self-aligned to the gate (Fig. 1.11(c)) [38, 39]. The introduction of negative ions in the AlGaN depletes the 2DEG by changing the surface potential. However, the V_{TH} stability and R_{ON} degradation may be severely impacted by this approach, making it not practicable for manufacturers.

(d) At present, the most attractive method to obtain normally off GaN transistors is the use of a p-doped GaN layer under the gate area (Fig. 1.11(d)) [40]. The presence of the p-GaN layer moves the band diagram to higher energies, so that the 2DEG results depleted under the gate contact even for V_{GS}=0V. In order to achieve an efficient depletion of the 2DEG and $V_{TH} > 0$ the properties of the AlGaN/GaN heterostructure (i.e., thickness of the AlGaN barrier and Al-concentration) must be appropriately defined [35, 41]. Moreover, a high doping level of the p-GaN layer ($> 10^{18}$ cm^{-3}) is typically required for an efficient depletion of the region at the metal-gate/p-GaN interface [42]. In this sense, one of the key elements to improve the threshold voltage V_{TH} for a fixed Mg-concentration of the p-GaN layer is to increase the Mg electrical activation. This latter can be done by appropriate p-GaN layer growth parameters and annealing conditions [43]. The metal/p-GaN conductivity depends on the properties of the materials formed at the metal/semiconductor interface during deposition and annealing. Depending on the choice of the metal, on the doping of p-GaN and on the process parameters, the metal/p-GaN contact can have a higher (referred to as Ohmic) or lower (Schottky) leakage current. In order to keep under control the gate leakage and increase the operative range for the gate bias, low leakage (i.e., Schottky) junctions are preferable, but this affects the stability of the device threshold voltage during operation, due to the presence of a floating p-GaN region. In fact, the metal/p-GaN interface in correspondence to the gate contact, yields a reverse biased Schottky diode when a positive gate bias is applied to the device, whereas the presence of a p-GaN layer above the AlGaN barrier and the electron channel (2DEG) in the GaN layer creates a p–i–n diode (see Figure 1.12). The presence of two back-to-back diodes, makes floating the p-GaN layer, being source for possible instabilities due to charge accumulation in this region.

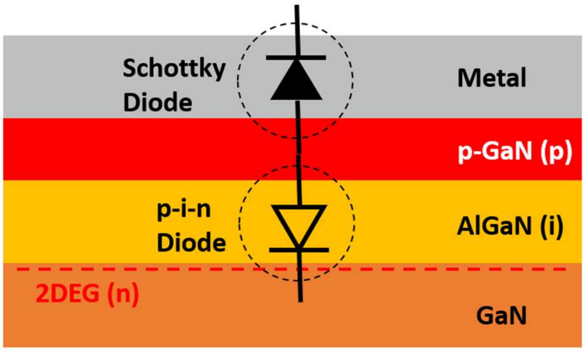

Figure 1.12: Schematic representation of the Metal/p-GaN interface forming a Schottky diode and the p-GaN/AlGaN/GaN stack forming a p-i-n diode. The back-to-back connection of the two diodes yields a floating p-GaN layer.

In this thesis, we investigated AlGaN/GaN HEMTs used for both power and RF applications. For the latter, we tested Shottcky gate devices featuring a normally-on behaviour, whereas for power devices we tested p-GaN gate HEMTs to have normally-off operation.

1.3.5 Epitaxial Structure

A part from the different gate stacks that can be adopted for GaN-based HEMTs, another key aspect governing the behavior of these devices is their epitaxial structure. This starts with a Si or SiC substrate [3]. In fact, Homoepitaxial growth of GaN based films, from a practical point of view, is not economically possible due to the very limited availability of GaN substrates in standard semiconductor wafer size. Accordingly, the two choices typically made nowadays refers to GaN-on-Silicon and GaN-on-SiC. One of the criteria that will lead the comparison among these two possibilities is the cost. In fact, Silicon Carbide is very mature, but limited in terms of wafer sizes, with wafer diameters in the order of 100-150 mm (4-6 inches), while Silicon already presents 300 mm (12 inches) wafer diameters from many suppliers in a very competitive market place. For this reason the cost per die is relatively lower with Silicon substrate, making GaN-on-Silicon the typical choice for price-sensitive power electronics applications. On the other hand, the GaN-on-SiC approach combines the high-power density capabilities of GaN with the superior thermal conductivity and low RF losses of SiC, that makes this solution the most performing one in the RF field. For this reason, SiC is still considered the best solution for microwave applications, even if Silicon is gaining appeal for its ability to address large scale production. Also in the RF market, the emerging 5G and beyond technologies requires investments on GaN-on-Silicon for the development of devices presenting sustainable costs, and since Si is fast improving its capabilities, it will probably win the contest in the near future.

On top of the chosen substrate, an AlN nucleation layer is typically grown, that aims at reducing strain and dislocations to the above active layers. In addition, it isolates the active device from the substrate thus reducing vertical leakage. Above the Nucleation layer stands the GaN Buffer (which can be separated from the Nucleation layer by several layers, called Transition Layers, again used to reduce strain and growth imperfections) above which the GaN channel layers is grown. The 2DEG forms in this layer at the interface with the AlGaN barrier layer. The basic device structure is then completed by the passivation layer (typically Silicon Nitride (SiNx)) that is then selectively etched to deposit the metal contacts. Each one of the aforementioned layers has a key importance on the epitaxial structure. The GaN Buffer must guarantee insulating property to the device in order to make it operating. One important option that is commonly employed to guarantee vertical insulation is the adoption of a Super-Lattice (SL) that is followed by a semi-insulating GaN Buffer layer in order to allow a good lattice math and stable growth for the actual GaN channel. Particularly, due to the n-type conductivity of GaN, the GaN Buffer is typically doped with acceptors (Carbon or Iron [44]) in order to make it semi-insulating. Nevertheless, the introduction of these impurities in the GaN Band-Gap yields the formation of trap states that could significantly impact the device's stability.

1.4 Traps

Dopants and impurities introduced both intentionally and un-intentionally in the material, induce trap states in the bandgap that can significantly affect the device's behaviour. Traps are basically defects in the crystalline structure that creates an energy level where charge carriers (electrons or holes) can be temporarily or permanently captured, i.e., trapped. In general, the trap occupancy is regulated by the Fermi-Dirac-statistics [45] via the quasi-Fermi levels for electrons and holes, E_{fn} and E_{fp}, respectively. If the energy level of an electron trap, E_{tn}, lies between E_{fn} and the conduction band edge, E_C, ($E_{fn} < E_{tn} < E_C$) the probability for trapping and thus its occupancy is low and the trap is mostly empty and thus positively charged. Such traps are called "shallow". In contrast, if E_{tn} is smaller than E_{fn} ($E_{tn} < E_{fn}$) the trapping probability and thus the occupancy is high. Such traps are called "deep" and they are mostly neutral. As this behavior, the occupancy with an electron and the charge state is very similar to that of a donor, such traps may be called "donor-like." Actually, the occupation probability for the electron trap is the same as that for the non-ionization of donors. Similarly, hole trapping centers may be called "acceptor-like" for the same reasons [46]. In this case, the energy level of an electron trap, E_{tp}, lies between E_{fp} and the valence band edge, E_V, ($E_V < E_{tp} < E_{fp}$) the probability for trapping and thus its occupancy is low and the trap is mostly empty and thus negatively charged. Such traps are called "shallow". In contrast, if E_{tp} is larger than E_{fp} ($E_{tp} > E_{fp}$) the trapping probability and thus the occupancy is high. Such traps are called "deep" and they are mostly neutral. A simplified representation of the possible traps configurations that can be encountered in the semiconductor's bandgap is reported in Fig. 1.13.

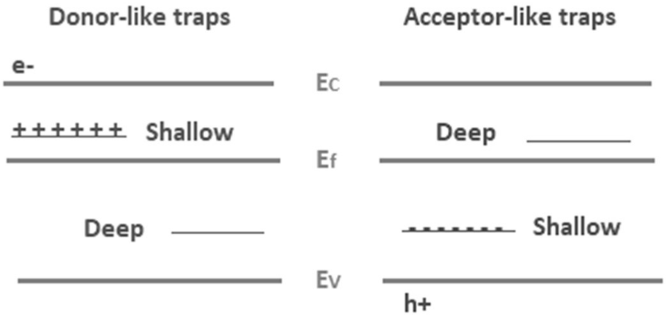

Figure 1.13: Schematic representation of donor-like and acceptor-like traps.

This distinction between donor-like and acceptor-like traps, along with the difference between Deep and Shallow levels is fundamental for defining the physical properties of the trap state considered. As a relevant example, the shape of the potential barrier describing the trap state, strongly depends on the trap's nature. With this in mind, we can distinguish trap states in two main categories: Coulombic and non-Coulombic traps. In general, Coulombic traps are charged when empty and neutral when they capture a carrier from the valence or the conduction band. On the other hand, non-Coulombic centers are trap states that are neutral when empty and becomes charged when capturing an electron/hole from the conduction/valence band [46].

1.5 Trapping Effects

As already mentioned, trapping effects are still a major cause of parameters degradation in both SiC MOSFETs and GaN-based HEMTs and do not allow to exploit all the theoretical advantages offered by these technologies. Particularly, several trapping effects can be encountered during devices operation as a consequence of capture/emission processes from traps. Among these effects, we report those that are discussed in this dissertation.

1.5.1 V_{TH} instability

Threshold voltage instabilities are typically analyzed by applying either negative gate bias (NGB) or positive gate bias (PGB) stress voltages with zero drain–source voltage, with the aim of isolating V_{TH} effects induced by the gate voltage biasing from the drain induced ones. For normally-on devices that required negative gate voltages to be turned-off, instabilities related to NGB is a critical aspect, while in normally-off devices, V_{TH} stability under PGB is of major concern. Nevertheless, assessing the stability of the device's V_{TH} under NGB conditions could be important even in case of normally-off devices, since a negative gate voltage can be applied to switch off the transistor, in order to prevent false turn-on and ensure safe operation against voltage spikes on the gate [47]. Moreover, NGB measurements can somehow emulate OFF-state operation, since similar large values of drain–gate voltage can be achieved with both biasing conditions. Another behaviour that can be encountered on both SiC and GaN devices is V_{TH} hysteresis. This effect can be measured by means of consequent I_D-V_{GS} curve acquisitions, separated by a short recovery time. The sweep of the gate voltage during the first acquisition can give rise to trapping effects under the gate terminal that are responsible for drifts in the device's V_{TH}. These drifts can be either negative or positive and yields a shift in the I_D-V_{GS} captured during the second acquisition. Generally speaking, V_{TH} instabilities, of both signs, can seriously affect the device operation. A negative V_{TH} drift could change the device behaviour from normally-off to normally-on, thus being a serious concern for reliability. On the other hand, positive shifts in V_{TH} could result into a reduced overdrive voltage (see Fig. 1.13(a)), thus reducing the device's current for a given driving V_{GS}. This could seriously impact also the on-state resistance as discussed in Section 1.2.2 for SiC MOSFETs.

1.5.2 Dynamic-R_{ON} increase

One of the most detrimental effects observed in power transistors employed in switching converters is the dynamic increase of the on-state resistance with respect to its DC value (see Fig. 1.14(b)), yielding an undesired increase in the conduction losses. Possible underlying mechanisms include electron trapping and/or hole emission from trap states in the gate-drain access region, taking place during the off-state phase of the switch-mode operation or during hard-switching transitions in which devices are subjected to both high voltage and current levels simultaneously. The conductivity of the device is reduced due the build-up of a negative charge that partially depletes the channel and cannot be promptly recovered as the device is switched back to its on-state condition due to the slow recovery dynamics of traps. The reduced conductivity gives rise to the increase in the R_{ON} that dynamically evolves over time during switching operations depending on the applied voltage and temperature.

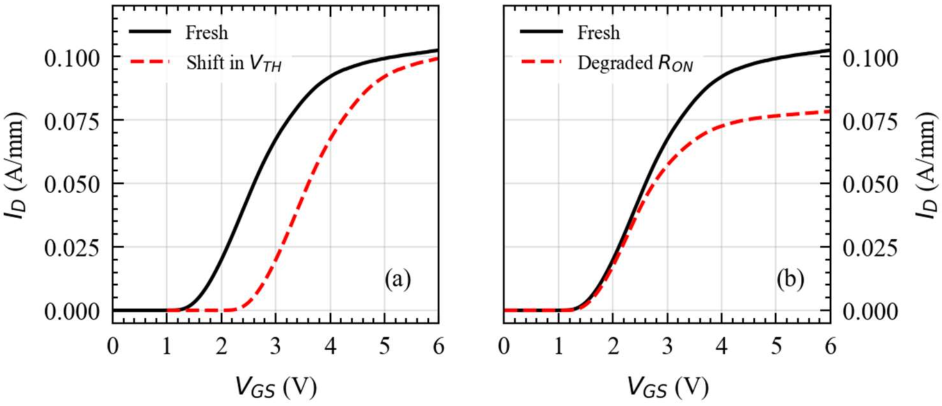

Figure 1.14: Example (a) positive V_{TH} drift and (b) increased R_{ON}. A positive shift in V_{TH} yields a reduction in the overdrive voltage for a given V_{GS}, while an increased R_{ON} results in a reduced triode current.

1.5.3 RF Current Collapse

Considering RF applications, the most harmful trap-related effect is the so-called RF current collapse resulting in a reduction in the maximum drain current and simultaneous increase in the minimum drain–source voltage explorable by the operating point during the RF sweep (see Fig. 1.15). The increase in the minimum drain–source voltage is also referred to as knee-voltage walkout. The overall result is a compression in the RF output power and a degradation of the power-added efficiency compared to the theoretical limits achievable by the given transistor that can be calculated from the DC output characteristics. Responsible mechanisms are related to electron trapping taking place under OFF-state or SEMI-ON bias. Channel conductivity is weakened by this and cannot promptly be restored as the dynamic operating point moves to the ON-state. Either V_{TH} or the drain access resistance or both parameters can, in principle, be increased, depending on whether electron trapping takes place under the gate, in the gate–drain access region, or both.

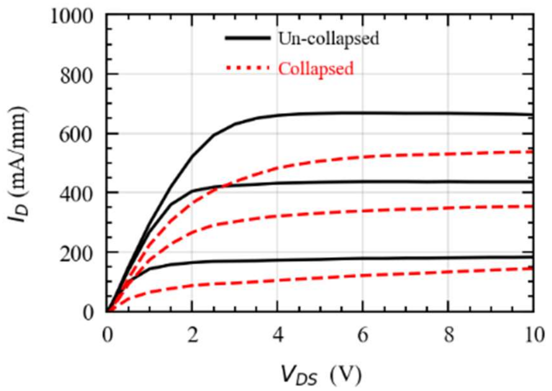

Figure 1.15: Example of un-collapsed (solid-black) and collapsed (dashed-red) output characteristics as a result of charge trapping phenomena.

1.5.4 Time-dependent Breakdown Voltage

Another important parameter to be considered is the breakdown voltage. Generally speaking, the breakdown phenomenon has to be taken into account very carefully, since it limits the maximum bias that a device can sustain, with a consequent limit on the output power and/or operative voltage of power converters. Concerning GaN-Based devices, depending on the type of breakdown occurring within the HEMT structure, the breakdown level obtained can be very different. There can be several physical mechanisms responsible for breakdown in GaN- based HEMTs [48, 49]. As a relevant example, Fig. 1.16 shows the source-drain breakdown mechanism, in which the off-state source leakage can be induced by short-channel effects and/or punch through of electrons from source to drain region as a consequence of a channel not optimally depleted [48].

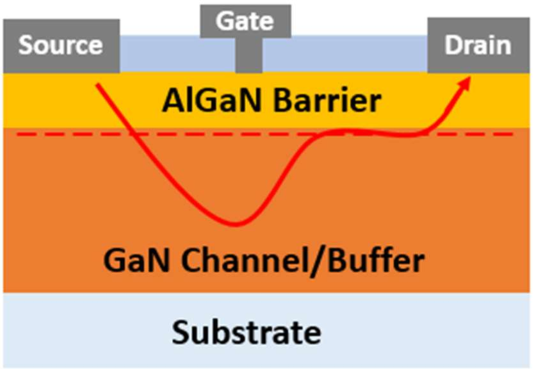

Figure 1.16: Source-Drain Breakdown mechanism in AlGaN/GaN HEMT.

The source induced leakage dominates the breakdown current for gate voltages close to the pinch off voltage, in a device operating in off state. This current leakage depends strongly on the voltage applied to the gate terminal during the IV measurement [50]. In particular, with a deep negative gate voltage, it is possible to suppress the drain-source component, just by improving the buffer depletion. These effects are very remarkable on short-channel devices, and are usually referred to a poor depletion of the under-gate region, resulting in a flow of current within the GaN bulk. At high drain potentials, the current flows in a loop deep in the GaN, far from the AlGaN/GaN interface. Thus, with high drain voltage it is possible to overcome the confining potential needed for GaN HEMT operation. This mechanism is typically called Drain Induced Barrier Lowering (DIBL) [51] or punch-through, and it can be partially avoided by changing the Buffer doping density [44]. So, the dominant leakage path, and consequently the breakdown level, is determined by the bias condition and, more importantly, by the basic properties of the device such as the GaN buffer. Particularly, the presence of traps whose occupation is time dependent, may be responsible for the so called time-dependent breakdown [52], since a different traps' occupancy can modify the Buffer conductivity and the electric field profile inside the structure, with a consequent impact on the voltage level required for triggering the breakdown condition. An example of this phenomenon will be addressed in Chapter 5, in which the time dependent occupancy of Iron traps in the buffer yields different breakdown voltages on AlGaN/GaN HEMTs for RF applications [52].

1.6 Wide-Bandgap Devices Characterization

Despite the large advantages offered by WBGs, the performances of the devices based on these technologies still suffer from parameters degradations and drifts that limits well below expectations their performances and reliability [53]. The main reason causing these degradations is always one: charge trapping/de-trapping. Accordingly, it is extremely important to characterize charge trapping/de-trapping in power devices based on WBGs, in order to gain insights in the physical mechanisms responsible for said degradation and provide useful feedbacks for improving device manufacturing, with the aim to exploit the complete potential of these technologies. In the following, we report some of the main characterization techniques employed for this scope, focusing on those that will be employed for the studies made in this dissertation.

1.6.1 Pulsed I-V

Trap characterization can be carried out by means of several techniques. The most important measurement adopted to quickly identify the presence of trapping phenomena is pulsed I–V (PIV) characterization. The basic idea behind this type of measurement is rather simple. The device is kept for a certain time interval into a quiescent bias point (i.e., baseline), with its source terminal grounded. This quiescent bias should be long enough to induce the complete filling of traps (i.e., longer than the trap's filling time constant). Synchronous and short voltage pulses, typically in the 100 ns–10 µs range with a duty-cycle in the 0.1%–1% range, are applied to the gate and drain terminals to evaluate the device I–V characteristics. The key point is that trap states present slow dynamics and are not able to restore their equilibrium condition if pulses of relative short duration are considered. In fact, if the pulses are shorter than the trap's emission time constant, a negligible effect is induced on the status of the trapped charge. Therefore, the measurement yields the I–V characteristics of the device obtained with the traps filled at the condition set by the quiescent bias point. Since trap filling condition depends on the baseline voltage, comparing pulsed I–V obtained at different quiescent bias points quickly allows us to evaluate the presence and in some way the amount of trapping phenomena. A typical set of pulsed I–V is performed by comparing at least three or more different quiescent bias points: (i) the $V_{GS} = 0$ V, $V_{DS} = 0$ V, which is fundamental to set the reference of the "fresh" device conditions; (ii) gate-lag effect is then evaluated with a baseline where V_{GS} is held below the device threshold voltage and $V_{DS} = 0$ V; and (iii) drain-lag effect is finally evaluated by a baseline with the device in OFF-state conditions and large V_{DS}. Obviously, many other combinations can be considered but the three reported are the most used for device characterization. PIV characterization quickly offers an overview on device operation and a qualitative evaluation of the reduced device performance due to trapping phenomena. Some information on trap spatial localization might also be obtained by comparing results from different trapping conditions. If the device experiences a V_{TH} shift, trapping phenomena are likely to be confined within the device buffer layer and/or the barrier or insulator layer under the gate terminal. On the other hand, a decrease in its transconductance might be induced by surface, barrier, or buffer traps.

There are basically two methods to carry out pulsed measurements:

The first one is the load-line method, in which a resistive load is connected to the drain of the device (see Fig. 1.17(a)). A constant DC voltage is applied to the drain and the gate voltage is pulsed from the off state (quiescent stress, trapping) conditions to the measurement point. This method is closer to real operating conditions, but does not allow to separate the effect of gate voltage stress (Gate Lag) from that of drain voltage stress (Drain Lag) [54].

In the double-pulse method [55], both gate and drain voltages are pulsed from a quiescent bias point; by calibrating the quiescent and measuring bias points it is possible to observe the entire pulsed I-V characteristics; stress induced by gate and drain voltage can be separated. An example of double pulse setup is shown in Fig. 1.17(b).

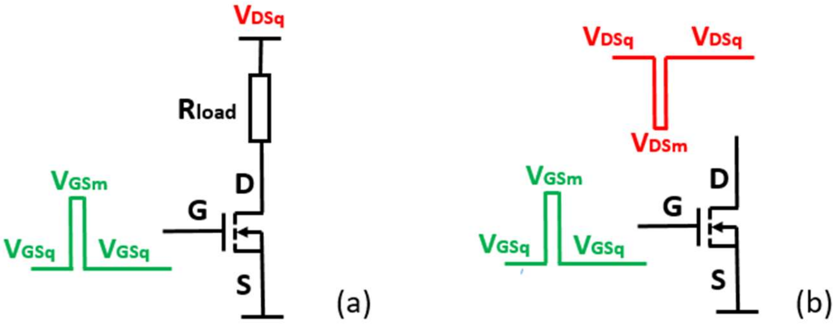

Figure 1.17: (a) Load-line method setup for pulsed I-V characterization. (b) Double-pulse method setup.

1.6.2 Transients Measurements

Capacitance transients are commonly employed to obtain information about an impurity level in the depletion region of a Schottky barrier or a p-n junction. The measurement consists in observing the capacitance transient associated with the return to thermal equilibrium of the occupation of the level, following an initial non equilibrium condition [56, 57]. To allow a faster characterization, still based on this method, Deep-level transient spectroscopy (DLTS) was introduced [58]. In this method, an emission rate window is set, such that the measurement apparatus only responds to transients presenting rates within this range. Thus, if the trap's emission rate is changed by the ambient temperature, the instrument will show a response peak just for the temperature yielding the emission rate in the selected range. However, this technique shows some limits. Impurity levels with a large activation energy result in a low emission rate, leading to transients with large time constants whose evaluation could be masked by slow drifts [59]. A novel methodology named deep-level optical spectroscopy (DLOS) was thus introduces to overcome this limitation [60]. Due to its wide bandgap, the characterization of the GaN material was typically carried out by combining both DLTS and DLOS measurements. The combination of the two measurement techniques allows a full investigation of the trap level within the whole bandgap. In fact, DLTS is adopted for evaluating levels with relatively low activation energies (i.e., < 1 eV), DLOS is employed to characterize deeper levels.

In order to have a well measurable capacitance value, DLTS and DLOS techniques are typically applied to large-area diodes. Conversely these methods are less effective for testing three-terminal devices presenting low capacitances. Moreover, the electric field distribution in actual transistors can be significantly different from that in large-area diodes. Consequently, we can state that DLTS and DLOS can provide useful information on crystal impurities, but they might not be able to provide a clear indication on the effects of said impurities on actual device dynamic operation. In DLTS and DLOS the trapping/de-trapping is evaluated by capacitance transients induced by depletion region variations linked to the emission of trapped charge. On an actual device, the effect of charge emission can be monitored by evaluating the drain current evolution as the emission process takes place. In fact, an emission of trapped electrons will lead to a decrease in the fixed negative charge within the device, leading to an increase in its channel carriers concentration, and, therefore, an increase in its drain current. Drain current transients (DCTs) are typically evaluated by monitoring the device current in the ON-state, after applying for a certain time a different bias condition typically in OFF-state condition (corresponding to the application of a V_{GS} below device V_{TH} and large V_{DS}). In this case, traps' characterization based on device current variations can be performed by means of drain current DLTS (I_D-DLTS), constant drain current DLTS/DLOS (CI_D-DLTS/DLOS), or multiple DCTs measurements carried out at different temperatures.

These measurements are based on the trap's transient behavior. In fact, an increase in the trapped charge in the device causes a decrease in the 2DEG density, thus yielding a reduced conductivity in on-state. This change in conductivity can evolve dynamically since the traps occupancy is time dependent as described by the Shockley-Read-Hall (SRH) theory. In fact, the emission time constant for a trap can be defined as:

$$\tau_e = \frac{e^{\frac{E_A}{kT}}}{T^2 \sigma_n \gamma_n} \tag{1.10}$$

where γ_n is the product of the effective density of states in conduction band (N_C) and the electron thermal velocity, σ_n is the capture cross sections, T is the temperature and E_A is the trap's activation energy. During an emission process the density of trapped charge varies according to:

$$n_t(t) = n_0 e^{\frac{-t}{\tau_e}} \tag{1.11}$$

where n_0 is the initial amount of trapped charge. Since the trapped charge density varies with the time also the carrier density into the 2DEG will become time dependent according to (1.12):

$$n_s(t) = \sigma_p - n_0 e^{\frac{-t}{\tau_e}} \tag{1.12}$$

Where n_s is the carrier density of the 2DEG and σ_P is the polarization charge. Accordingly, the device current, that is directly proportional to n_s, will become time dependent, too:

$$I_D(t) = I_\infty - I_T e^{\frac{-t}{\tau_e}} \tag{1.13}$$

The last equation explains the emission signature observer in current-DLTS for a single trap.

I_D-DLTS [61] is typically performed by applying a constant V_{DS} voltage to have a readable drain current. The gate terminal is periodically pulsed between a filling condition and a sensing condition. The sensing condition is typically slightly above device threshold voltage, with the aim of obtaining a readable current level while at the same time reducing device self-heating effects. Monitoring the current transient over a certain temperature range allows us to obtain a plot of the DLTS signal vs temperature. The detection of peaks in DLTS spectra corresponds to the presence of a trap level, whose activation energy can be extracted by means of an Arrhenius plot [62].

The CI_D-DLTS/DLOS [63] technique is based on a dynamic control of either the device gate or drain voltages with the aim of maintaining a fixed drain current in response to a thermally and optically stimulated trap emission. For a gate-controlled method, a constant and large enough V_{DS} is applied to the device to have it working in its saturation region. The gate terminal is pulsed to the ON-state to induce trap filling and then lowered near pinch-off conditions. The dynamic control on V_{GS} for maintaining a constant I_D will thus give rise to a V_{GS} transient, which will thus be recorded. This condition is sensitive for trap levels located beneath the gate contact and affecting device V_{TH}. For a drain-controlled method, the device is biased in its linear region with low V_{DS} and a V_{GS} large enough to have a negligible forward transconductance g_m. Filling condition here is obtained by biasing the device in pinch-off conditions with large V_{DS}. The subsequent change in device resistance $\Delta R_D = \Delta V_{DS}/I_D$ is then recorded. This condition is particularly sensitive to traps located in the device access regions. The detection of peaks in either the temperature or optical spectra corresponds to the presence of a trap level, whose activation energy can be extracted by means of an Arrhenius plot.

Multiple DCT measurements provide an important advantage in reducing the number of measurements to be carried out, since DCTs are typically evaluated at some temperature levels. On the one hand, this technique is rather simple and can be easily applied to actual transistors. Voltage pulse generators or a load-line drain biasing network are required to switch the device between a filling and a sensing condition. Multiple DCTs, however, can yield results that might be strongly dependent from the device bias conditions used, and the method adopted for the analysis of DCTs required for Arrhenius plot extraction. Additional comments on bias conditions and the DCT analysis will be provided in Chapter 5. DCTs can be recorded with a sensing condition lying in the linear or in the saturation region. Significantly different results might be obtained when comparing results obtained in the linear and saturation region. Nevertheless, an accurate evaluation of the different DCTs response might be useful for spatially localize traps [64]: a sensing condition in the linear region of the device with reasonably high V_{GS} should highlight the effect of traps located within the device access regions. On the other hand, sensing in saturation near the pinch-off voltage, i.e., at low current level so that the effect of device access region can be minimized, should be more sensitive to the effect of traps located beneath the gate contact. The extraction of time constants at different temperatures is the process leading to the construction of the Arrhenius plot from which the trap activation energy is obtained. Several techniques can be used to this aim. A multi-exponential approach can be adopted by least-square fitting the experimental data with the sum of several exponential functions, typically in the amount of few hundreds, with different amplitudes and time constants as described in the following equation:

$$I_{fit} = \sum_{i=1}^{n} a_i \exp\left(\frac{-t}{\tau_i}\right) + I_\infty \tag{1.14}$$

By plotting the amplitude coefficients a_i vs the time constants τ_i, the trap associated time constants can be inferred by looking at the peaks of the spectra obtained.

A different approach relies on the so-called stretched multi-exponential fitting. This least-square method fits the experimental data by means of stretched exponential functions, one for each of the low-pass or high-pass transitions observed in DCTs according to the equation:

$$I_{fit} = \sum_{i=1}^{n} a_i \exp\left(\frac{-t}{\tau_i}\right)^{\beta_i} + I_\infty \tag{1.15}$$

Where β is the stretching factor that is equal to 1 in case of a pure exponential process induced by a single-level defect. Then, n corresponds to the number of transitions observed in DCTs (i.e., potential number of charge emission/capture processes). The Arrhenius plot of each of the i^{th} process can be built using the τ_i values obtained at different temperatures. An alternative approach widely used is the analysis of the derivative of the DCT by the logarithm of time. Peaks in the derived spectra are used to locate the characteristic time constants of different traps and used to derive the emission energies.

The second approach is considered to be more accurate [56] and it has more physical meaning, since it potentially refers each exponential fitting function to its correspondent capture/emission process. Moreover, the parameter β takes into account the possible presence of a distribution of defects instead of a single level trap, which a more realistic case.

In fact, a stretched exponential is by definition a sum of multiple exponentials (i.e., multiple defects and/or a defects distribution) as indicated by equation (1.16).

$$a\exp\left(\frac{-t}{\tau_i}\right)^{\beta} = \sum_{i=1}^{k} a_i \exp\left(\frac{-t}{\tau_i}\right) \tag{1.16}$$

An example of acquired DCT and the corresponding time constant extraction is reported in Fig. 1.18.

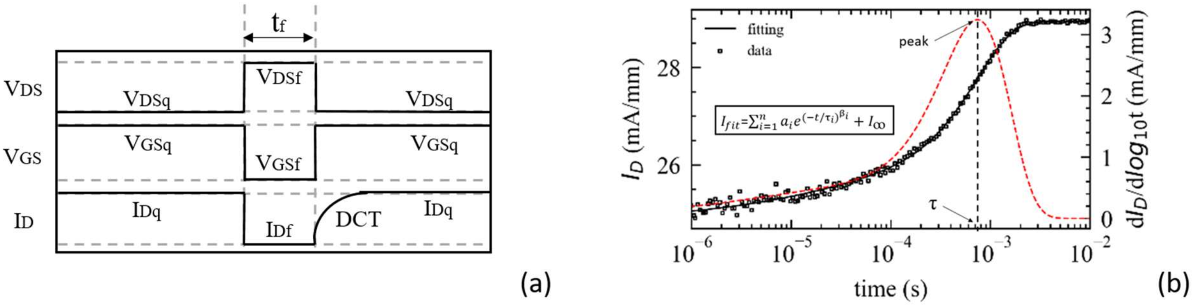

Figure 1.18: (a) Example of typical waveforms employed for the DCTs measurement. (b) DCT and corresponding derivative signal: the emission time constant (τ) is extracted in correspondence to the peak in the $dI_D/dlog_{10}t$ signal.

1.6.3 On-the-fly characterization

The trap characterization methods based on the sensing of device drain current assume that the emission process takes place when the device is biased in the ON-state. Only in this way, it is possible to observe current variations linked to charge emission processes. If said emission process would take place instead in OFF-state conditions, it would be impossible to perform a proper characterization. The analysis of such a trap level can be performed then by means of the so-called on-the-fly characterization [65]. In this case, the device is biased in a condition promoting the charge emission process, and it is periodically turned on to sample within a short time interval the drain current evolution. This allows us to obtain a drain current evolution over time, similarly to the DCT method previously described. The same approach can be used for monitoring other key parameters like the on-state resistance and the threshold voltage, by properly acquiring the drain voltage and the gate voltage corresponding to the current sensed in the short on-state time.

An example of waveforms typically adopted for the on-the-fly characterization under off-state stress conditions is reported in Fig. 1.19.

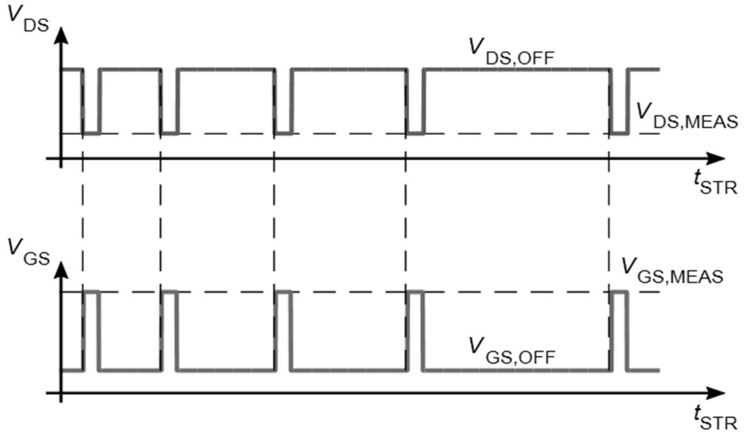

Figure 1.19: Example of the V_{DS} and V_{GS} time sequences applied for the on-the-fly characterization during OFF-state stress [66].

In the example shown in Fig. 1.19, the device under test is kept for most of the time in off-state condition (i.e., $V_{GS,OFF} < V_{TH}$) and it is periodically turned on (i.e., $V_{GS,MEAS} > V_{TH}$) in order to acquire the parameters evolution over time.

In this kind of characterization, it is extremely important to limit the relaxation time between the stress removal and the measurement. This allows to reduce the parameters recovery prior the actual measurement [67], thus yielding a fear evaluation of the stress-induced degradation and properly characterize the trap emission process. Moreover, it is important to optimize the number of acquisition in order to minimize the stress interruption without losing informations on the monitored phenomenon. To this end, the interruption of the stress at logarithmically spaced time intervals is a widely adopted solution [65], since it allows to distribute the acquired data over several time decades, providing an accurate picture of the parameter dynamics.

1.7 Outline

Having defined the technologies and the characterization methods that will be addressed in this thesis, we now briefly summarize the content discussed in detail in the next chapters:

Chapter 2 presents a customized measurement setup developed for the evaluation of V_{TH} and R_{ON} drifts in Silicon Carbide and Gallium Nitride Packaged devices.

Chapter 3 investigated the V_{TH} and R_{ON} drifts experienced by packaged SiC MOSFETs and identifies the main causes for the observed instabilities.

Chapter 4 discusses the problem of dynamic R_{ON} in GaN HEMTs for power applications, focusing on the role of Carbon doping in the buffer layer for Soft-Switching mode and of hot carrier issues under Hard-Switching mode and/or on-state stress conditions.

Chapter 5 treats the behavior of Fe-related buffer traps in GaN HEMTs, focusing on the mechanisms affecting the emission times for said deep-levels. Moreover, the correlation between the time dependent occupancy of Fe-traps time-dependent breakdown voltage in Fe-doped GaN HEMTs is demonstrated.

Chapter 6 presents a novel technique for temperature estimation in GaN based HEMTs whose performances are evaluated by means of TCAD Simulations and compared with state-of-the-art techniques.

Finally, Chapter 7 draws the conclusions of this work and offers an outlook on the future studies that could be performed on upcoming technologies like Ultra-Wide-Bandgap (UWB) semiconductors.

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2 Measurement Setup for V_{TH} and R_{ON} drifts characterization

2.1 Setup Overview

This Chapter treats the development of a novel measurement setup for the characterization of V_{TH} and R_{ON} drifts in packaged SiC and GaN devices. Particularly, the main goals of this chapter are: (i) to highlight the peculiarities of the measurement method employed, (ii) to describe the main parts constituting the setup and (iii) to provide a user manual for the system.

2.1.1 Principle scheme

V_{TH} and R_{ON} drifts are detrimental effects that typically manifest in SiC and GaN devices driven under conventional switch-mode operations [1, 2]. Under these operative conditions, the device is continuously switched between a large drain voltage off-state condition and a low voltage on-state one, by means of a fast gate signal. Accordingly, V_{TH} and R_{ON} drifts can be either induced by the large drain voltage applied in off-state [3, 4], by the gate voltage used for driving the device [5] or by a combination of both drain- and gate-related effects [6]. These parameters drifts could significantly impact the device performances, stability and reliability [1], suggesting the importance to gain insights the mechanisms leading to the observed degradations to provide feedbacks for improving device manufacturing. To this end, it is important to discern drain and gate contributions on parameter drifts [6], thus providing a characterization tool able to separately investigate them. Moreover, the monitoring of the parameter evolution during the stress phase can provide important information not only on the amount of degradation, but also on the dynamics (and thus on the physics) governing the parameters' drift. Particularly, in order to monitor the real evolution of V_{TH} and R_{ON} over time, it is important to reduce as much as possible the time during which the stress is removed for acquiring the parameter of interest. This is important for having a fine control on the overall stress time (i.e., cumulative stress time) and to avoid undesired recovery during parameter extraction, which could lead to an underestimation of the actual level of degradation [7]. According to this aim, the measurement procedure has to be carried out by means of on the fly characterization (OTF) [6], in which the DUT is kept for most of the time in a stress condition (e.g., high-voltage OFF-state stress), while the variation in V_{TH} and R_{ON} is evaluated by switching the devices to the ON-state for a short time interval during which the signals for V_{TH} and R_{ON} measurement are acquired through a Digital Sampling Oscilloscope (DSO). During this ON-state time interval, the measurement is performed by sweeping the gate voltage from OFF-to-ON state level through a ramp signal for extracting the threshold voltage, while a short flat gate voltage level is held at the pulse final edge for extracting the on resistance at constant

V_{GS}. This must be performed by a relatively fast gate voltage ramp and requires a specific gate driver solution for characterizing packaged devices [8]. Accordingly, a custom gate driver circuit that is able to satisfy this requirement is proposed in the designed system.

It is worth noticing that parameters drifts could either show up after short or relatively long times of operation [9], suggesting the importance to characterize both time windows in order to get a complete picture of the device behaviour [10]. If pursuing with the observation of both time intervals, the main obstacle with this approach would be a fast saturation of the oscilloscope memory in case of linearly distributed acquisitions. A clever approach to this problem is to exploit a MCU to control the operation of the DUT in stress condition and on-state biasing, while sending a trigger signal to a DSO for the V_{TH} and R_{ON} extraction in a logarithmic fashion [6, 11], i.e. collecting lots of samples in the first ms of operation and sparser samples when the stress time increases.

The designed system is composed by several parts:

- A Gate Driver circuit which is specifically designed for driving packaged devices with the required speed;
- A set of electrically controlled switches that allows to implement different types of stress/measurements;
- A DSO used for acquiring the signals for the measurement (V_G, V_D, V_{D1} and V_{SENSE});
- A low voltage power source for supplying the circuit;
- A high voltage power supply for providing the V_{PH} stress voltage under OFF-state stress conditions and conventional switch-mode operations;
- A MCU used to generate the TTL logic signals for synchronizing the stress/measurement.

By controlling the sequence of signals generated by the MCU it is possible to perform:

- High voltage off-state stress measurements under Soft-Switching conditions [3, 6, 9];
- High voltage off-state stress measurements under Hard-Switching conditions [12];
- Hysteresis measurements [8, 9];
- Positive Bias Temperature Instability (PBTI) studies [5];
- Negative Bias Temperature Instability (NBTI) studies [13, 14].

The principle scheme of the designed setup is depicted in Fig. 2.1.

The MCU’s output signals are interfaced with the circuit by means of optocouplers, in order to provide the proper level of isolation between the TTL logic and the power part of the schematic. In the simplified schematic reported in Fig. 2.1, we can see just the most important components required for the measurement. For sake of brevity, we haven’t reported the optocouplers that are needed for interfacing all the MCU’s outputs with the schematic, nor the circuits used for supplying them. Concerning the latter, the usage of isolated DC/DC converters has been identified as the way to go, with the insertion of regulators for tuning the voltage at the proper level. The circuitry and the way in which the system’s functionalities are implemented are described in the following sections.

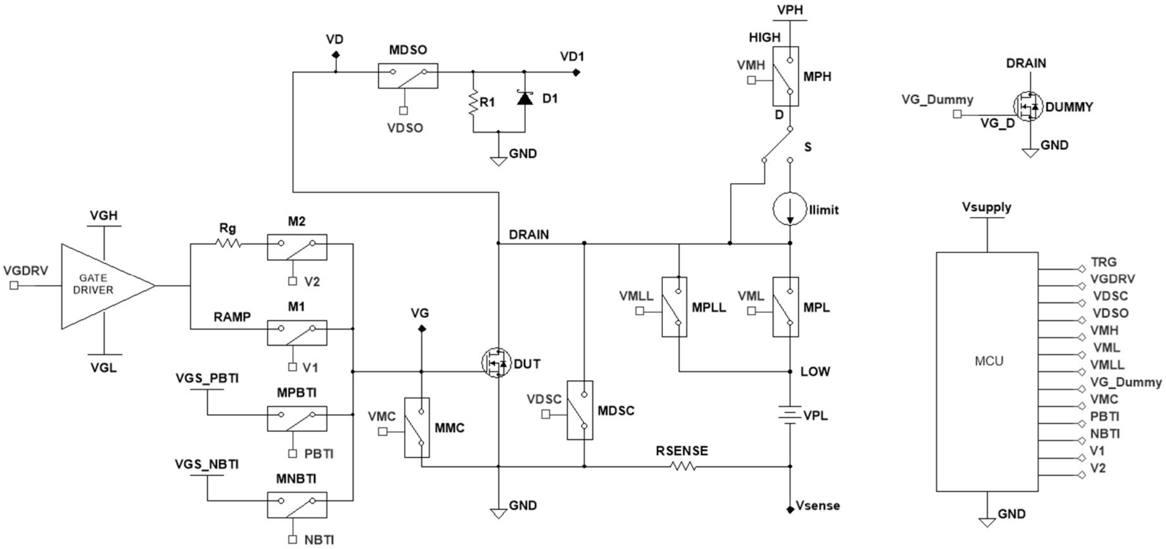

Figure 2.1: Principle scheme of the whole measurement setup

The custom Gate driver circuit allows to generate a fast V_{GS} signal ranging from V_{GL} and V_{GH} that is required for switching on and off the Device Under Test (DUT). Two electrically controlled switches (M_1 and M_2) allows to drive the DUT through a ramp-like signal for V_{TH} and R_{ON} extraction or through a gate resistance R_G. Two additional switches (M_{PBTI} and M_{NBTI}) are connected to the gate terminal to eventually perform negative or positive bias temperature instability (BTI) studies, while a Miller Clamp circuit (M_{MC}) is placed between the gate and the source terminal of the DUT. On the other hand, the drain potential can be pulsed between a low (V_{PL}) and high (V_{PH}) voltage by means of a couple of switches (M_{PH} and M_{PL}) arranged in a push-pull configuration, with an additional NMOS device (M_{PLL}) inserted for reducing the series resistance during DUT turn on. A 0.1 Ω resistor (R_{SENSE}) is connected to the DUT's source terminal in order to extract the drain current while a clamping circuit (M_{DSO}, R_1, D_1) is connected to the drain terminal of the DUT for improving the measurement accuracy at low voltages. A two-via selector (S) allows to limit the current flowing through the high voltage branch in case of Hard-Switching transitions, whereas an additional switch (M_{DSC}) is placed between the DUT's drain terminal and GND to eventually force the drain voltage to 0 V. This condition is required for monitoring the parameters recovery after the V_{PH} stress removal. A RC Snubber (not shown) is connected between the drain terminal of the DUT and ground to suppress ringing [15]. Finally, a dummy transistor is placed in parallel to the DUT to allow the system warm up and guaranteeing a stable characterization.

2.2 Gate Driver

The gate driver circuit is responsible for switching the DUT ON and OFF and is devoted to the generation of the ramp signal required for the extraction of the V_{TH} and R_{ON} values. For performing on-wafer measurements, the usage of a simple waveform generator would be sufficient, thanks to the small parasitic capacitances of the DUTs. However, this solution is not viable for characterizing packaged devices due to the gate-to-source capacitances (C_{GS}) in the order of few nF [16]. In fact, the simultaneous presence of large C_{GS} and 50 Ω characteristic impedance of conventional waveform generators (WFGs) would result in the low-pass filtering of the V_{GS} ramp, yielding a significant reduction in the measurement speed [8]. For this reason, a custom gate driver circuit is required to prevent any distortion of the ramp signal, thus ensuring a fast and accurate V_{TH} extraction. The typical waveforms corresponding to the gate driver circuit are depicted in Fig. 2.2.

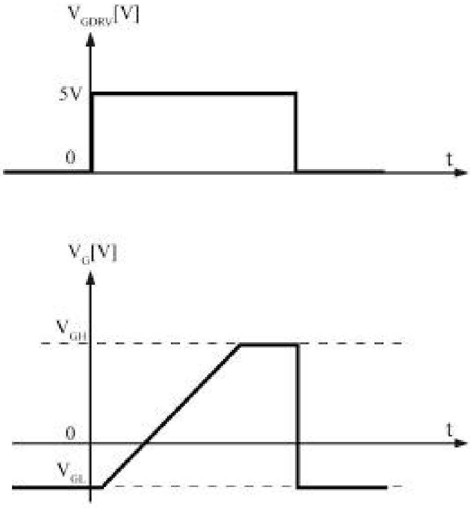

Figure 2.2: Representation of a typical gate driver response. In correspondence of a step signal between 0 to 5 volts on V_{GDRV}, a ramp signal is generated at the gate of the DUT, taking V_G from V_{GL} to V_{GH}.

The V_{GDRV} signal is generated by the MCU and controls the activation of the gate driving voltage applied to the DUT. When the V_{GDRV} signal changes from low to high logic level (i.e., from 0V to 5V) the gate voltage starts to linearly increase from the low level V_{GL} to the high V_{GH} level. Then, the V_{GH} level is kept till the following commutation of V_{GDRV} signal to its low level. The time duration of the generated V_{GDRV} signal defines the on-state time of the DUT. At this point, it is important to focus on the way in which the ramp-like V_G signal is obtained during this time interval.

2.2.1 Implemented solution

The custom gate driver should be able to generate a V_{GS} signal presenting two important features: the V_{GS} signal (i) should present a fast and non-distorted ramp-like shape and (ii) should be weakly affected by the connected load (i.e., by the C_{GS} of the DUT). These two requirements are very important in order to provide a fast characterization that is guaranteed for a wide range of packaged devices (i.e., presenting different C_{GS} values).

In principle, if we are able to properly drive a load presenting a capacitance sufficiently higher than those presented by the devices to be characterized, the ramp signal will be non-distorted by the connected DUT, and the driving circuit will be load-independent.

The solution adopted for this purpose is schematically depicted in Fig. 2.3.

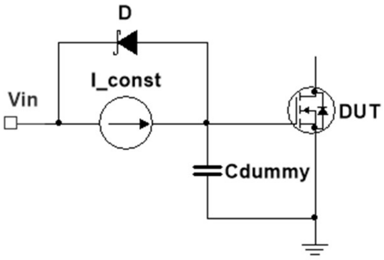

Figure 2.3: Schematic representation of the solution proposed. A relatively large "dummy" capacitor is connected in parallel to the DUT gate-source junction, so that the overall load capacitance is dominated by C_{dummy}. A constant current is provided in order to obtain a ramp like voltage on the gate terminal of the DUT.

The basic idea behind the purposed solution relays on the fact that, by charging a load capacitor with a constant current, it is possible to obtain a voltage ramp whose slope is directly proportional to the charging current [17]. Thus, it is necessary to design a circuit able to provide a constant current that is large enough for charging a "dummy" load capacitor in very short time interval (i.e., in the micro-seconds time range).

The design formula that defines the required charging current is:

$$I = C_{dummy} \times \frac{dV}{dt} \tag{2.1}$$

where C_{dummy} is the value of the dummy capacitor that has to be charged and dV/dt is the voltage slope required for the generated ramp. In the design phase, it is important to set the slope of the ramp (dV/dt) at the maximum desired, in order to fix the proper constraint for the current.

On the other hand, the choice of the "dummy" capacitor is driven by the target DUT's specifications. Considering the worst case as the leading one, the C_{GS} upper bound settles around 10 nF, yielding to the choice of C = 47 nF as a good compromise for this application.

2.2.2 Current limiting circuit

According to the solution proposed, a circuit able to generate a constant charging current is required. To this end, a current limiting circuit can be adopted. Particularly, the current limiting circuit was implemented through a couple of N-MOS depletion mode transistors (e.g., BSS159N) connected in parallel (see Fig. 2.4).

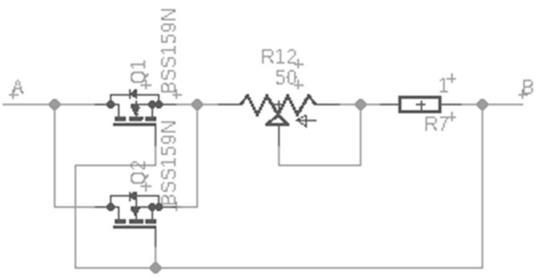

Figure 2.4: Circuit of the implemented current limiting circuit. Two depletion mode NMOS connected in parallel are degenerated through a variable source resistance to control the flow of current through the branch.

By paralleling two N-MOS transistors, the current capacity of the limiting circuit is doubled, thus increasing the speed capability of the gate driver. With this configuration we can easily obtain the current level previously designed just by inserting a fixed series resistance. In this way, it is possible to satisfy the maximum voltage slope defined by the design. However, since the charging current depends on the voltage sweep and defines the ramp-time, it is important to make this parameter tunable in order to adjust it according to the characterization requirements. In fact, the ramp-time sets the time required to reconstruct the I_D-V_{GS} characteristic of the DUT during the measurement phase, making it an important parameter for the characterization in terms of accuracy. Thus, it is important to adjust the output current according to the measurement to be accomplished. In order to do that, a variable resistor connected in rheostatic configuration (R_{12}) was used.

Another important consideration concerns the high-to-low transition of the gate signal; in fact, we expect to see an almost vertical transition when the DUT has to be turned off. In order to guarantee this kind of behavior, it is sufficient to add a switching diode in parallel to the current limiting circuit (see Fig. 2.5). A Schottky diode (e.g., 1N5819) allows to obtain a fast enough transition whose slope can be controlled through the series resistance (R_{13}).

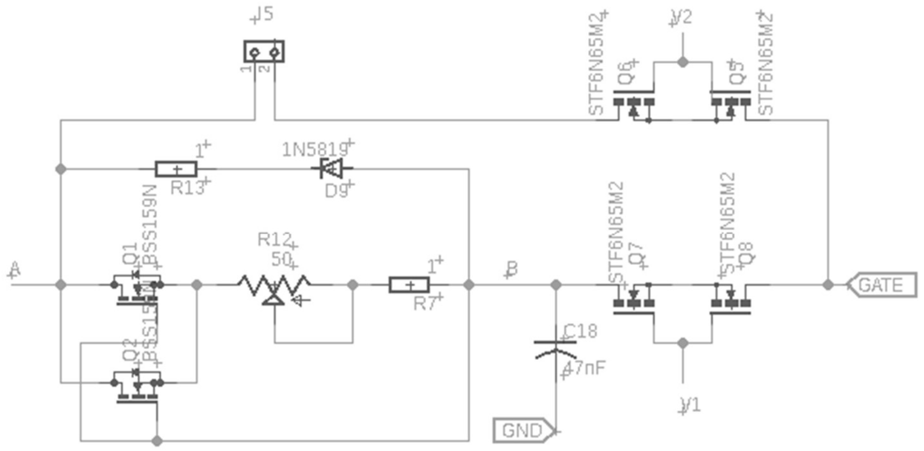

Figure 2.5: Schematic of the circuit employed for the generation of the ramp-like V_{GS} signal and switches for selecting between the R_G and Current limiter branch.

Further looking at Fig. 2.5, it is possible to recognize two separated branches. In the lower branch, it is reported the gate driver solution described so far, whereas the upper branch presents a two pin connector (J_5). This connector has been added for inserting a discrete gate resistance (R_G) for monitoring the DUT behaviour under Hard-Switching mode operations. To independently activate the two branches, two couples of switching transistors (i.e., Q_5, Q_6 for upper branch and Q_7, Q_8 for the lower branch) have been inserted. This allows a perfect synchronization between the two branches during hard-switching mode operations and allows to electrically disconnect both branches from the DUT's gate terminal in case of NBTI/PBTT stress.

With the circuit designed, we have a complete control of the ramp-like signal required for measuring the I_D-V_{GS} curve in the measurement phase. On top of this, a constant voltage level is required at the end of the ramp for providing a correct R_{ON} measurement by averaging several samples of drain current and voltage. In order to obtain this constant voltage level at the ramp edge, a voltage limiter circuit is used. Particularly, the voltage limit must be adjustable in order to obtain a versatile tool for characterizing different types of DUT (i.e., different technologies requiring different gate driving voltage) and/or to extract R_{ON} at several V_{GS} levels. In the same way, we need also to limit the lower voltage level for the ramp, to have the possibility to characterize both normally-OFF and normally-ON devices.

Before considering the way in which the voltage can be limited in the two phases just cited, we have to consider the way in which the gate driving voltage is generated. The gate biasing is triggered with a TTL signal generated by the MCU. Thus, a proper level of insulation between the TTL signal and the power circuit that actually biases the gate terminal of the device under test is required. In order to obtain this effect, an optocoupler is used (see Fig. 2.6).

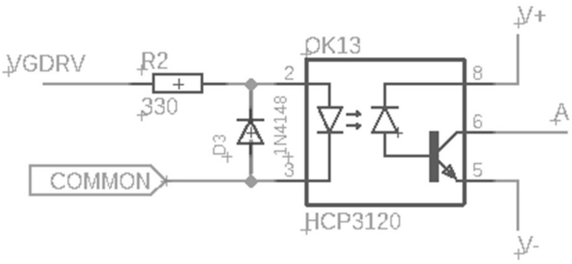

Figure 2.6: Optocoupler employed for generating the ramp-like gate voltage according to the V_{GDRV} signal generated by the MCU.

At the input section of the optocoupler, the V_{GDRV} signal is used for driving the circuit. Accordingly, the output terminal switch between V+ and V- providing the input voltage at the current limiting circuit. The two supply voltages (V+ and V-) have to be somehow generated and for this purpose two isolated DC/DC converters are used (see Fig. 2.7).

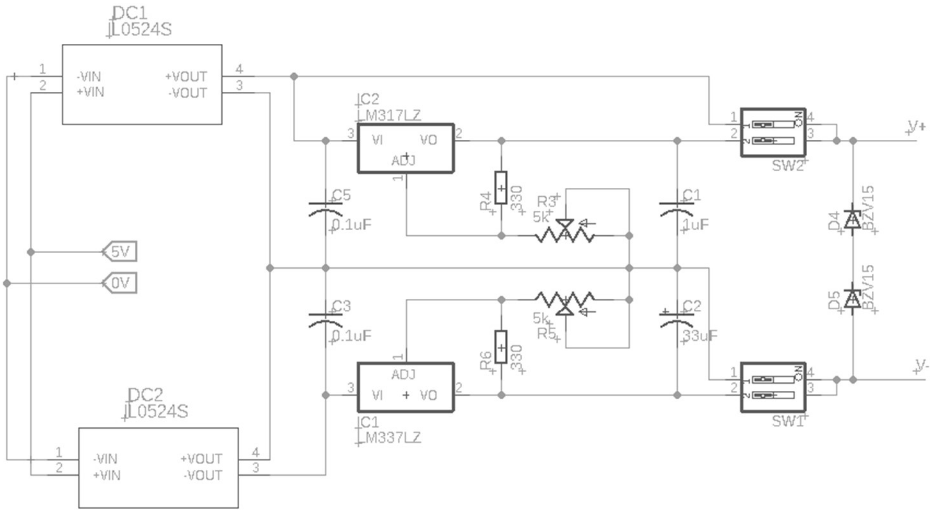

Figure 2.7: Schematic of the circuit employed for providing the V+ and V- voltage to the optocoupler used for driving the Gate of the Device Under Test.

The converter chosen generate a 24 V output starting from a 5 V DC input. Exploiting two DC/DC converters connected in series, it is possible to obtain the dual supply required for this application. The positive +24 V obtained at the output can be directly connected to the V+ terminal of the optocoupler, in order to have the ability of biasing the DUT at the maximum voltage available. At the same time, we want the possibility of controlling the voltage level provided at the optocoupler in order to reduce the wasted power when the output voltage is limited. To this end, a dual in-line package (DIP) switch allows to select V+ between the constant +24 V level and an adjustable voltage level set by a linear voltage regulator (e.g., LM317). For the same reason, the voltage applied at the V- terminal is controllable by means of a linear negative voltage regulator (e.g., LM337), while a simple DIP switch allows to set the low voltage at 0 V. In this way, the V_{CC}-V_{EE} difference applied to the coupler can be simply varied, respecting the operative limits of the component.

To safely respect the maximum difference V_{CC}-V_{EE} allowed by the integrated optocoupler, a couple of Zener diode sustaining 15 V are series connected and placed in parallel to the supply chain, thus limiting the voltage range below 30 V.

The voltage V+ is equal to the positive supply voltage of the optocoupler (V_{CC}) and so the ramp generated will always try to reach this target value. In order to limit the positive voltage to a predefined (i.e., lower) value, obtaining the flat region for extracting R_{ON}, we exploit an adjustable voltage limiting circuit (see Fig. 2.8).

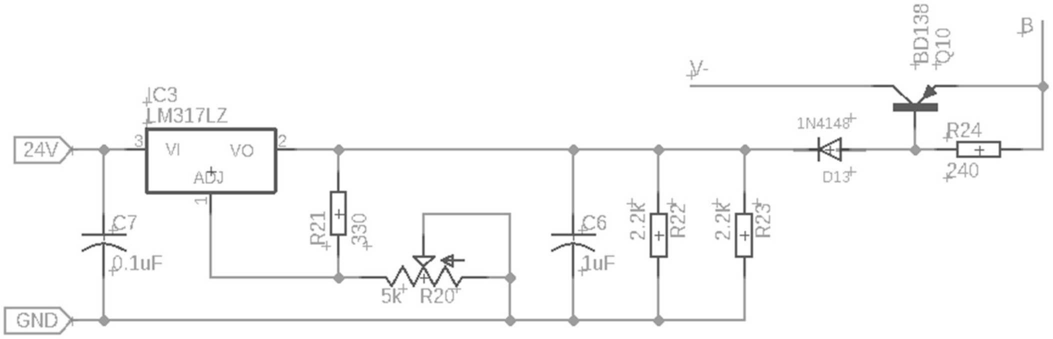

Figure 2.8: Schematic of the Voltage Limiting circuit employed in the Gate Driver for obtaining the stable V_{GS} level at the end of the ramp-like signal

The limit voltage can be regulated through the linear voltage regulator LM317, by acting on the trimmer R_{20}. When the voltage at the node "B" (i.e., at the output of the current limiter) reaches the V_{GH} value set the voltage limiter, the excessive current is sank by the PNP bipolar junction transistor (Q_{10}) and the voltage on C_{dummy} saturates, thus yielding the flattening required for a correct R_{ON} extraction at constant V_{GS}.

As already mentioned in the principle scheme of Fig. 2.1, an additional Miller clamp circuit is connected between the gate and the source of the DUT. This is implemented through a couple of mosfets (Q_{11}, Q_{12}) connected in anti-series (M_{MC} in Fig. 2.1) that are used for avoiding the self-turn-on of the DUT under high voltage off-state stress measurements (see Fig. 2.9). This additional precaution is needed when the device is turned off with a non-negative gate bias and the large stress voltage applied to the drain terminal presents a fast rising edge. The high harmonic content presented by this steep transition could cause the unwanted turn on of the DUT due to the capacitive coupling offered by the C_{GD} parasitic capacitance. The undesired high-frequency current passing through C_{GD} is thus diverted into M_{MC}, keeping the DUT safely in its off state condition [18]. Another option consists in selecting a negative V_{GL} values able to mitigate the effect just described, but this could introduce additional stress on the gate that would affect the measurement.

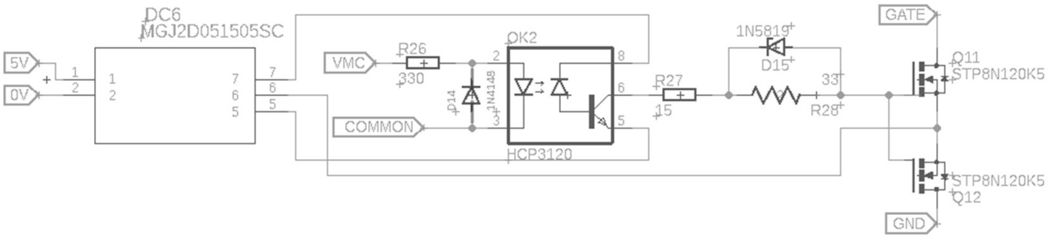

Figure 2.9: Schematic of the Miller Clamping circuit inserted in order to eventually clamp the gate voltage during high voltage off-state stress measurements

All the circuitry just described is connected together to form the PCB board shown in Fig. 2.10.

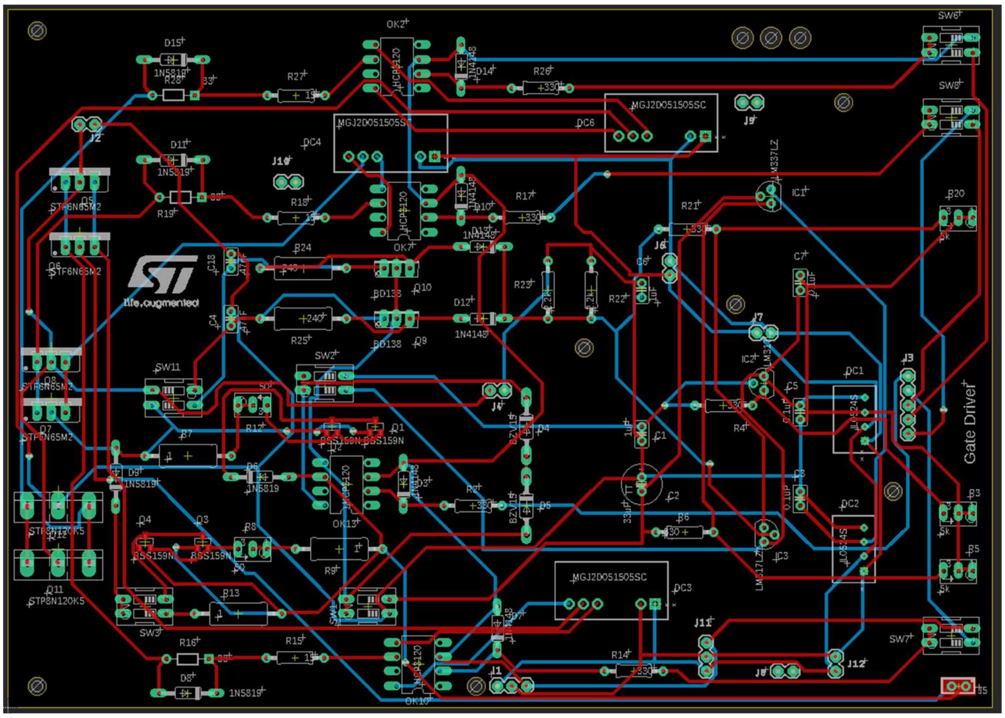

Figure 2.10: Picture of the Gate Driver Board drawn in Eagle PCB Design.

2.3 Drain Pulser

Another key part of the system is the Drain Pulser circuit. To realize it, a specific Drain Pulser Board has been designed, in which we can find all the BNC connectors required for supplying the setup and for providing the signals to the DSO. Moreover, this board presents the circuitry needed for switching the drain voltage under pulse-mode operation. Particularly, in order to perform high voltage off-state stress measurements, it is necessary to provide a relatively high voltage to the drain of the DUT. To this end, a NMOS transistor is connected between the “HIGH” terminal (i.e., positive terminal of the high voltage power supply) and the drain terminal of the DUT (see Figure 2.11). The NMOS is degenerated trough a source fixed resistance and a trimmer placed on the J_{20} connector. This allows to control the slope of the low-to-high voltage transitions when Q_{15} is activated by the V_{MH} signal coming from the MCU.

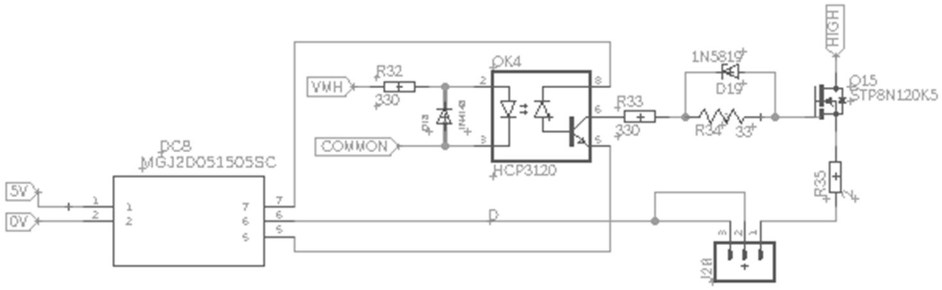

Figure 2.11: Schematic of the circuit used for activating the high-voltage branch that provides the off-state drain voltage stress to the DUT.

Concerning high-to-low voltage transitions, a couple of NMOS are connected between the drain of the DUT and the “LOW” terminal (see Figure 2.12). These two NMOS (corresponding to the switch M_{PL} in Fig. 2.1) are connected in anti-series to prevent the conduction through their body diodes when the DUT is driven under Hard-Switching mode operation [12].

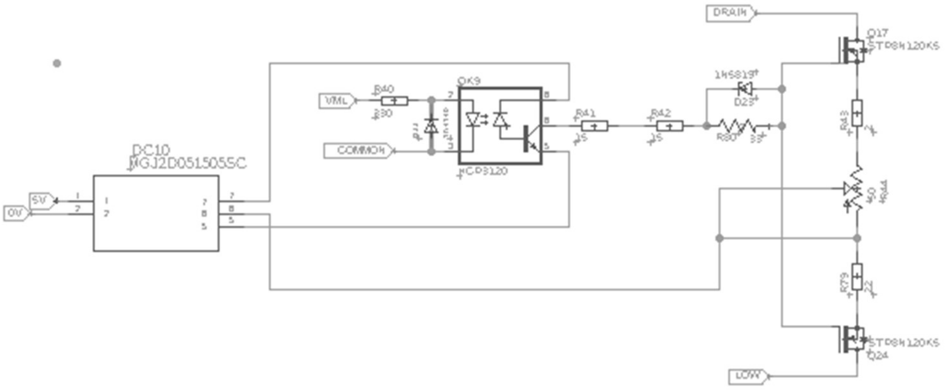

Figure 2.12: Schematic used for the implementation and the control of the M_{PL} switch.

Once again, the NMOS transistors are degenerated with two fixed source resistances and a variable resistance in order to control the slope of the transitions. This is very important for controlling the dV/dt rate of the drain waveform.

On the same branch, another couple of NMOS transistors is connected in parallel to the “DRAIN” and “LOW” terminals (see Figure 2.13). These two transistors present a very low on-state resistance and are inserted to provide a low impedance path between the V_{PL} circuit and the DUT during the on-state time interval.

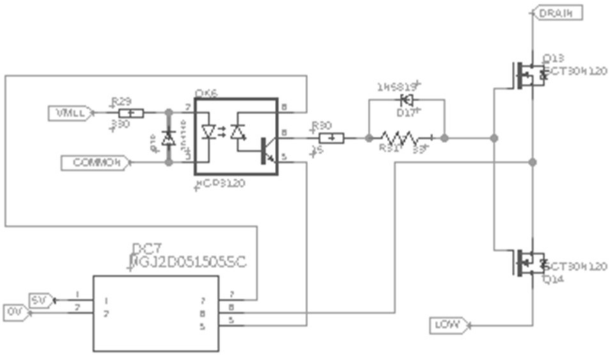

Figure 2.13: Schematic used for the implementation and the control of the MPLL switch.

An additional NMOS transistor (see Fig. 2.14) is connected between the DUT drain terminal and GND. This allows to eventually clamp the drain voltage to ground in off-state conditions, to monitor the parameters recovery after the high voltage off-state stress phase. The activation of this transistor can be also used under NBTI/PBTI measurements to keep the drain voltage at 0 V during the stress. This allows to prevent drain induced effects and investigate just gate-induced instabilities.

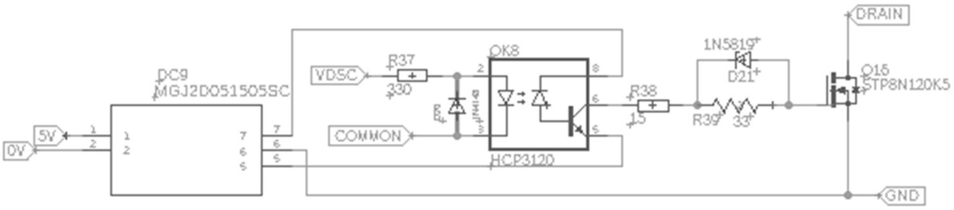

Figure 2.14: Schematic used for the implementation and the control of the MDSC switch.

Another important part of the circuit is depicted in Fig. 2.15. A drain clamping circuit is connected to the drain terminal of the DUT in order to acquire the signal V_{D1} only during the on-state time interval. This allows to select the best scale in the DSO for the on-state drain voltage measurement, thus obtaining the best achievable accuracy for the R_{ON} measurement.

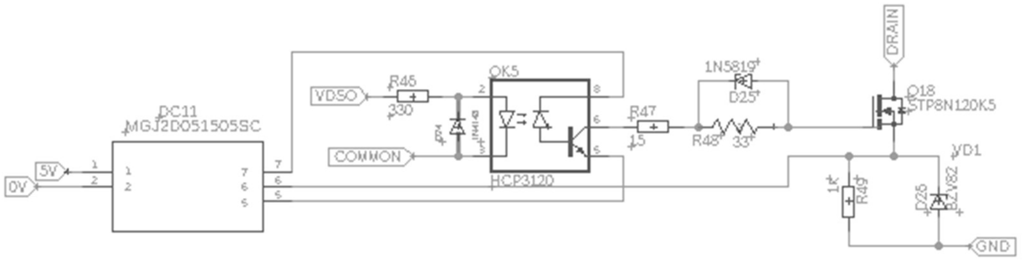

Figure 2.15: Schematic used for the implementation and the control of the drain clamping circuit that allows to select the best scale in the DSO for the on-state voltage measurement.

On the Drain Pulser Board, another important part is constituted by the Dummy transistor driver. In fact, a dummy transistor is typically connected in parallel to the DUT (i.e., it shares the same Drain and Source connections of the DUT) to allow a controlled warm up of the system. In fact, the setup presents several components that could be affected by thermal and electrical transients which could yield different conditions during the characterization. To prevent this issue, a series of non-stress cycles is applied to a dummy transistor prior to the real characterization of the DUT. In this way, the warm up of the setup will be experienced by the dummy transistor which is the only one that is turned on in this phase. This allows to reach a steady state condition, after which the dummy transistor is excluded and the characterization is performed on the actual DUT. In this way, the DUT charactirazion can be safely performed without thermal or electrical transients on the setup components, thus providing stable measurement conditions.

This solution is implemented through the schematic reported in Fig. 2.16, in which a dedicated gate driver signal is applied to the Gate terminal “VG_D” of the dummy transistor during the warm up phase. At the same time, the DUT is not activated, thus avoiding undesired stress on the device to be characterized. In this way, the dummy transistor will sink the current provided by the setup during the warm up phase, while the DUT will be turned on during the real measurement sequence in which the setup has already reached its steady state.

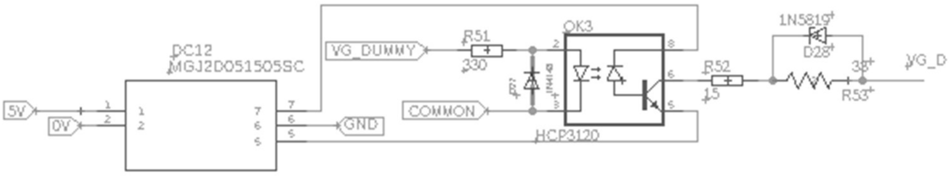

Figure 2.16: Schematic used for the control of the dummy transistor used during the warm-up of the system.

The circuits just described have been designed in Eagle PCB Design, yielding the Board layout shown in Fig. 2.17.

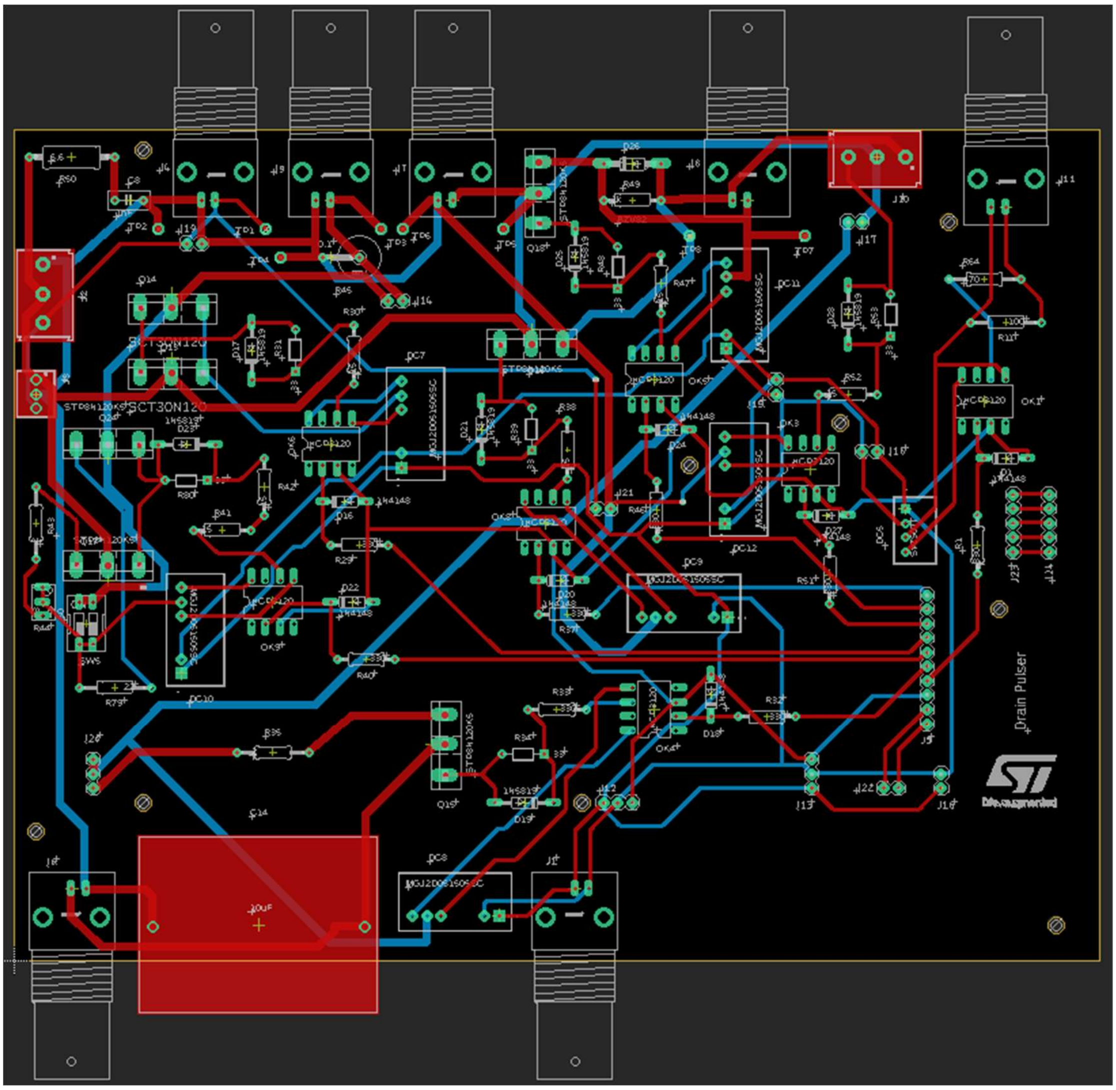

Figure 2.17: Picture of the Drain Pulser Board drawn in Eagle PCB Design

2.4 V_{PL} Circuit

In order to generate the low voltage level required during the turn-on phase of the DUT, a dedicated circuit, hereby named V_{PL}, has been designed. Particularly, the V_{PL} circuit is connected between the LOW terminal and the V_{SENSE} terminal of the setup.

This circuit is shown in Fig. 2.18 and consists of two main parts:

- Voltage Generation
- Series Resistance

Concerning the Voltage Generation part, five isolated DC/DC converters connected in parallel and a linear voltage regulator have been used. The usage of five DC/DC converters allows to increase the power capability of the setup, thus allowing to drive the DUT at higher current levels. On the other hand, for having the possibility to adjust the voltage level provided in on state, the LM317 linear voltage regulator has been used, giving the possibility to change the voltage level by acting on the trimmer R_{78}.

The second part of the circuit allows to choose the series resistance connected to the voltage generator. This is possible thanks to several switches (SW_{12}, SW_{13}, SW_{14}, SW_{15}) that allow to change the series resistance value between 0.1 and 2 Ω with 0.1 Ω steps. This option allows to change the current sank by the DUT in triode region (where R_{ON} is extracted) while keeping constant the voltage at which V_{TH} is evaluated.

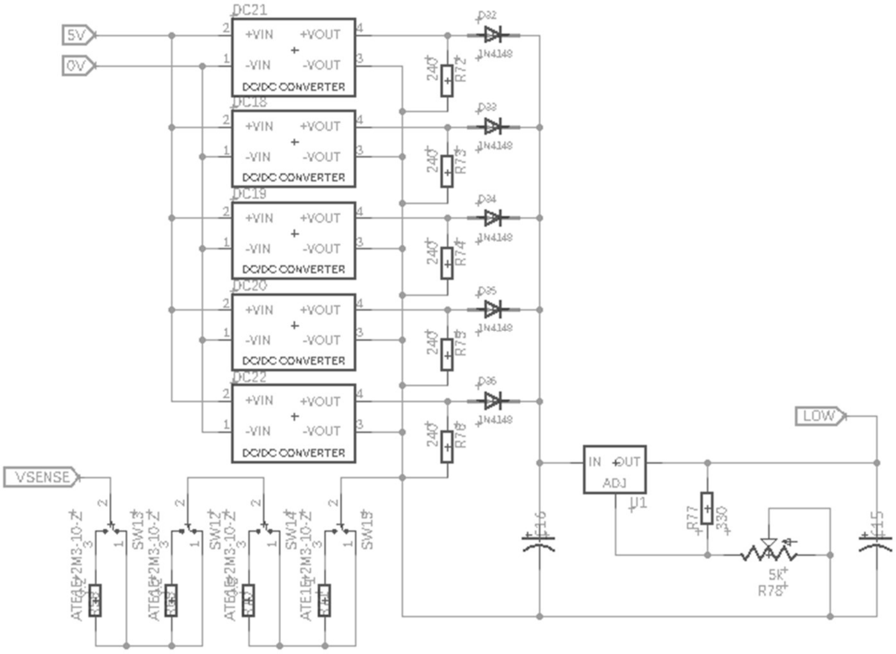

Figure 2.18: Schematic of the designed V_{PL} circuit

The PCB Board corresponding to the designed V_{PL} circuit is reported in Fig. 2.19.

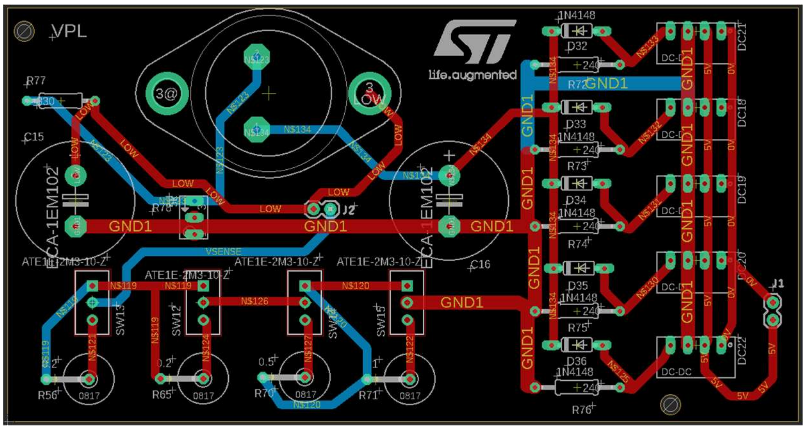

Figure 2.19: Picture of the V_{PL} Board drawn in Eagle PCB Design

2.5 NBTI/PBTI Board

In order to implement the possibility to perform NBTI and PBTI stress on the DUT, a specific Board has been designed (see Fig. 2.20). Particularly, this circuit allows to generate negative $V_{GS,NBTI}$ stress down to -20 V and positive $V_{GS,PBTI}$ stress up to +20 V. The circuit is composed by two different branches: one for negative and one for positive stress. In both cases, a linear voltage regulator (based on LM337 and LM317 respectively) is used to set the stress voltage. The two branches are connected to the gate of the DUT through NMOS switches (Q_{19}, Q_{20} for NBTI and Q_{21}, Q_{22} for PBTI) that allows to electrically exclude the stress voltage when desired. This allows to periodically turn-on the DUT by generating the ramp-like gate signal for V_{TH} and R_{ON} extraction. Accordingly, the V_{GS} applied for the measurement is totally independent on the stress condition. This allows, for instance, to evaluate the effect of different stress voltages on the V_{TH} and R_{ON} drifts, while comparing results obtained under the same measurement conditions (i.e., allowing consistent extractions and direct results comparison).

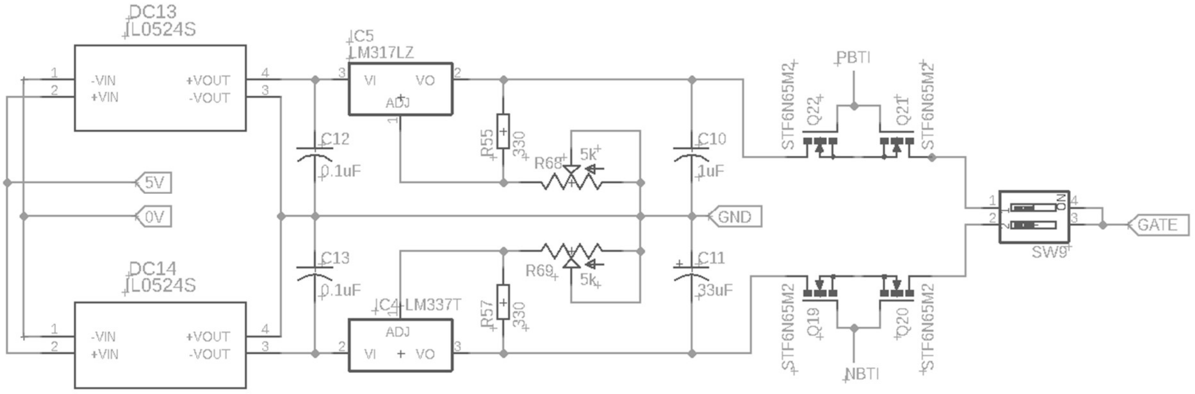

Figure 2.20: Schematic of the NBTI/PBTI circuit

The voltage level for PBTI and NBTI stress can be adjusted by acting on the trimmers R_{68} and R_{69}, respectively. The DIP switch SW_9 allows the user to exclude the connection of these two additional branches when not required. This could be useful to avoid undesired load to the DUT's gate terminal when NBTI and/or PBTI studies are not performed.

The layout of the designed PCB board is depicted in Fig. 2.21.

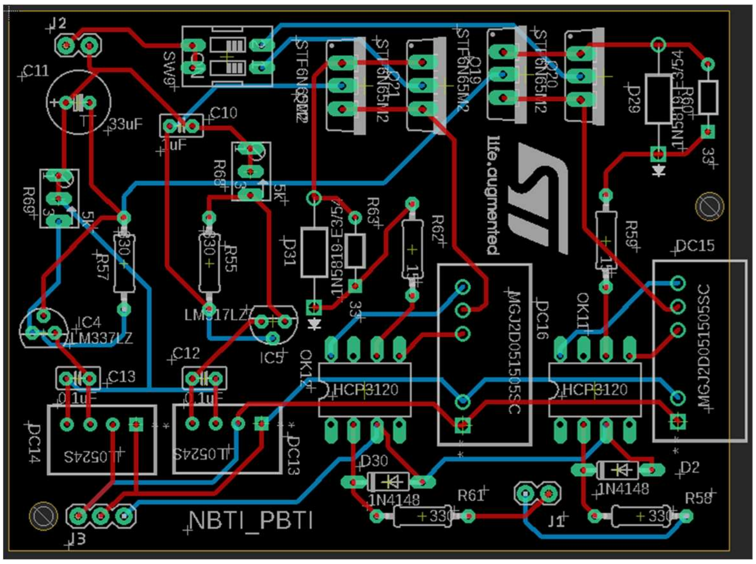

Figure 2.21. Picture of the NBTI/PBTI Board drawn in Eagle PCB Design

2.6 Hard-Switching Board

The Hard-Switching (HS) Board allows to select between two switching mode operation: (i) Soft-Switching mode (i.e., in which high-low and low high voltage transitions are performed at zero current) and Hard-Switching mode (i.e., in which transitions are led at constant current). Accordingly, a current limiting circuit has been inserted in the high voltage branch, with a 2-vias selector (SW_{16}) which allows to exclude the current limiting circuit in case of Soft-Switching mode operation (see Fig. 2.22).

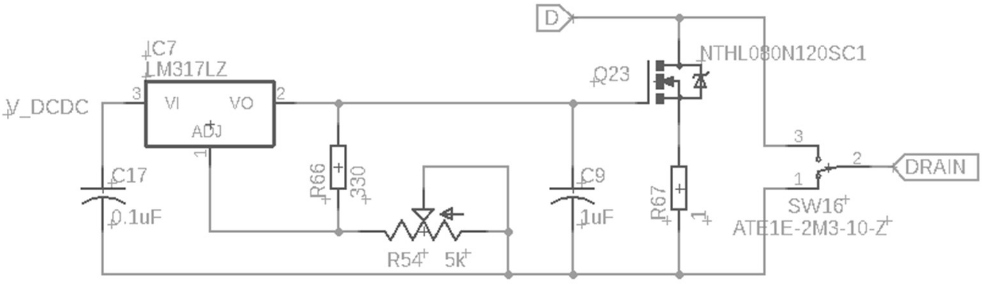

Figure 2.22: Picture of the Hard-Switching Board circuit

For the design of the current limiting circuit, a power enhancement mode transistor operating in saturation region has been used (Q_{23}). Accordingly, by acting on the gate voltage applied to this transistor, it is possible to regulate the current level (I_{limit} in Fig. 2.1). The gate voltage regulation is performed through a commercial DC/DC isolated converter connected to a linear voltage regulator (e.g., LM317). Moreover, since the drain current presents a quadrating dependence on the gate-to-source voltage applied, a degeneration resistance has been connected to the source of the current limiting transistor (R_{67}). This solution allows to implement a negative feedback that is required for a finer control of the imposed current. By acting on the trimmer R_{54} in Fig. 2.22, it is possible to regulate the limiting current at which transitions are performed. The PCB Board is shown in Fig. 2.23.

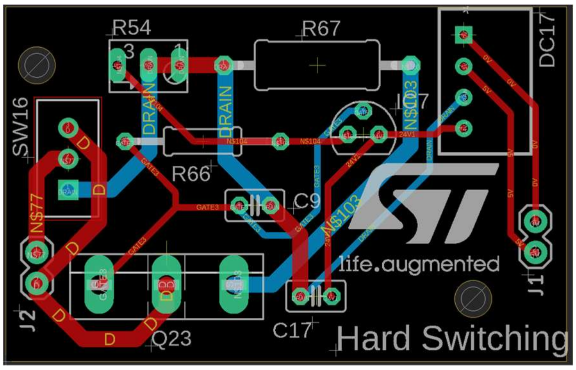

Figure 2.23: Picture of the Hard-Switching Board designed with Eagle PCB design

2.7 MCU Board

In order to provide a stable connection between the MCU and the circuit, a dedicated PCB board has been designed (see Fig. 2.24). Particularly, this board allows a stable placement of the MCU and of the USB-RS232 module (required for the communication with the PC), while providing all the connection between these two blocks. Moreover, the signals generated by the MCU are provided to the upper circuit layers through a vertical connector, which allows a modular and easy connection of the boards composing the system.

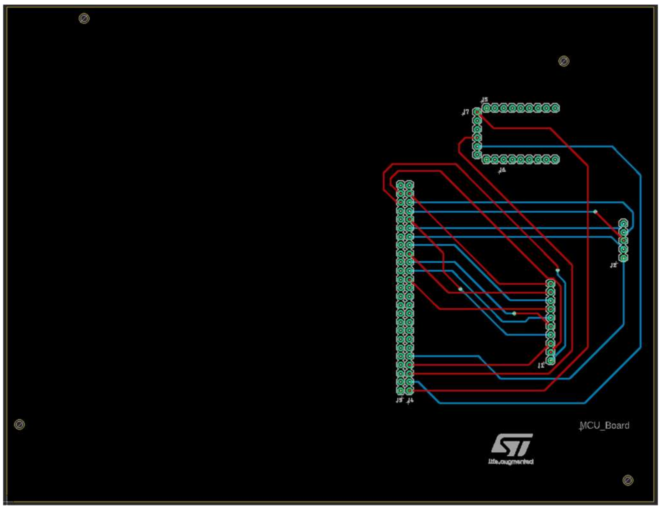

Figure 2.24: Picture of the MCU Board designed with Eagle PCB Design

2.8 User Manual

2.8.1 Power Supply Setting

The measurement setup requires two distinct power supply to operate.

- A low voltage power supply (see Fig. 2.25(a)) is required in order to provide a constant 5 V level to supply the whole system (i.e., supply the DC/DC isolated converters);
- A high voltage power supply (see Fig 2.25(b)) is required for providing the high voltage stress during off-state stress measurements.

In Fig. 2.25, we highlighted the most important buttons/needles on the front panel of the two power supply.

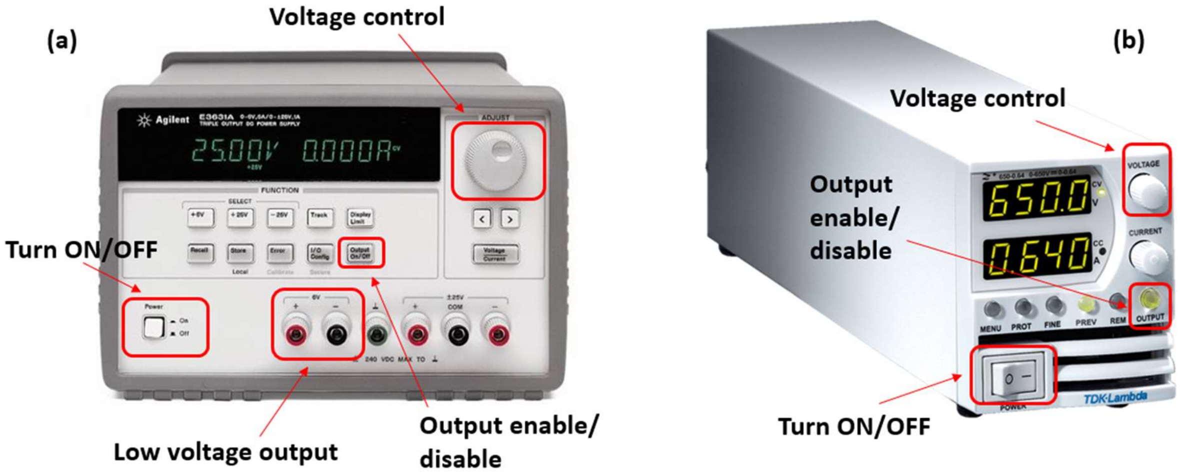

Figure 2.25: (a) Low voltage and (b) High voltage power supply. We highlighted the most important buttons on the front panel of each instrument.

Before connecting these instruments to the circuit, it is important to set the voltage levels required for the measurements and disable the power supply's outputs. This guarantees to safely connect the instruments to the circuit without providing undesired voltages.

Procedure to set the low voltage power supply:

1) Turn ON the low voltage power supply;
2) Select the 6 V Output port as low voltage supply;
3) Enable the power supply output through the Output enable/disable button;
4) Regulate the output voltage to 5 V through the Voltage control needle;
5) Disable the power supply output through the Output enable/disable button.

Procedure to set the high voltage power supply:

1) Turn ON the High voltage power supply;

2) Enable the power supply output through the Output enable/disable button;
3) Regulate the output voltage to the stress voltage required for the off-state stress through the Voltage control needle (eventually, select the "FINE" button for a better control);
4) Disable the power supply output through the Output enable/disable button.

2.8.2 Connections to the circuit

On the front side of the setup we can see two BNC connectors (Fig. 2.26):

- The BNC connector on the right, marked with the label "5 V", is used to supply the measurement setup. The corresponding BNC cable is connected to the low-voltage output channel of the DC power supply "Keysight Technologies E3631A" [19].
- The BNC connector on the left, marked with the label "V_H", is used to provide the high-voltage required for off-state stress measurements. The corresponding BNC cable is connected to the high-voltage power supply "TDK-Lambda Z650-0.32-U" [20].

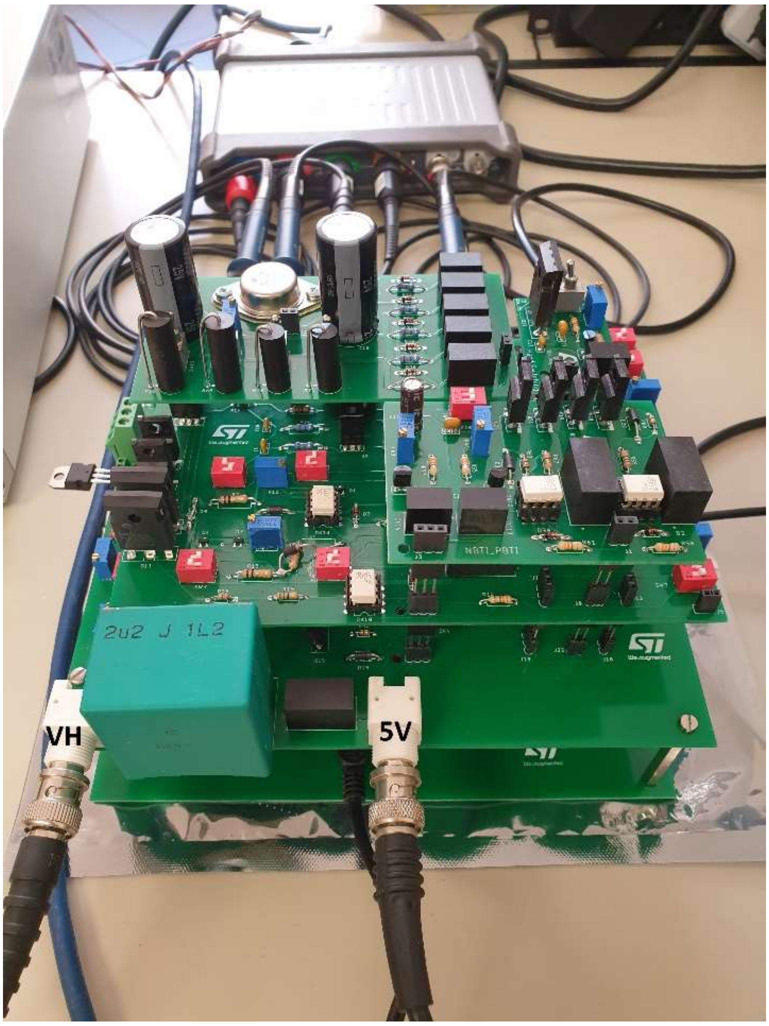

Figure 2.26: Front side view of the setup

In Fig. 2.27 we reported the side view of the setup, from which we can see that the rear panel features five BNC connectors. These BNC connectors are used to bring the signals from the circuit board to the digital sampling oscilloscope (DSO). Particularly, the signals “V_G”, “V_{SENSE}”, “V_D” and “V_{D1}” are acquired by means of four voltage probes connected to the four channels of the DSO, while the signal “TRG” is connected to the External trigger input of the DSO by means of a BNC cable.

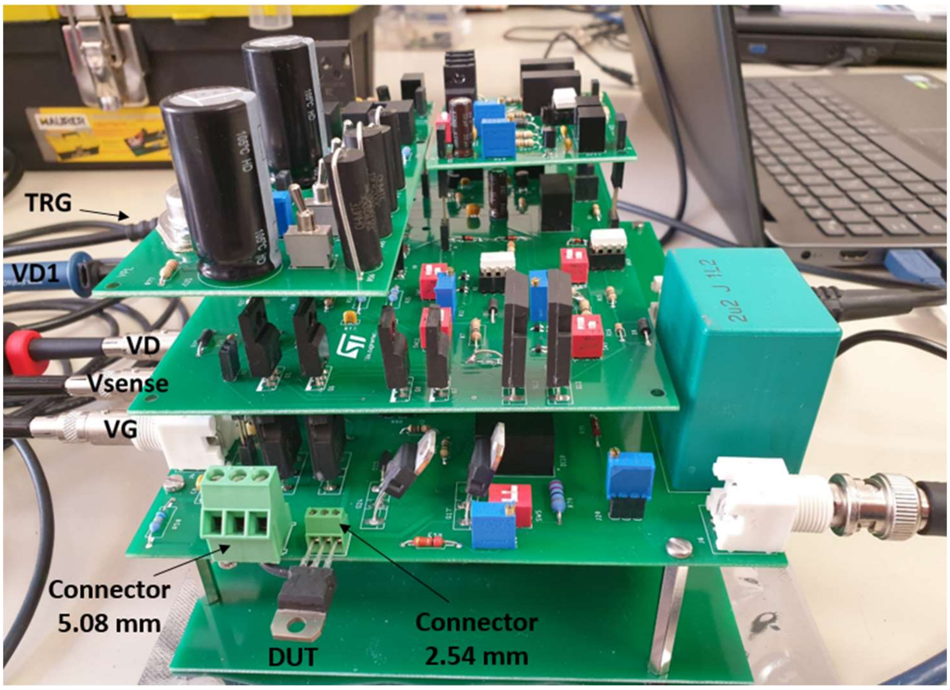

Figure 2.27: Side view of the circuit

Further looking at Fig. 2.27, we can see two 3-pins connectors on the left side of the setup. These connectors allow to fix the device under test (DUT) to the setup; particularly, only one of them will be used for each measurement. In fact, the 3-pins connectors feature a different pin spacing (5.08 mm for the one on the left and 2.54 mm for the one on the right). This allows to directly connect devices with different packaging (i.e., TO-247 on the left and TO-220 on the right). Another important difference between these two connectors concern the pin order. In fact, the connector on the left (5.08 mm spacing) present a Gate-Drain-Source pin order (from right to left), while the connector on the right (2.54 mm spacing) present a Gate-Source-Drain pin sequence (from right to left). This difference is due to the fact that tested TO-220 packaged devices frequently presented the source terminal on the central pin, while for TO-247 package, the central pin typically refers to the Drain terminal (see Fig. 2.28).

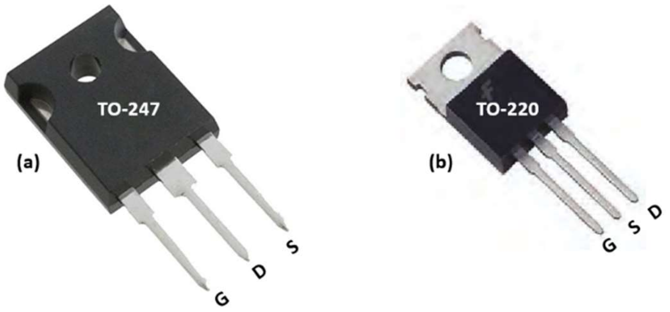

Figure 2.28: (a) TO-247 package and (b) TO-220 package with corresponding pin orders

2.8.3 Digital Sampling Oscilloscope (DSO)

The Digital Sampling Oscilloscope (DSO) is used to acquire the signals required for the measurement. To this end, a four-channel PicoScope 5000 Series [21] with 14-bit resolution and a 200 MHz maximum bandwidth was used. Particularly, the rapid block mode was used for data acquisition in order to improve the time accuracy of the system. In fact, in this operative mode, the oscilloscope's segmented memory is used to store the acquired data. The stored data are then delivered to the PC only when the complete block has been acquired, thus eliminating the delay due to data visualization between consecutives acquisition. This optimizes the time resolution of the instrument, being constrained just by the maximum number of points that can be stored in the DSO's memory.

In this work, the number of point for each acquisition was set to 3000. Accordingly, the maximum number of acquisitions allowed is 4136, since the maximum number of points that can be stored in the DSO's segmented memory is 125000000.

The connections to the DSO are briefly summarized in Fig. 2.29.

Figure 2.29: Digital Sampling Oscilloscope (DSO) connections.

The Digital Sampling Oscilloscope (DSO) used in this system present four channels for the signals acquisition and an additional channel for the external trigger signal.

The DSO’s channels are connected as follows:

- Channel A is connected to a 100x voltage probe in order to monitor large drain voltages eventually applied in off-state stress conditions (V_D);
- Channel B is connected to a 1x voltage probe in order to measure the drain voltage experienced by the DUT in on state condition (V_{D1});
- Channel C is connected to a 1x voltage probe in order to measure the voltage drop across a sense resistor and extract the drain current in on-state (V_{SENSE});
- Channel D is connected to a 10x voltage probe in order to measure the gate voltage applied to the DUT (V_G). A 10x probe allows to measure gate signals above the 20 V limit of the DSO, exploiting the attenuation factor of the probe;
- External trigger is connected to a BNC cable that brings the trigger signal (TRG) from the circuit to the DSO, thus allowing to trigger the acquisition only when required.

2.8.4 MicroController Unit (MCU)

The MicroController Unit (MCU) that is used in this setup is the dsPIC33EV256GM106 by Microchip [22]. The choice was led by the fact that this MCU presents a relatively high number of output ports and a high operation frequency of 70 MIPS. The former guarantees the scalability of the system, giving the possibility to implement new signals and functionalities, while the latter provides the speed needed for a fast control of the whole measurement setup.

A picture of the MCU board is shown in Figure 2.30, accompanied by its main parameters reported in Table 2.1.

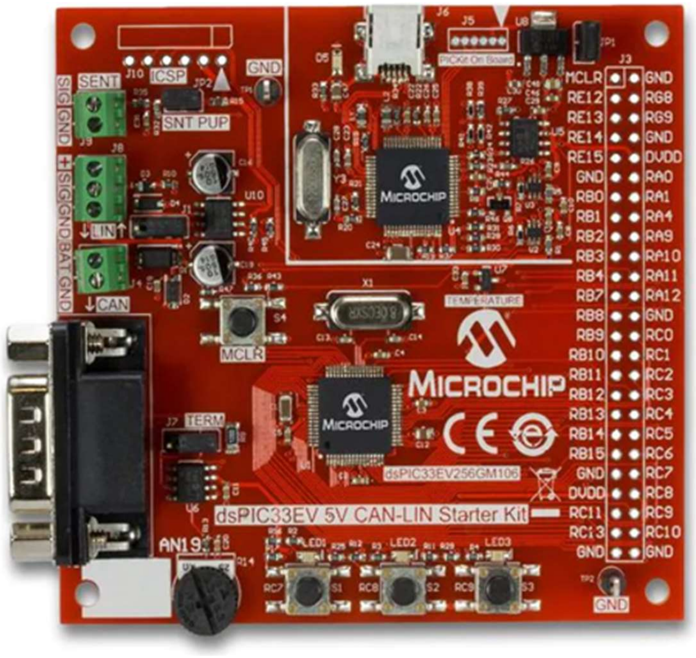

Figure 2.30: dsPIC33EV 5V CAN-LIN STARTER KIT evaluation board of the MCU used in the designed measurement setup accompanied by its main parameters [22].

Table 2.1: Main parameters of the selected MCU.

Parametric	**dsPIC33EV256GM106**
Architecture	16-bit
Max CPU Speed (MHz)	70
CPU Speed (MIPS)	70
Program Memory Size (KB)	256
SRAM (KB)	16
Pin Count	64

The MCU is programmed with MPLAB X IDE and an USB-RS232 interface is used to allow the communication between the PC and the MCU (see Fig. 2.31).

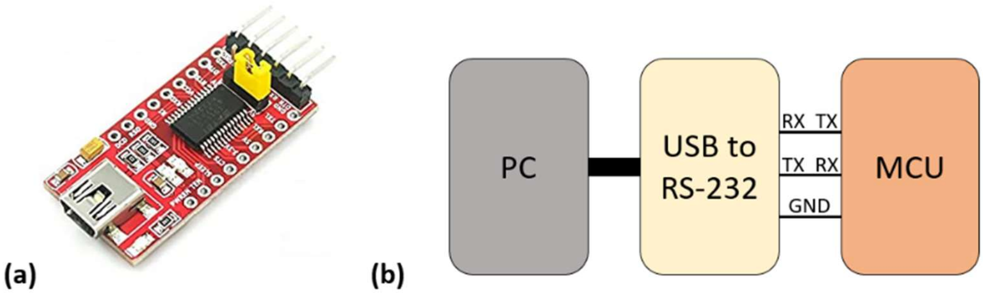

Figure 2.31: (a) USB to RS-232 interface module used to allow the communication between PC and MCU; The module is based on the FT232RL chip by FTDI [23]. (b) Simplified wiring diagram between PC, USB-RS232 interface and MCU.

The MCU is responsible for the generation of all the driving signals required for the system operation. Particularly, these signals are written sequentially on the MCU's output port to drive the corresponding switches in the circuit. Six different sequences are allowed by the MCU program. Each sequence is formed by five output port configurations that depend on the type of measurement to be performed. This can be easily selected by the user through a Graphical User Interface (GUI).

As a relevant example, in the following tables we report the sequences corresponding to High-voltage off-state stress measurement in Soft-Switching conditions:

Table 2.2: NOS ON (No-stress turn-on): This sequence contains a series of output pins configurations that govern the turn-on of the DUT during periods in which the stress is not performed; The last configuration of the sequence is kept for a time interval equal to the ON_time set by the user.

NBTI	PBTI	V_{DSC}	V_2	V_1	TRG	V_{GDRV}	V_{MC}	V_{G_Dummy}	V_{DSO}	V_{MH}	V_{ML}	V_{MLL}
0	0	0	0	1	0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	0	0	0	0	1	0
0	0	0	0	1	0	0	0	0	0	0	1	1
0	0	0	0	1	1	0	0	0	1	0	1	1
0	0	0	0	1	1	1	0	0	1	0	1	1

Table 2.3: NOS OFF (No-stress turn-off): This sequence contains a series of output pins configurations that govern the turn-off of the DUT during periods in which the stress is not performed; The NOS sequences allow to set a reference fresh value for both V_{TH} and R_{ON} parameters. The last configuration of the sequence is kept for a time interval equal to the OFF_time set by the user.

NBTI	PBTI	V_{DSC}	V_2	V_1	TRG	V_{GDRV}	V_{MC}	V_{G_Dummy}	V_{DSO}	V_{MH}	V_{ML}	V_{MLL}
0	0	0	0	1	1	0	0	0	1	0	1	1
0	0	0	0	1	0	0	0	0	0	0	1	1
0	0	0	0	1	0	0	0	0	0	0	1	0
0	0	0	0	1	0	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0	0	0

Table 2.4: ST ON (Stress with Trigger turn-on): This sequence contains a series of output pins configurations that govern the turn-on of the DUT during the actual stress-phase; In this sequence, the TRG signal is generated and the waveforms are acquired by the DSO. The last configuration of the sequence is kept for a time interval equal to the ON_time set by the user.

NBTI	PBTI	V_{DSC}	V_2	V_1	TRG	V_{GDRV}	V_{MC}	V_{G_Dummy}	V_{DSO}	V_{MH}	V_{ML}	V_{MLL}
0	0	0	0	1	0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	0	0	0	0	1	0
0	0	0	0	1	0	0	0	0	0	0	1	1
0	0	0	0	1	1	0	0	0	1	0	1	1
0	0	0	0	1	1	1	0	0	1	0	1	1

Table 2.5: ST OFF (Stress with Trigger turn-off): This sequence contains a series of output pins configurations that govern the turn-off of the DUT during the actual stress-phase; In this sequence, the TRG signal is generated and the waveforms are acquired by the DSO. The last configuration of the sequence is kept for a time interval equal to the OFF_time set by the user.

NBTI	**PBTI**	V_{DSC}	V_2	V_1	**TRG**	V_{GDRV}	V_{MC}	V_{G_Dummy}	V_{DSO}	V_{MH}	V_{ML}	V_{MLL}
0	0	0	0	1	1	0	0	0	1	0	1	1
0	0	0	0	1	0	0	0	0	0	0	1	1
0	0	0	0	1	0	0	0	0	0	0	1	0
0	0	0	0	1	0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	0	0	0	1	0	0

Table 2.6: S ON (Stress turn-on): This sequence contains a series of output pins configurations that govern the turn-on of the DUT during the actual stress-phase; In this sequence, the TRG signal is not generated and the waveforms are not acquired by the DSO. The last configuration of the sequence is kept for a time interval equal to the ON_time set by the user.

NBTI	**PBTI**	V_{DSC}	V_2	V_1	**TRG**	V_{GDRV}	V_{MC}	V_{G_Dummy}	V_{DSO}	V_{MH}	V_{ML}	V_{MLL}
0	0	0	0	1	0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	0	0	0	0	1	0
0	0	0	0	1	0	0	0	0	0	0	1	1
0	0	0	0	1	0	0	0	0	1	0	1	1
0	0	0	0	1	0	1	0	0	1	0	1	1

Table 2.7: S OFF (Stress turn-off): This sequence contains a series of output pins configurations that govern the turn-off of the DUT during the actual stress-phase; In this sequence, the TRG signal is not generated and the waveforms are not acquired by the DSO. The last configuration of the sequence is kept for a time interval equal to the OFF_time set by the user.

NBTI	**PBTI**	V_{DSC}	V_2	V_1	**TRG**	V_{GDRV}	V_{MC}	V_{G_Dummy}	V_{DSO}	V_{MH}	V_{ML}	V_{MLL}
0	0	0	0	1	0	0	0	0	1	0	1	1
0	0	0	0	1	0	0	0	0	0	0	1	1
0	0	0	0	1	0	0	0	0	0	0	1	0
0	0	0	0	1	0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	0	0	0	0	0	0

To better understand the way in which the stress/measurement sequence is performed, in Fig. 2.32 we reported an example of waveforms generated for the High-voltage off-state stress condition described so far. Particularly, we represent the time evolution of the drain voltage (V_{DS}), Gate-driving voltage (V_{GDRV}) e trigger signal (TRG). A pre-stress phase constituted by 2 NOS periods is performed; then, the stress phase begins and 2 ST periods, followed by a single S period are considered. The 2 ST periods are then repeated in order to measure the parameters evolution and the number of S periods is doubled for allowing the logarithmic distribution of the acquisitions. The doubling of S periods is performed till a certain SMAX value. In the example reported in Fig. 2.32, NOS=2, ST=2 and S=1 are considered, but these parameters can be adjusted according to the user requirements in terms of measurement accuracy and time resolution.

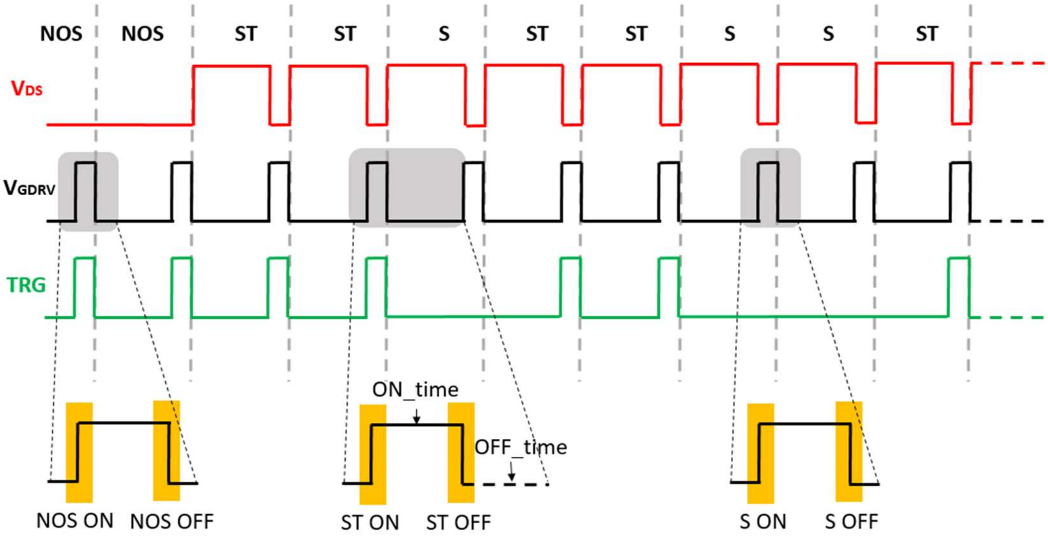

Figure 2.32: Example of waveforms generated during the measurement sequence for the High-voltage off-state stress condition.

In Fig. 2.32, we also highlighted the time window dedicated to the setting of the MCU output ports and thus to the sequence of operations to be performed in each period in order to turn ON and OFF the DUT. The sequences to be used depends on the period considered. In general, for performing the high-voltage stress measurement, the gate driving voltage and the drain voltage are pulsed at every switching cycle, but the trigger signal is generated only in correspondence to the NOS and ST periods, while it remains at low logic level during S periods.

The example reported here refers to the case in which the stress voltage is applied on the drain terminal under off-state conditions and soft-switching transitions are considered. Nevertheless, the same principle can be applied on any possible stress/measurement sequence implemented, making it possible to perform a large set of characterization with a relative simple and versatile tool.

In order to correctly perform the sequence described in Fig. 2.32, an accurate programming of the MCU was required. Particularly, a main program was developed, accompanied by several subroutines that allows to perform all the functionalities.

For sake of brevity, we do not report the corresponding code in this dissertation, but we can schematically depict the developed code through a Flow Chart Graph.

The Algorithm Flow Chart of the main program executed by the MCU is reported in Fig. 2.33.

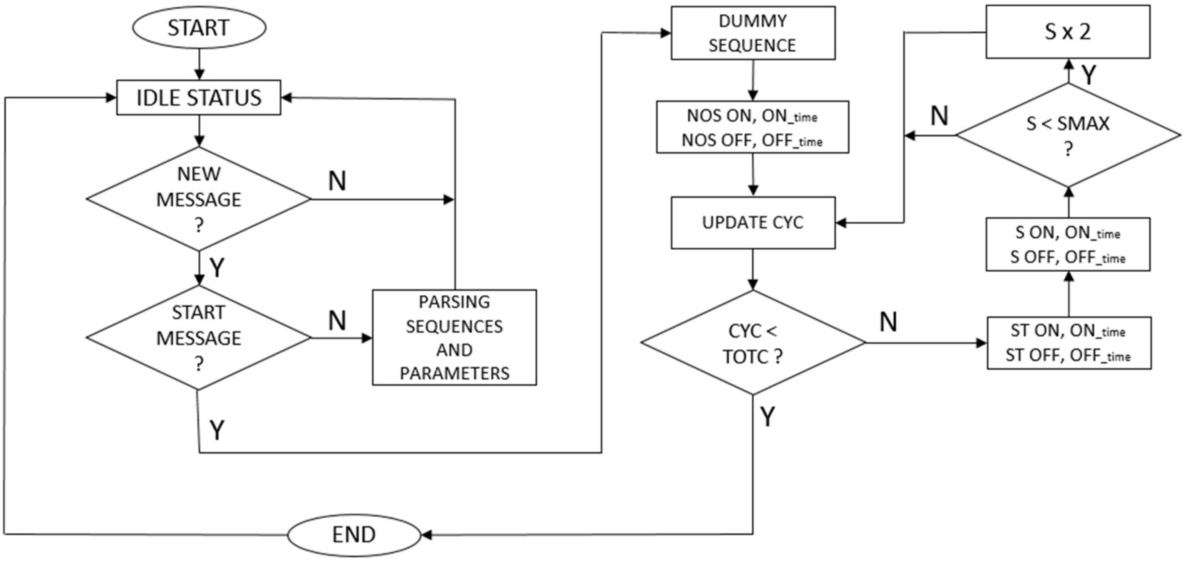

Figure 2.33: Algorithm Flow Chart representing the main program executed by the MCU

First of all, an IDLE STATUS is kept, during which all the output signals are at low logic level in order to avoid undesired configurations of the setup. In this phase, the parsing of the sequences and parameters for the measurement is performed and the MCU waits for the start command through periodical interrogation (i.e., polling). Once the start command is sent to the MCU, the program starts to execute the sequence of instructions needed for the characterization. Particularly, a first dummy sequence is performed in order to allow the warm up of the setup prior to the beginning of the actual characterization on the DUT. Immediately after this warm up phase, a sequence of no-stress cycles (NOS) is performed in order to acquire a reference fresh value for both V_{TH} and R_{ON} parameters of the DUT. After the NOS ON sequence, the on-state configuration is kept for a time interval equal to $ON_{\_time}$, after which the NOS OFF sequence is performed in order to set back the DUT to its off-state configuration lasting $OFF_{\_time}$. The number of cycles is then updated and if it is lower than the total number of cycles defined by the user, the program proceeds with the stress-phase. In the stress-phase, an ST number of ST ON and ST OFF sequences is performed, during which the stress is applied to the DUT and the DSO acquisition is triggered. After this ST number of cycles, an S number of S ON and S OFF sequences is performed, during which the stress is still applied, but the DSO is not triggered and thus the parameters of interest are not acquired in correspondence of these periods. The distinction between S and ST sequences allows the logarithmic distribution of the TRG signal over time as shown in [24]. After the S sequences, there is a control on the value of S: if S is lower than the parameter S_{MAX} set by the user, S is multiplied by 2, otherwise the last S value is kept. In both cases, the number of cycles is updated in order to count the number of stress periods applied to the DUT. When the number of periods is greater or equal to the limit imposed by the user (i.e., t_{otc}), the program ends and the output port is set back to its IDLE STATUS.

2.8.5 Graphical User Interface (GUI)

A Graphical User Interface (GUI) was developed in LabView to allow an easy and User-friendly control of the setup. A picture of the GUI is reported in Fig. 2.34.

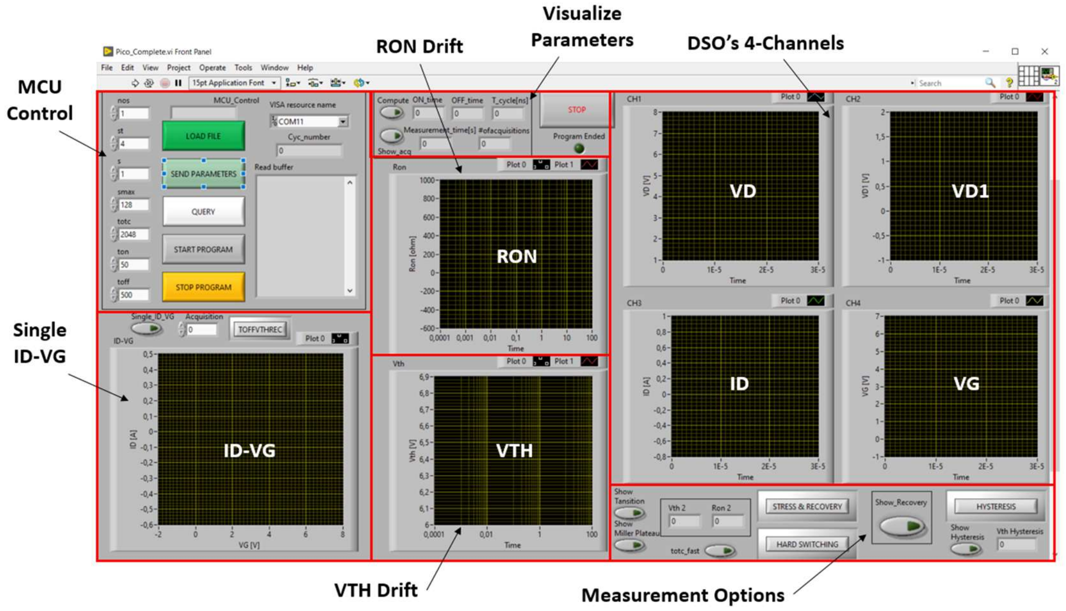

Figure 2.34: Graphical User Interface (GUI) developed in LabView.

The GUI is composed by several blocks. On the top left corner, it is possible to recognize the "MCU Control" block which is responsible for the communication between MCU and PC. The "LOAD FILE" button is used to upload the desired measurement sequence to the MCU, while the button "QWERY" allows to visualize the sequence and parameters actually stored in the MCU, by reading the strings appearing on the "Read buffer" panel. The button "START PROGRAM" allows to start the measurement while the button "STOP PROGRAM" can be used to stop the measurement before the scheduled time. On the left of this block it is possible to see a list of parameters that can be set by the user. These parameters allow to change the measurement conditions and, once set, is it possible to send the them to the MCU by pressing the "SEND PARAMETERS" button. The correspondence between the parameters set by the user and the measurement conditions (time and acquisition distribution) can be checked through the block "Visualize Parameters". Particularly, the $ON_{\_time}$ and $OFF_{\_time}$ values are defined by the parameters "t_{on}" and "t_{off}", while $T_{\_cycle}$ is defined as:

$$T\_cycle = ON\_time + OFF\_time + T\_dead \tag{2.2}$$

where $T_{\_dead}$ is the time required for writing the signals to the MCU output port and completing the sequence of states for switching between ON-OFF condition and vice versa. Particularly, it has been verified that a single writing operation on the output port requires 30 ns to be performed. Moreover, a series of null operations (NOP) can be inserted on purpose between consecutive writing operations in order to guarantee the dead time for the switches to be driven. According to the MCU frequency (i.e., 70 MHz) each NOP requires 14.286 ns to be executed. During each turn-on (or turn-off) phase, there are 5 configurations to be written on the output port that are interleaved by 4 blocks of null operations (#NOP). Accordingly, for each cycle, there are 8 blocks of #NOP and 10 writing performed. This traduces into:

$$T\_dead = (14.286ns \times \#NOP) \times 8 + (30ns \times 10) \tag{2.3}$$

Concerning the definition of $ON_{\_time}$, a FOR loop containing a single null operation has been used. Particularly, the FOR loop is executed a number of times equal to the "t_{on}" defined by the user. The same approach has been employed for the $OFF_{\_time}$ definition, by tuning the parameter "t_{off}". It has been verified that, for the chosen MCU, the FOR loop requires 9 assembly operations (each one taking 14.286 ns) to be performed. Accordingly, the $ON_{\_time}$ and $OFF_{\_time}$ are defined as:

$$ON\_time = 14.286ns \times (9+1) \times t_{on} \tag{2.4}$$

$$OFF\_time = 14.286ns \times (9+1) \times t_{off} \tag{2.5}$$

On the other hand, the Measurement time is defined by the parameter "t_{otc}" and it sets the cumulative stress time (i.e., $T_{\_cycle}$ multiplied by the total number of cycles). Concerning the number and the distribution of the acquisitions over time, they are defined by the remaining parameters (S, ST and S_{MAX}). The impact of the parameters set on the acquisitions distribution can be easily verified by the user through the buttons "Compute" and "Show_acq". It is important to notice that, in general, an increase in ST yields a higher resolution at the beginning of the stress (i.e., for short stress time), at the cost of an increased number of acquisitions. To get rid of this, the S_{MAX} parameter can be increased, allowing a sparser acquisition for long stress times.

The waveforms acquired by the oscilloscope channels can be visualized on the panel on the top right corner. On the other hand, the I_D-V_{GS} characteristics can be visualized in the bottom left corner and, through the corresponding selector, it is possible to visualize the I_D-V_{GS} reconstructed for each acquisition. If required, it is also possible to check the DUT's status by acquiring a single I_D-V_{GS} curve by pressing the button "Single_I_D_V_G".

Below the “Visualize Parameters” Block, the GUI shows two distinct blocks for visualizing the R_{ON} and V_{TH} parameters evolution over time. Particularly, for each acquisition, the R_{ON} parameter is computed as the ratio between V_{DS} and I_D values averaged over several samples captured during the stable part of the V_{GS} ramp, while V_{TH} is extracted through the extrapolation in the linear regime method [25].

In the bottom right corner, we can find some interesting features, like the possibility to monitor the V_{TH} and R_{ON} recovery after the stress removal by pressing the button “STRESS&RECOVERY” or activating the button “HARD SWITCHING” for the corresponding operative mode. It is also possible to evaluate the parameters hysteresis by applying a sequence of two consecutive gate ramps in the on state time interval, thus extracting twice per cycle the parameter of interest through the “HYSTERESIS” button.

2.8.6 Whole Setup

All the parts described so far are connected together and the overall system is reported in Fig. 2.35. Particularly, a Laptop is used to control the whole system and elaborate the signals acquired by the DSO. In order to connect the system to the Laptop, three USB connections are required:

- The first USB cable connects the Laptop to the DSO which stores the signals measured;
- The second USB cable connects the Laptop to the MCU in order to supply it and to allow the programming;
- The third USB cable connects the Laptop to the USB-RS232 module which allows the communication between LabView and the MCU.

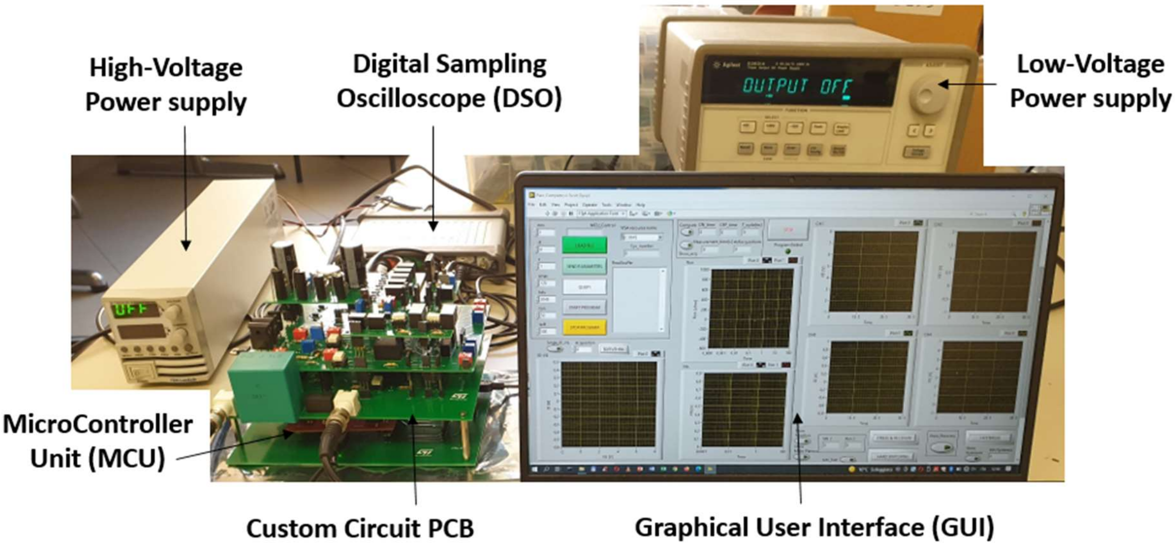

Figure 2.35: Picture reporting all the system parts with the Graphical User Interface (GUI) developed in LabView for controlling the whole setup.

2.8.7 *Procedure for Waveforms Setup*

The procedure for the waveforms setup is typically performed without DUT connected and is extremely useful for visualizing the signals applied during the measurement and to eventually modify the measurement waveforms by acting on the corresponding components in the circuit.

The procedure is composed of several steps which are briefly described in the following.

- Upload the program on the MCU through the MPLAB X IDE tool;
- Open the “Picoscope 6” software;
- In the “Picoscope 6” software, enable the four channels with the corresponding probe attenuation and modify the voltage range according to the signals expected for each channel. Typical values: 1 kV for ChA, 5 V for ChB, 5 V for Ch C and 20 V for ChD;
- Change the time scale according to the measurement specifications;
- Change the bit resolution to 14-bit (maximum allowed with four channels DSO);
- Set the Trigger to “Auto” and select ChD as Trigger source;
- Set the trigger level between the low and the high voltage levels of the V_G signal;
- Keep the “Picoscope 6” software opened to visualize the waveforms in real time;
- Open the LabView VI “Set Waveforms”;
- Select the COM port corresponding to the MCU to allow the communication with PC;
- Launch the VI, by pressing the arrow in the top left corner of the VI;
- Press the Button “QUERY” to verify the communication between PC and MCU;
- Select the measurement sequence by pressing the Button “Load File”;
- Set the parameters for the measurement in the MCU Control panel and press the Button “SEND PARAMETERS”;
- Enable the outputs of the low voltage and high voltage power supply;
- Press the Button “START PROGRAM”;
- Visualize the waveforms on the “Picoscope 6” software (see Fig. 2.36) and eventually modify the voltage values by acting on the circuit. Once the waveforms have been correctly set, press the Button “STOP PROGRAM”;
- Disable the outputs of the high voltage and low voltage power supply;
- Close the “Picoscope 6” software.

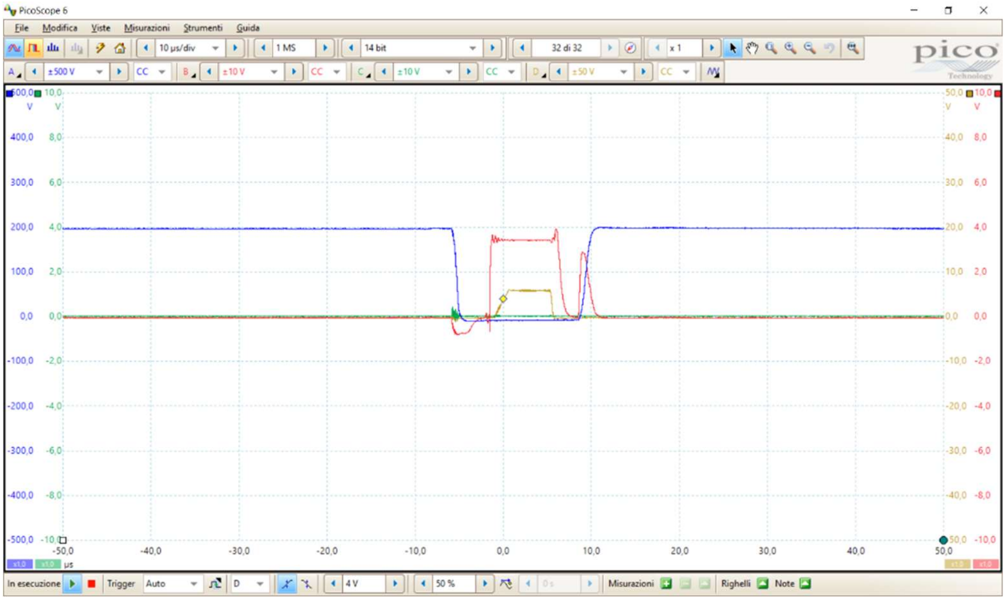

Figure 2.36: Picture of the "Picoscope6" program that is used to check/set the waveforms for the measurement

During the Waveforms Setup Procedure, the voltage levels can be adjusted by acting on the switches/trimmers highlighted in Fig. 2.36. The V_{PL} level provided in on state can be varied through the corresponding trimmer, whereas the series resistance for limiting the drain current can be changed by different combinations of the "R_{series} value" switches. In case of Hard-Switching mode operation, it is possible to connect the desired gate resistance R_G through the corresponding connector and to select the current limiting branch via the SS/HS selector. The "I_{limit} level" trimmer allows to change the limiting current at which the transitions are led.

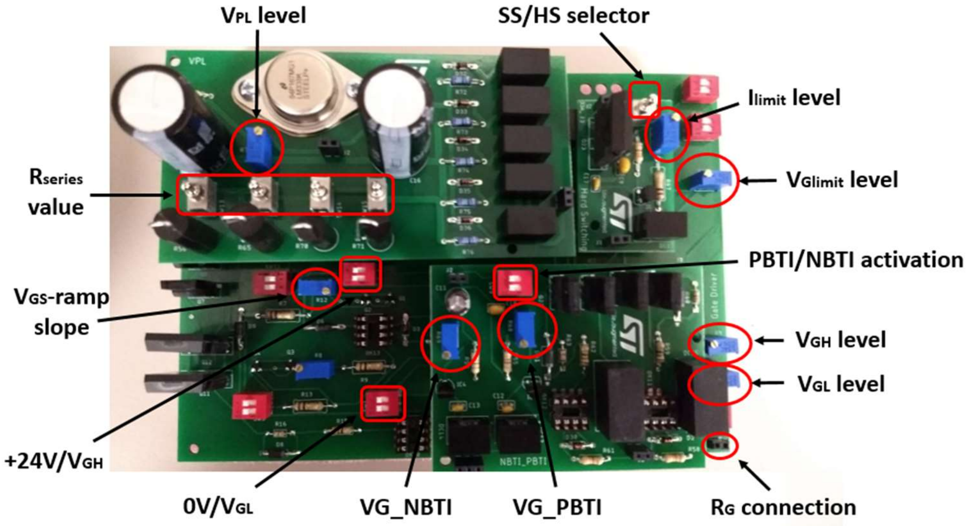

Figure 2.37: Highlight of trimmer and switches on which the user can act to change the waveforms for the measurement

2.8.8 Procedure for Measurement

The procedure for performing a generic measurement is briefly described in the following.

- Upload the program on the MCU through the MPLAB X IDE tool;
- Open the LabView VI “Pico Complete” containing the GUI for controlling the Setup;
- Select the COM port corresponding to the MCU;
- Launch the VI, by pressing the arrow in the top left corner of the VI;
- Press the Button “QUERY” to verify the communication between PC and MCU;
- Select the measurement sequence for the stress by pressing the Button “Load File”;
- To perform both stress and recovery, press the button “STRESS & RECOVERY” to activate the recovery monitoring and select the measurement sequence for the recovery phase by pressing the Button “LOAD FILE”;
- Set the parameters for the measurement in the MCU Control panel and press the Button “SEND PARAMETERS”;
- Connect the DUT to the Setup;
- Enable the outputs of the low voltage and high voltage power supply;
- Press the Button “START PROGRAM”;
- Once the measurement has been performed and the results are displayed on the monitor, press the Button “STOP” to stop the VI execution;
- Disable the outputs of the high voltage and low voltage power supply;
- Disconnect the DUT from the Setup.

2.9 Conclusions

A novel measurement setup for the characterization of V_{TH} and R_{ON} drifts in packaged power devices has been successfully developed. The main novelties introduced by the system are the programming of the MCU to provide a logarithmic control of the trigger signal and the usage of a custom gate driver circuit. The former allows to monitor the parameters evolution over several time decades without saturating the DSO memory while preserving time accuracy. The latter guarantees the generation of a fast gate driving voltage that allows a fast extraction of the device I_D-V_{GS} characteristics even in case of packaged DUTs presenting large gate-source capacitances. Moreover, the designed system presents the advantage of being extremely versatile, since it allows to choose the type of characterization and the measurements conditions without having to change equipment. In fact, the measurement conditions can be totally defined by the user from the GUI developed in LabView. Moreover, the implementation of the system on several boards allows an easy scalability of the setup. In fact, it is possible to modify just a few parts of the system to implement additional functionalities and/or to insert other boards to extend its capabilities. The system, as it is, already provide a powerful tool for the characterization of packaged power devices and it enables an accurate study of the V_{TH} and R_{ON} stability in state of the art SiC and GaN devices.

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3 V_{TH} and R_{ON} Drifts in Packaged SiC MOSFETs

In this chapter, we present the experimental results concerning the characterization of V_{TH} and R_{ON} drifts in packaged SiC MOSFETs. To this end, the custom measurement setup presented in Chapter 2 has been employed. After a preliminary introduction on the most important issue related to V_{TH} and R_{ON} instabilities, we present the results obtained under several measurement conditions, accompanied by the interpretations proposed to explain the observed phenomena.

3.1 Instabilities in SiC power MOSFETs

As already mentioned, Silicon Carbide (SiC) is a common technology option for replacing silicon in power-switching applications that require low switching and conduction losses [1]. Unfortunately, the degradation of key electrical parameters in SiC power devices under repetitive switching stress reduces both device performance and reliability well below specifications [2]. In this scenario, stability issues like threshold voltage (V_{TH}) and dynamic on-resistance (R_{ON}) drifts are often encountered [3], severely impacting device lifetime and performance. For instance, a positive R_{ON} drift (i.e., R_{ON} increase) affects the conduction losses within power-switching converters, yielding a considerable efficiency reduction. Similarly, a positive V_{TH} shift results in a lower current level for a given driving gate voltage (V_{GS}) [4, 5], whereas negative V_{TH} variations could impede fully turning off the device, causing unwanted conduction at a large drain bias [6].

Generally, Bias Temperature Instability (BTI) experiments are employed to reveal the mechanisms underlying these issues in SiC technology [7-9]. However, BTI tests can only be used to investigate the effects related to gate bias, neglecting the effects related to the potential applied on the drain. To get a more complete picture of the detrimental effects produced by repetitive switching stress [2-10], it is necessary to evaluate the V_{TH} and R_{ON} evolution when the device is driven in realistic operating conditions, i.e., with both gate and drain potential repeatedly switched. To this end, test circuits should be designed to mimic conventional switching conditions in terms of frequency, voltage, and current level. At the same time, these circuits should also extract the parameters of interest (e.g., V_{TH} and R_{ON}) without affecting device operation. Accordingly, a fast stress measurement approach is needed, in order to cope with switching frequencies in the kHz range [11] and also to limit the delay between the stress and readout [8, 12, 13] phases, thus avoiding ambiguous parameter drifts and/or wrong data interpretation. Nevertheless, achieving these goals is challenging for conventional parameter analyzers, especially when characterizing packaged devices with large parasitic capacitances [14]. The development of custom, ad-hoc, systems is thus essential to investigate the stability and performance of commercially available state-of-the-art devices: For this reason, the novel measurement setup presented in this thesis represents a powerful tool to perform the studies necessary to investigate the devices' performances under switch-mode operations.

3.2 V_{TH} and R_{ON} instability in Switching Mode Operation

The first important test to be performed, concerns the evaluation of V_{TH} and R_{ON} dynamic evolution under soft-switching mode operation. To this end, measurement is carried out by means of the double-pulsed on-the-fly (OTF) characterization described in Chapter 2, in which the Device Under Test (DUT) is repeatedly switched between a high voltage off-state condition and a low voltage on-state one in the kHz frequency range. By applying the proposed measurement method on commercially available devices (i.e., TO-247 vertical SiC MOSFETs), it was possible to test the effectiveness of the setup and to provide a qualitative interpretation of the physical mechanisms leading to the observed V_{TH} and R_{ON} drifts. Particularly, devices from two different vendors were characterized, namely Type-A (1200V/520mΩ) and Type-B (650V/120mΩ), for which different phenomena were observed.

The reduced schematic of the custom measurement setup is shown in Figure 3.1.

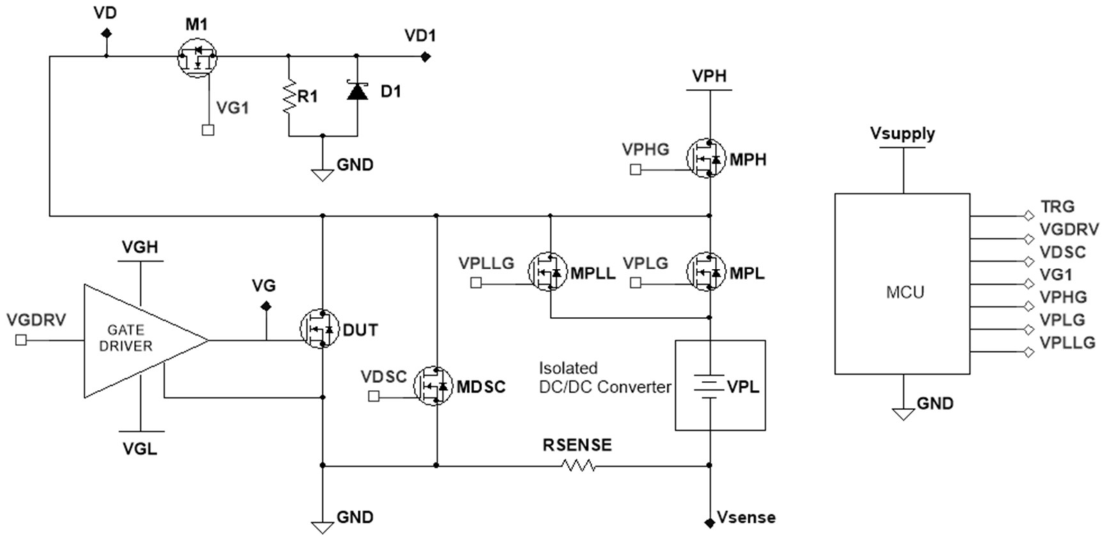

Figure 3.1: Setup schematic. The whole setup is controlled by an MCU used for triggering the DSO acquisition with logarithmic time steps and generating the necessary synchronization signals.

The gate driver circuit is responsible for repeatedly switching the DUT ON and OFF and is devoted to the generation of the ramp signal required for the extraction of the V_{TH} and R_{ON} values [15]. In off-state conditions, the DUT is stressed with a large drain voltage (V_{PH}), provided by a DC power supply, while the on-state drain bias voltage (V_{PL}) is provided through an isolated DC/DC converter as described in Chapter 2. The drain voltage is pulsed by means of a couple of NMOS (M_{PH} and M_{PL} in Figure 1) arranged in a push-pull configuration, with an additional NMOS device (M_{PLL}) inserted for reducing the series resistance during DUT turn on. A 0.1 Ω resistor (R_{SENSE}) is connected to the DUT's source terminal in order to extract the drain current (I_{DS}) while a clamping circuit (M_1, R_1, D_1) is connected to the drain terminal of the DUT for improving the measurement accuracy at low voltages. An additional NMOS (M_{DSC}) was placed between the DUT's drain terminal and GND in order to force the drain voltage to 0 V. This condition is required for monitoring the parameters recovery after the V_{PH} removal. The whole setup is controlled by an MCU used for triggering the DSO acquisition with logarithmically-spaced time steps [16] and for generating the necessary synchronization signals. Figure 3.2 illustrates a typical waveforms obtained in the circuit.

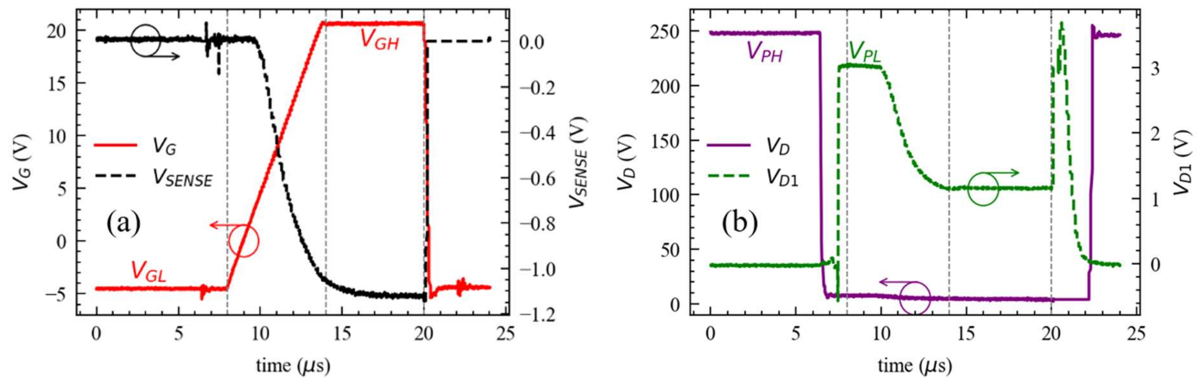

Figure 3.2: (a) Gate voltage (V_G) is swept for extracting V_{TH} and a stable 20 V level is held at the end of the ramp to ensure a stable current and voltage level for a correct R_{ON} extraction. (b) V_D is monitored during the off-state stress phase, while V_{D1} is the signal provided by the clamping circuit (M_1, R_1, D_1).

Measurements were carried out with a 120 μs switching period and 10% Duty Cycle, i.e., by applying a gate bias rising from -5 V to 20 V in 6 μs, and staying at 20 V for further 6 μs during the low-(drain)-voltage on-state time interval (see Figure 3.2(a)). In off-state conditions, a V_{PH} stress voltage is applied to the DUT whereas in on-state V_{PL} is set to 3 V (see Figure 3.2(b)). V_{GL} is typically set to -5 V in order to prevent false turn-on and ensure safe operation against voltage spikes on the gate [6]. During the 6 μs rising ramp, the I_{DS}-V_{GS} characteristic is reconstructed, allowing the extraction of the device V_{TH} using the extrapolation in the linear regime method [7]. To perform a correct R_{ON} extraction, at the end of the gate ramp a stable V_{GH} level is held for 6 μs to compute R_{ON} as the ratio between the measured V_{D1} and I_{DS} averaged over the 6 μs range. A sequence of no-stress acquisitions (i.e., V_{PH}=0 V) is performed on fresh devices at the beginning of each characterization and the corresponding I_{DS}-V_{DS} curves were acquired to set a reference value (V_{TH0} and R_{ON0}) from which the relative drifts are evaluated. Then, the parameters evolution is monitored for 1000 s. ΔV_{TH} is simply calculated as ($V_{TH} - V_{TH0}$), whereas the acquired R_{ON} values are normalized with respect to R_{ON0}.

3.2.1 V_{GH} and V_{PH} effects on V_{TH} and R_{ON} Drifts (Type-A)

We firstly considered device Type-A. To get a complete picture of the device behavior, it is important to know the influence of the measurement conditions on the parameters drifts. To this end, the effects associated to (i) the gate-driving voltage provided in on-state (V_{GH}) and (ii) off-state drain voltage (V_{PH}) were investigated. With the aim to pursue a deeper investigation, after 1000 s stress an additional 1000 s measurement phase was inserted for monitoring the parameters recovery after the V_{PH} removal. During this additional phase, the V_{PH} bias is no longer applied to the DUT and the drain voltage in the off-state condition is set to 0 V. On the other hand, the same gate ramp (V_{GL}; V_{GH}) and low drain voltage (V_{PL}) are provided to the DUT for extracting V_{TH} and measure R_{ON} in triode region.

To highlight the V_{GH} effect on the observed drifts, the characterization was performed by ramping the gate voltage from -5 V to three different V_{GH} levels (15 V, 17.5 V and 20 V), whereas the V_{PH} voltage was fixed to 100 V. The results obtained for the V_{TH} and R_{ON} parameters are shown in Figure 3 and Figure 4, respectively.

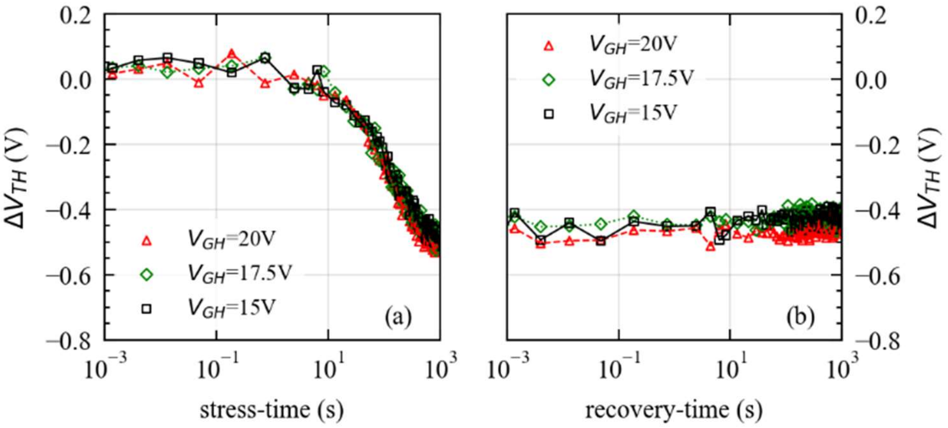

Figure 3.3: (a) Effect of gate voltage level (V_{GH}) on the V_{TH} drift during the stress with V_{PH} = 100 V. (b) Monitored V_{TH} recovery at different V_{GH} levels (15 V, 17.5 V and 20 V) with V_{PH} = 100 V.

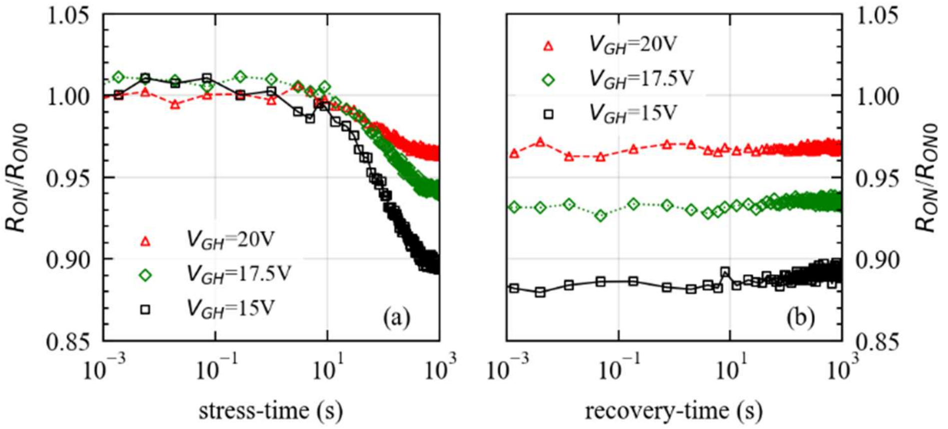

Figure 3.4: (a) Effect of gate voltage level (V_{GH}) on the R_{ON} drift during stress with V_{PH} = 100 V. (b) Monitored R_{ON} recovery at different V_{GH} levels (15 V, 17.5 V and 20 V) with V_{PH} = 100 V.

The transients capture during the stress time for both V_{TH} and R_{ON} present similar time constants, suggesting a possible correlation between the two phenomena. Particularly, the observed negative V_{TH} drift should lead to an increase of the device conductivity (at a fixed driving V_{GH}), thus yielding an R_{ON} reduction. The observed R_{ON} transients (Figure 3.4(a)) could thus be directly correlated to the V_{TH} ones (Figure 3.3(a)), indicating the presence of a single underlying mechanism. Particularly, these negative drifts could be potentially explained by the presence of traps at the SiC/SiO_2 interface [17] and the long transients observed could be signature of charge emission dynamics.

However, a different V_{GH} effect was observed for V_{TH} and R_{ON} transients during the stress phase. As shown in Figure 3.3(a), the V_{TH} transients are not affected by the applied V_{GH}, while a reduction in the R_{ON} drift is observed for higher V_{GH}. This can be ascribed to the fact that, at higher V_{GH}, the device transconductance (g_m) degrades [18], yielding a negligible impact of the overdrive voltage (i.e., $V_{GS}-V_{TH}$) variations on the device current and, consequently, on R_{ON}. On the other hand, at lower V_{GH}, variations in the V_{TH} affect the device current (i.e., R_{ON}), due to a less degraded g_m [18]. Accordingly, the R_{ON} variation increases with decreasing V_{GH} from 20 V to 15 V (see in Figure 3.4(a)) even though the associated V_{TH} transients present negligible differences (i.e., the V_{TH} drift is the same). Concerning the recovery phase (see Figure 3.3(b) and 3.4(b)), both V_{TH} and R_{ON} drifts are unrecoverable in the considered time interval (i.e., 1000 s), independently on the applied V_{GH} level. This observation can be explained by the fact that the applied V_{PH} stress (i.e., 100 V) does not affect the parameters drift, and the observed instabilities can be totally ascribed to the gate switching applied during the OTF measurement. In fact, it is important to notice that the monitoring of the device parameters in the recovery phase requires the gate voltage to be repeatedly switched from negative to positive and vice-versa. As a consequence, the corresponding stress cannot be removed.

This hypothesis is consistent with the vertical structure presented by tested devices. In fact, the influence of the drain voltage on interface states is limited by the physical distance between the oxide and the drain contact, while the gate bias plays a major role on the V_{TH} stability [7, 8]. However, the drain voltage applied in off-state could be significantly higher than 100 V during typical device operation, thus the complete absence of drain-induced instabilities cannot be ruled out.

We thus investigated the V_{TH} and R_{ON} drifts at higher stress voltages (V_{PH}). To this end, it is important to keep constant the driving V_{GL} and V_{GH} in order to discern the gate/drain contributions. Accordingly, a gate voltage between -5 V and 15 V was applied to the DUT, while three different V_{PH} levels were considered (100 V, 250 V and 500 V).

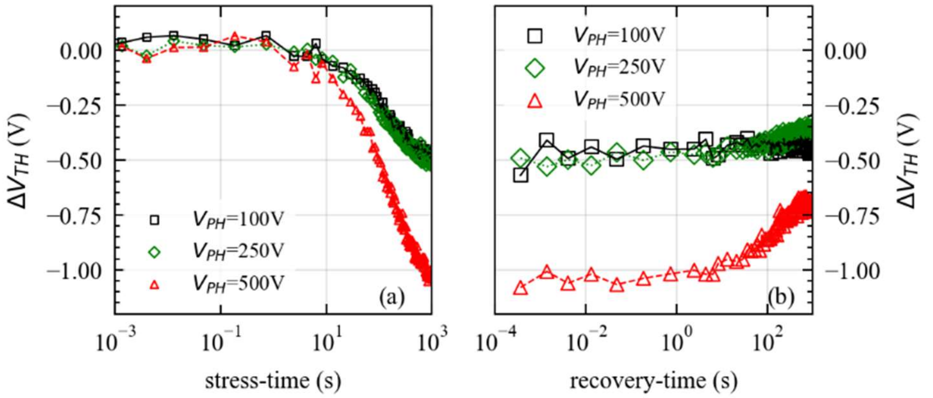

Figure 3.5: (a) Effect of drain off-state stress voltage (100 V, 250 V and 500 V) on the V_{TH} drift during the stress with V_{GH} =15 V. (b) Monitored V_{TH} recovery at different drain stress voltages.

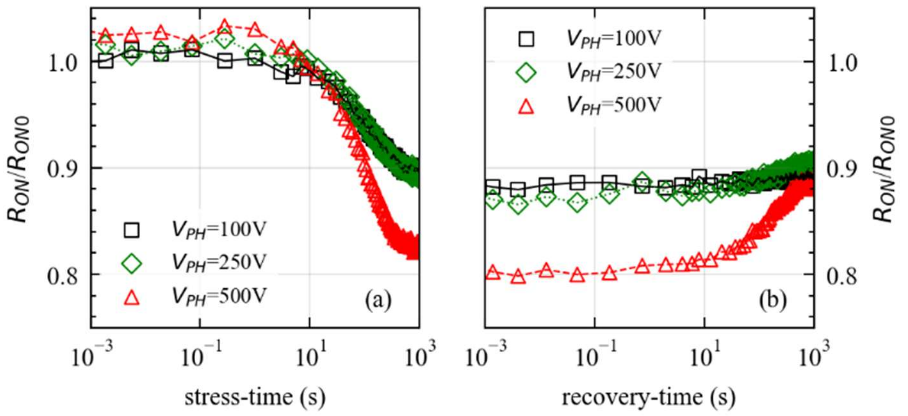

Figure 3.6: (a) Effect of drain off-state stress voltage on the R_{ON} drift during the stress with V_{GH} = 15V. (b) Monitored R_{ON} recovery at different drain stress voltages (100 V, 250 V and 500 V) with V_{GH} = 15 V.

The negative V_{TH} shift observed at V_{PH} = 500 V is stronger with respect to that measured at lower V_{PH} (Fig. 5(a)). At the same time, the R_{ON} drift clearly changes from -10% to -17% while passing from 250 V to 500 V, showing the same V_{PH} dependence observed on V_{TH} (compare Figure 3.5(a) and Figure 3.6(a)). The fact that similar trends were observed on both V_{TH} and R_{ON} degradation confirms that the observed instabilities share the same origin. Particularly, the R_{ON} drift is a direct consequence of the V_{TH} one, since at V_{GH} = 15 V the less degraded g_m [18] makes the device current (i.e., R_{ON}) highly sensitive on the overdrive voltage (i.e., V_{GH}-V_{TH}). Accordingly, the significant impact of the drain stress voltage observed on V_{TH}, yields an additional R_{ON} drift at V_{PH} = 500 V, whereas a negligible effect is observed at 100 V and 250 V. A further evidence of the V_{PH} role is given by the partial recovery observed after 500 V stress. Almost no-recovery was observed after the stress performed at 100 V and 250 V, whereas the recovery transients appears for both R_{ON} and V_{TH} at 500 V. In fact, after the V_{PH}

removal, the drain induced instabilities can be recovered, whereas the gate-induced ones are still present, yielding a residual drift in V_{TH} and R_{ON}. Accordingly, the recovery monitoring can be used to isolate the drain-induced instabilities from the gate-related ones, whereas the effect of the gate driving voltage can be observed by reducing (or potentially by removing) V_{PH}.

3.2.2 V_{TH} and R_{ON} Slow/Fast Drifts (Type-B)

The designed system was then used for characterizing Type-B devices and the measurement conditions were modified in order to investigate also fast gate-effects on V_{TH} and R_{ON}. To this end, a double-ramp gate signal was applied in on-state to extract the parameters of interest twice per cycle (see Fig. 3.7), being able to capture fast hysteresis effects and gate-induced instabilities. Moreover, the R_{ON} and V_{TH} evolution was still monitored over a 100µs-1000s time range, in order to appreciate their complete dynamics. The drain terminal was pulsed between a high stress voltage V_{PH} (off-state) and a low voltage V_{PL} (on-state) as discussed in Section 2, and the DUT was driven with a 120 µs switching period (T_S) and 18 µs T_{ON}.

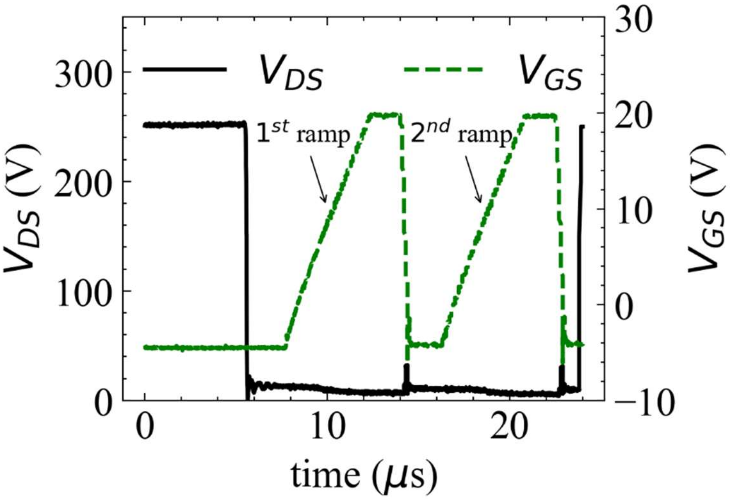

Figure 3.7: Waveforms corresponding to V_{GS} (dashed-blue) and V_{DS} (solid-black) signals used for the stress/measurement. DUTs are safely turned off with V_{GS}= -5 V and after each 4 µs ramp used for measuring V_{TH}, a stable 20 V level is held (2 µs) for R_{ON} extraction.

In order to investigate the fast gate effects, we compared the fresh I_{DS}-V_{GS} characteristics acquired with the two ramp signals before starting the stress phase (i.e., V_{DS} is maintained at V_{PL}). As we can see in Fig. 3.8(a), a single ramp of V_{GS} was sufficient for positively shift V_{TH}, as highlighted by the data acquired during the 2nd ramp.

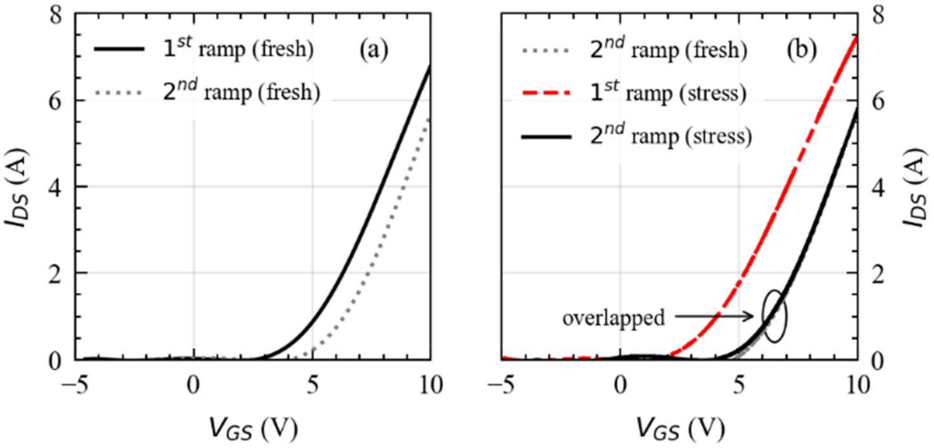

Figure 3.8: (a) I_{DS}-V_{GS} extracted on fresh device with 1st and 2nd ramp. (b) Comparison between I_{DS}-V_{GS} acquired after the first stress period (100 µs at V_{PH}=250 V) with the double-ramp signal and the (fresh) I_{DS}-V_{GS} acquired with the 2nd ramp.

This effect can be ascribed to the tunneling of electrons into oxide traps [19] and is not recoverable in the subsequent short off-state interval preceding the 2nd ramp, due to the slow nature of the emission process. On the other hand, the opposite V_{TH} shift was observed during the stress phase, as highlighted by the drain-induced hysteresis shown in Figure 3.8(b). In fact, the first 100 µs stress at V_{PH}=250 V induces a significant negative V_{TH} shift, which is observed during the 1st ramp. Interestingly, V_{TH} fully recovers during the 2nd ramp whom yields overlapped results with those of the fresh 2nd ramp measurement. The mechanism governing this drift was induced by the drain stress voltage applied in off-state (V_{PH}). We thus analysed this fast V_{TH} drift at several V_{PH} levels, reporting in Figure 3.9 the ΔV_{TH} obtained with the 1st and with the 2nd gate ramp.

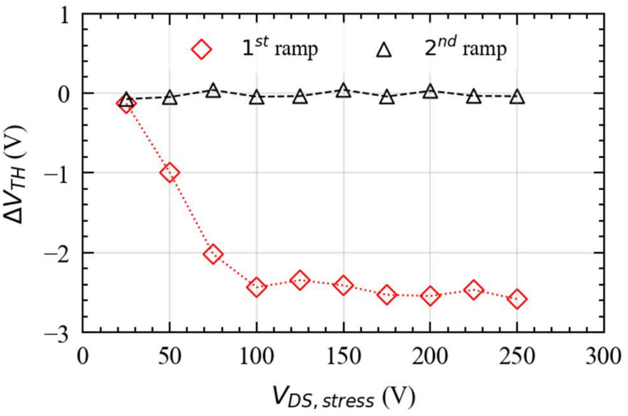

Figure 3.9: Comparison between the fast V_{TH} shift (experimented after 100 µs stress) measured with the 1st ramp and with the 2nd ramp applying different off-state stress voltages (V_{PH} from 25 V to 250 V).

The V_{TH} shift measured with the 1st ramp increases rapidly up to V_{PH}=100 V and then saturates for higher V_{PH}. Said shift is not present during the 2nd ramp for the investigated V_{PH} range (see Figure 3.9). The observed V_{TH} drift is clearly a fast phenomenon which onsets with a single 100 µs off-state stress and recovers during the 1st V_{GS} ramp from -5 V to 20 V during on-state. Moreover, the observed V_{PH} dependence suggests that it might be related to field enhanced charge/discharge trapping phenomena beneath the gate contact.

For long stress times (> 10 s), a negative V_{TH} drift appears for both ramps. By removing the V_{TH} offset induced by the fast drift on 1st ramp data, the slow drifts measured with both ramps are nicely overlapped (see Figure 3.10), suggesting that said slow phenomenon is affecting equally both of them.

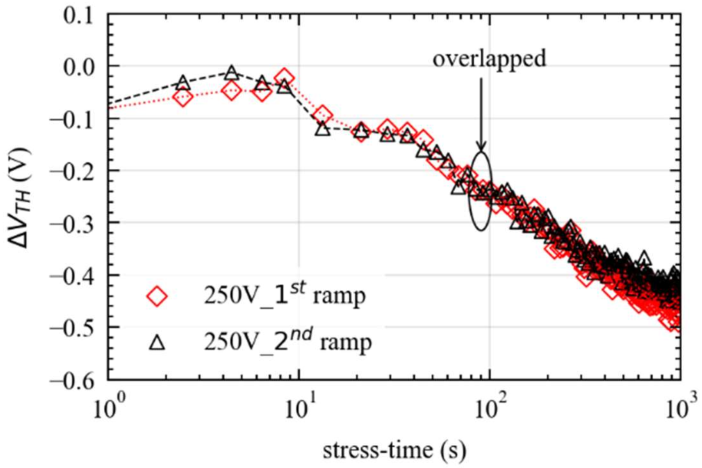

Figure 3.10. ΔV_{TH} transients measured for long stress times with V_{PH}=250 V. The negative drift associated to the fast hysteresis effect has been removed from the data provided by the 1st ramp in order to compare the slow transient with the one captured by the 2nd ramp.

Concerning R_{ON}, the values extracted with both ramps present negligible differences, suggesting that the fast V_{TH} drift phenomenon does not significantly affect this parameter. In fact, R_{ON} remains stable up to 10 s and then, similarly to the slow drift of V_{TH}, experiences a 3% increase within the 10 s to 1000 s stress-time range, as reported in Figure 3.11. Two opposite slow trends were thus observed for V_{TH} and R_{ON}, which somehow make it not straightforward to explain their origin. Nevertheless, by comparing the transients observed in the 1s-1000s time range (see Figure 3.12), we noticed that R_{ON} and V_{TH} slow drifts present similar time constants, suggesting a possible correlation between the two mechanisms.

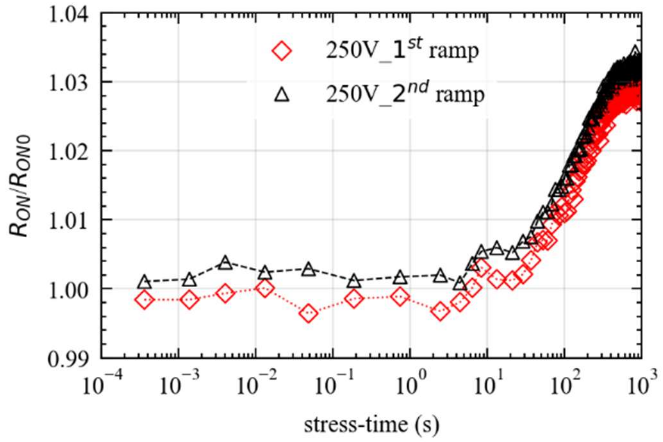

Figure 3.11: R_{ON} transients measured during the stress phase (V_{PH}=250 V) with 1st ramp and 2nd ramp. Data are normalized with respect to the fresh R_{ON} value extracted before the stress. A 3% R_{ON} increase has been observed after 1000 s stress at V_{PH}=250 V.

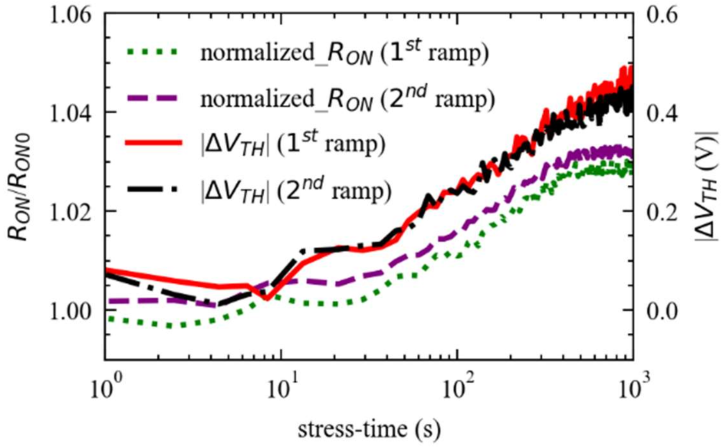

Figure 3.12: Comparison between the R_{ON} transients and the absolute $|\Delta V_{TH}|$ transients acquired with 1st ramp and 2nd ramp for long stress times (> 1 s) with V_{PH}=250 V. Measured transients present similar time constants suggesting a correlation between R_{ON} and V_{TH} slow drifts.

With this in mind, both drifts could be explained by device self-heating reducing the carriers' mobility (i.e., increase R_{ON}) and negatively shifting V_{TH} due to fewer negatively-charged interface traps [17].

In order to highlight the role of device self-heating (SHE) on the parameters drifts, we should change the average power dissipation (P_D) experimented by the DUT during the characterization. In fact, if SHE plays any role in affecting the parameters stability, by changing P_D, we should observe a significant variation in the experimented R_{ON} and V_{TH} drifts [20].

Accordingly, measurements were performed for either i) different Duty Cycles (i.e., different T_{ON} at constant T_{OFF}) and ii) several on-state current levels (I_{DS}).

To prevent misleading results, we removed the off-state stress voltage (i.e., V_{DS} is maintained at V_{PL}), so that the observed R_{ON} and V_{TH} instabilities can be totally ascribed to the gate biasing and to the conduction-related effects. Moreover, since the information captured by the 1st and 2nd ramp for long stress times (i.e., in the 1s-1000s range) were proven to be identical, we removed the 2nd gate ramp to have a finer control on T_{ON} (i.e., on P_D).

The gate signals used in this phase are sketched in Figure 3.13(a), in which we reported the different T_{ON} values explored. On the other hand, the I_{DS} effect was investigated according to the I_{DS}-V_{GS} characteristics shown in Fig. 3.13(b).

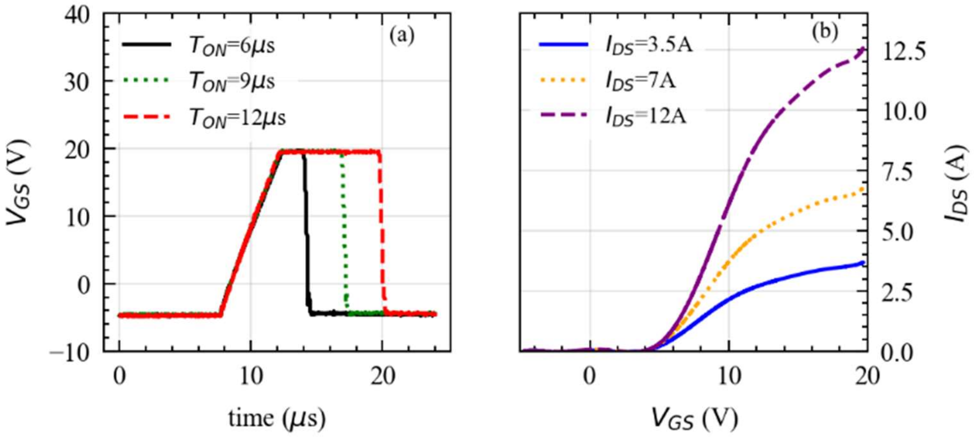

Figure 3.13: (a) V_{GS} waveforms corresponding to three different on-state time intervals (6 μs , 9 μs and 12 μs). (b) I_{DS}-V_{GS} acquired with different V_{PL} levels yield different current levels in triode region.

The trends observed in Figure 3.14 seem to confirm our hypothesis. In fact, by increasing T_{ON} (i.e., increasing DC), the average P_D increases as well, rising the temperature in the device active region. Accordingly, a larger drift is observed on both V_{TH} and R_{ON} while passing from T_{ON}=6 μs to T_{ON}=12 μs.

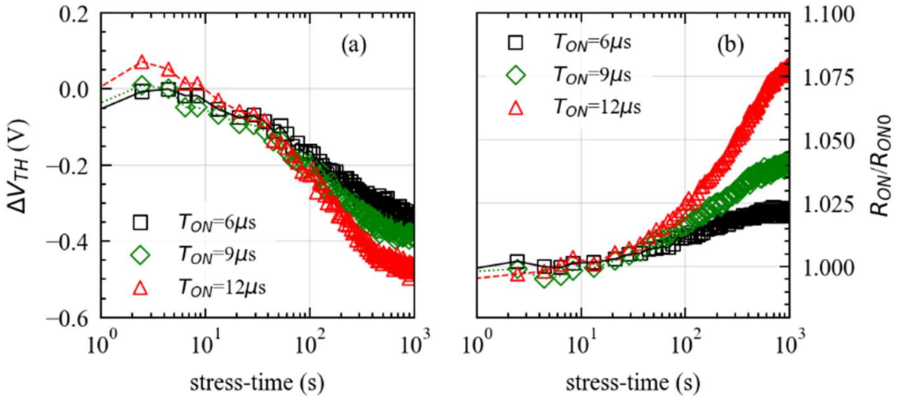

Figure 3.14: (a) Effect of on-state time interval (T_{ON}) on V_{TH}. (b) Effect of on-state time interval (T_{ON}) on R_{ON}.

In order to explore case (ii), T_S and T_{ON} are kept constant (T_S=120 µs and T_{ON}=12 µs, respectively), whereas the self-heating effect is investigated by changing the triode-current between 3.5 A and 12 A. The current level was adjusted by acting on V_{PL}, while the gate signal is not varied (V_{GL}=-5 V and V_{GH}=20 V), to guarantee the same gate-induced stress for all the tested conditions. The drifts experimented in the 1s-1000s time range are presented in Fig. 3.15. As we can see, a larger negative V_{TH} shift was obtained for I_{DS}=12 A, corresponding to a higher R_{ON} degradation. Conversely, for I_{DS}=3.5A, a negligible R_{ON} drift and a reduced V_{TH} instability were observed.

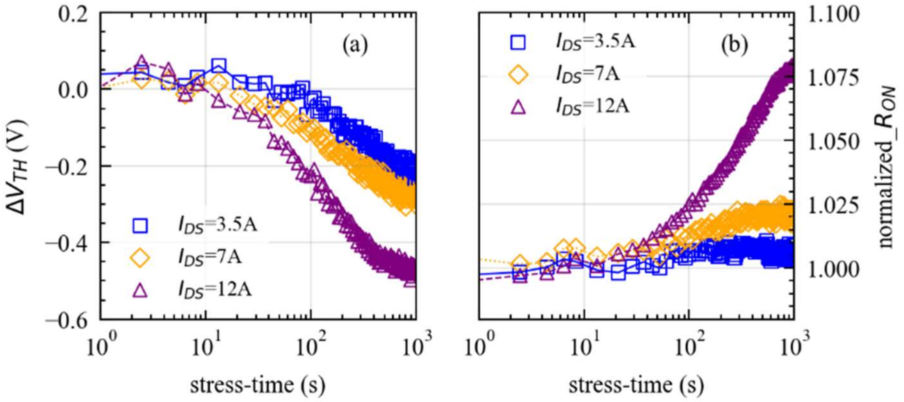

Figure 3.15: (a) Effect of drain current level (I_{DS}) on V_{TH}. (b) Effect of drain current level (I_{DS}) on R_{ON}.

These results are coherent with the interpretation proposed so far. In fact, at higher V_{PL} and I_{DS} levels, the average power dissipation becomes significant and the device temperature increases as a consequence of the self-heating effect (SHE). In fact, an increase in the device temperature results in a fewer negatively-charged interface traps [17], yielding a decrease in V_{TH}. At the same time the device R_{ON} increases with temperature due to the reduction in electron mobility (μ_n) caused by the interaction of the carriers with the lattice vibrations [21].

Accordingly, we can speculate that self-heating effects impact significantly both R_{ON} and V_{TH} parameters during conventional switch-mode operations. Particularly, a positive R_{ON} drift is expected to increase the conduction losses in power converters, thus yielding a significant efficiency reduction. On the other hand, the observed V_{TH} instability could be a concern for the device reliability as well, since a negative shift of the I_{DS}-V_{GS} characteristic could lead to a substantial increase in the subthreshold leakage current. For a power MOSFET, this would mean an increase in drain leakage in the off-state and therefore a decrease in its functional blocking voltage [22].

3.3 Comparison between Soft and Hard Switching Transitions

So far, we have discussed the on-the-fly monitoring of V_{TH} and R_{ON} drifts in soft-switching (SS) mode [15]. However, SS represents just a relaxed operative scenario, since devices may also be driven in more severe hard-switching (HS) conditions [23]. Particularly, during HS mode operation, the DUT is switched at high current and high voltage levels simultaneously, and this condition may be responsible for additional parameters degradations due to hot-carriers and/or self-heating effects (SHE) [24, 25]. Accordingly, the operative mode (SS or HS) could have a significant impact on the parameters drifts.

Aim of this section is thus to extend the monitoring of V_{TH} and R_{ON} to HS operations, highlighting the role of transitions on the parameters drifts [26]. To this end, we still employed the measurement setup presented in Chapter 2, allowing for the first time the on-the-fly characterization of both V_{TH} and R_{ON} during HS mode operation in packaged SiC MOSFETs. Particularly, in order to highlight the impact of the operative mode on the parameters degradations, we compare the results obtained under both SS and HS. Then, by focusing on HS mode, we investigate the effect (i) of the drain voltage applied in off-state (V_{PH}) and (ii) of the gate resistance (R_G) used for driving the DUT. A thermal characterization is then performed in order to properly investigate the role of self-heating effects (SHE), becoming more pronounced in HS, due to transitions performed at high current and high voltage levels.

Devices tested (named as Type-C) were 650V/120mΩ TO-247 packaged SiC MOSFETs. The simplified schematic of the setup configuration employed for the stress/measurement is reported in Fig. 3.16, in which we can recognize the current limiter described in Chapter 2, that is extremely important for performing a controlled Hard-Switching mode characterization.

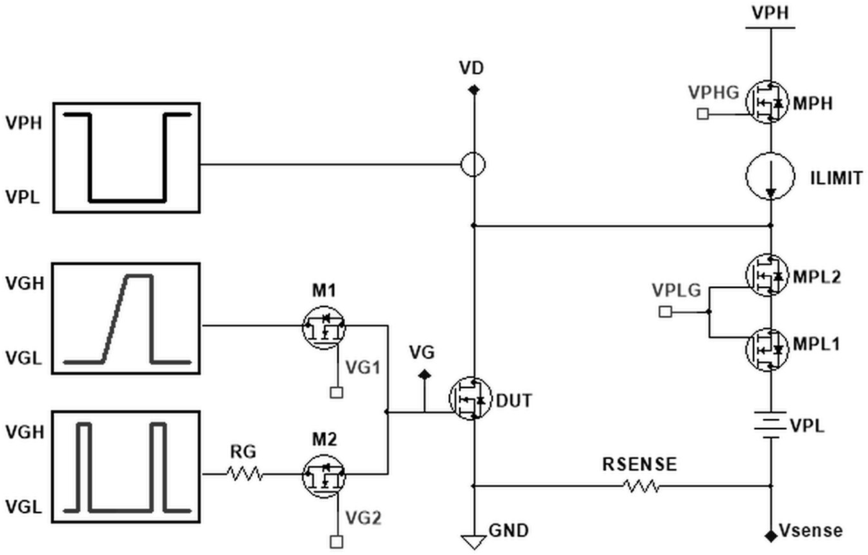

Figure 3.16: Simplified schematic of the measurement setup configuration: R_{SENSE} (0.1 Ω) is used for measuring I_{DS}. M_1 and M_2 provide the driving V_{GS} to the DUT, allowing both soft- and hard-switching operations.

The DUT is continuously switched between a high voltage off-state condition (V_{PH}) and a low voltage on-state one ($V_{PL} = 1.5$ V) with a 120 µs switching period and an 18 µs on time. In off-state, a $V_{GS} = -5$ V is provided in order to safely turn-off the device under test [6], whereas in on-state a ramp-like V_{GS} (see Fig. 3.17(a)) is applied to the DUT to measure its I_{DS}-V_{GS} characteristic and extract the device's threshold voltage. A stable V_{GS} level (e.g., 20 V) is held at the end of the ramp for a correct R_{ON} measurement in triode region. The parameters evolution is monitored over 1000 s of operation (i.e., stress-time) by means of a Digital Sampling Oscilloscope (DSO) whose acquisition is triggered logarithmically [16] according to the MCU program presented in Chapter 2.

3.3.1 Control of Soft- and Hard-Switching operations

To highlight the impact of transitions, measurements are performed under both soft- (SS) and hard-switching (HS) conditions, whose typical measurement waveforms are sketched in Fig. 3.17(a) and Fig. 3.17(b), respectively.

Drain voltage transitions are performed by means of n-channel MOSFETs (M_{PH}, M_{PL1} and M_{PL2}) arranged in a push-pull configuration. As already mentioned in Chapter 2, M_{PL1} and M_{PL2} are connected in anti-series on the V_{PL} branch in order to avoid conduction through their body diodes in HS mode. In SS conditions, the gate driving voltage is provided to the DUT by turning-on M_1. On the other hand, HS operations are allowed by M_2, thanks to which a gate resistance R_G is connected to the DUT, while V_{PH}/V_{PL} (V_{PL}/V_{PH}) transitions are led at constant current ($I_{LIMIT} = 2$ A). Then, equivalently to SS mode, M_1 is activated for V_{TH} and R_{ON} extraction in on-state. The required synchronization between M_1 and M_2 is guaranteed by an MCU that generates all the driving signals for the measurement.

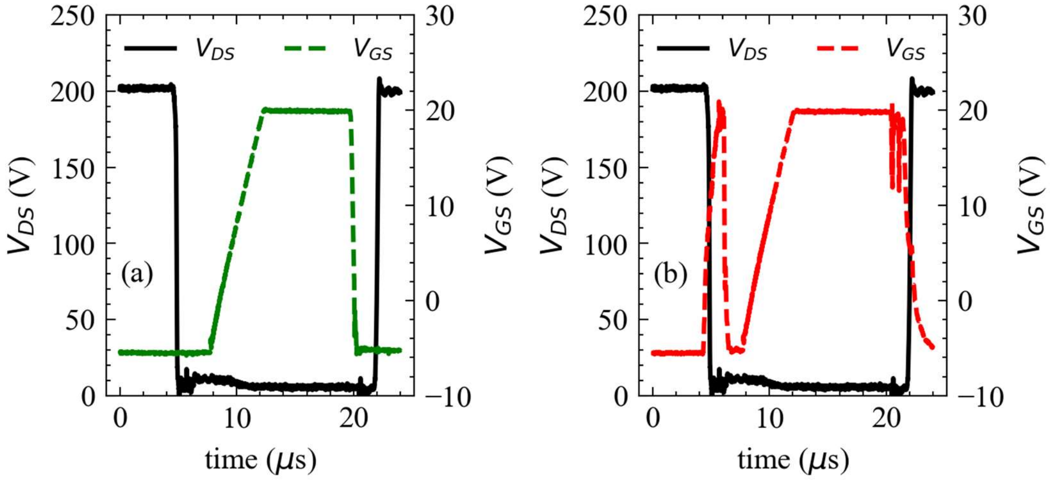

Figure 3.17: V_{DS} and V_{GS} waveforms employed in (a) soft- (SS) and (b) hard-switching (HS) conditions. SS transitions are led at I_{DS} = 0 A. HS transitions are led at I_{DS} = I_{LIMIT} = 2 A with a gate resistance R_G = 220 Ω. A ramp-like V_{GS} ranging from -5 V to 20 V is applied to the DUT for V_{TH} and R_{ON} extraction in on-state.

In the following, we separately evaluate the effects of (i) the drain voltage applied in off-state (V_{PH}) and (ii) the gate resistance (R_G) employed in HS condition. The parameters drifts are represented in terms of their relative variations with respect to the fresh V_{TH} and R_{ON} values measured before starting the stress (i.e., V_{TH0} and R_{ON0}).

3.3.2 V_{PH} effect

The evolution of V_{TH} and R_{ON} in SS and HS conditions is reported in Fig. 3(a) and Fig. 3(b), in which we observed negative V_{TH} shifts and positive R_{ON} drifts.

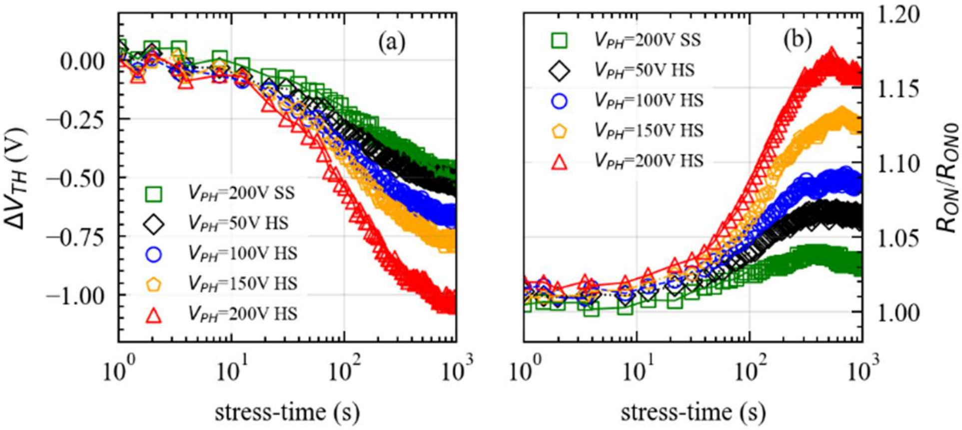

Figure 3.18. (a) ΔV_{TH} (V_{TH}-V_{TH0}) and (b) R_{ON}/R_{ON0} transients monitored at room temperature (R_T) during soft- (V_{PH} = 200 V) and hard-switching (V_{PH} between 50 V and 200 V) operative mode.

Looking at Fig. 3.18, we immediately observe that V_{TH} and R_{ON} transients present similar time constants, suggesting that a single underlying mechanism may be responsible for both drifts [20]. Moreover, parameters degradations are larger in HS and increase while passing from V_{PH} = 50 V to V_{PH} = 200 V.

The fact that both V_{TH} and R_{ON} drifts are larger in HS with respect to SS, suggests that the conduction of relatively high current during transitions (i.e., I_{LIMIT} = 2 A) is detrimental for the device operation. In fact, during HS transitions, a high current level flows through the DUT for a non-null time interval (i.e., Miller Plateau), yielding a relatively high power dissipation in the device. This effect is enhanced at high V_{PH}, since the dissipation increases and transitions get longer, as indicated by the enlarged Miller plateau (see Fig. 3.19).

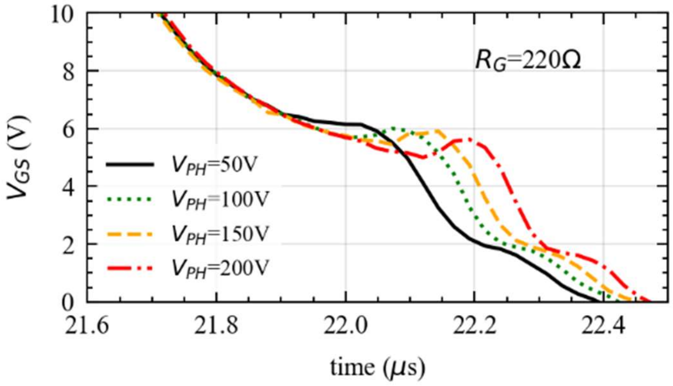

Figure 3.19: Miller plateau measured during the turn-off transition in hard-switching conditions for different V_{PH} (between 50 V and 200 V) at RT.

Accordingly, the larger degradation observed at higher V_{PH} in HS could be associated to longer transitions performed at high power levels, that yields a significant increase in the average power dissipation in the DUT. In fact, longer transitions at high I_{DS} and V_{PH} results in a non-negligible self-heating effect (SHE), yielding a temperature (T) increase in the DUT that could explain both V_{TH} and R_{ON} drifts.

This interpretation is coherent with the V_{PH} effect observed. However, by increasing V_{PH}, other field-enhanced mechanisms (e.g., hot carriers' effects) may come into play, being responsible for dynamic-R_{ON} and V_{TH} instability. In order to exclude other field-dependent mechanisms and further validate our interpretation, it is important to investigate the problem from a different point of view. To this end, it is possible to act on the transition time (i.e., switching time), while keeping constant V_{PH}. This can be done by changing the gate resistance R_G. In fact, the Miller plateau shown in Fig. 3.19 is magnified by the large gate resistance chosen [27] (R_G = 220 Ω), since a higher R_G yields a reduction in the switching speed, with a consequent increase in the transition time [27-29]. Accordingly, if the switching time plays any role on the parameters degradation, a change in R_G would produce a significant effect on V_{TH} and R_{ON} drifts.

3.3.3 R_G effect

In order to assess the impact of the transition time on the parameters degradation, we compared the results obtained with different gate resistances (R_G). The results are shown in Fig. 3.20.

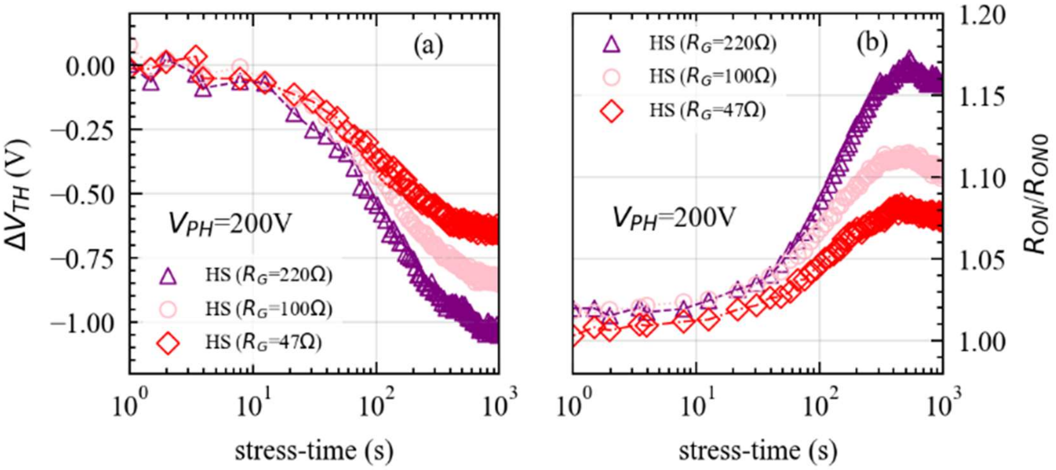

Figure 3.20: (a) ΔV_{TH} (V_{TH}-V_{TH0}) and (b) R_{ON}/R_{ON0} transients measured at R_T (V_{PH} = 200 V) with a gate resistance R_G = 220 Ω, R_G = 100 Ω and R_G = 47 Ω. A higher R_G increases the transition time. This enhances the parameters degradation in HS mode operation.

As we can see in Fig. 3.20, both V_{TH} and R_{ON} drifts get higher when R_G increases from 47 Ω to 220 Ω. This is coherent with the interpretation proposed so far, since a higher gate resistance reduces the DUT switching speed, resulting in a longer transition time. This yields an increase in the average power dissipated by the DUT during HS operation, causing the self-heating effect to increase significantly. According to this consideration, the observed parameters drifts may be completely ascribed to the temperature rise in the DUT induced by SHE. To verify this hypothesis, the role of temperature and SHE on the parameters stability is investigated in the following subsection.

3.3.4 Role of temperature and Self-Heating Effect (SHE)

In order to get a preliminary indication on the role of temperature, we performed a thermal characterization by focusing on the I_{DS}-V_{GS} characteristics of the DUT (see Fig 3.21). To this end, a thermal chuck (thermally connected to the device via the back metal contact of the package) was used for setting the device temperature during the measurements.

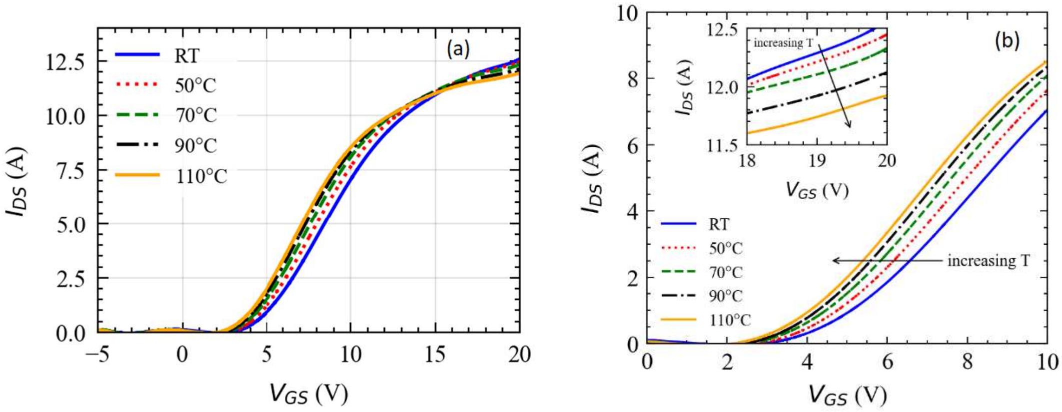

Figure 3.21: (a) I_{DS}-V_{GS} curves measured at different temperatures (T) using a thermal chuck. At higher T, V_{TH} decreases due to fewer negatively charged interface traps, while the triode I_{DS} decreases (i.e., R_{ON} increases) due to a reduced carriers' mobility (see figure (b) inset).

The results obtained seem to confirm our hypothesis. In fact, an increase in T yields a reduction in V_{TH} due to fewer negatively charged interface traps [8, 17, 30] and reduces the DUT triode current due to a lower electrons' mobility (see Fig. 3.21), caused by the interaction of carriers with lattice vibrations [21]. This behavior is consistent with the trends observed during the on-the-fly monitoring of V_{TH} and R_{ON}, indicating that both drifts positively correlate with device self-heating. Nevertheless, this indication is still insufficient to completely associate V_{TH} and R_{ON} drifts to SHE. In fact, we also need to discern thermal and electrical contributions on the parameters drifts observed under SS and HS operation. To this end, we repeated the on-the-fly characterization by connecting a heatsink to the DUT (see Fig. 3.22). In fact, with a heatsink connected, we can reduce the heating effects and highlight just the electrical contributions on the V_{TH} and R_{ON} drifts.

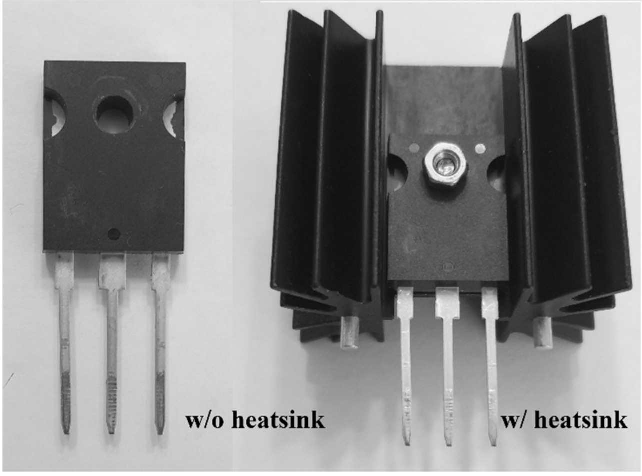

Figure 3.22: Picture of the Device Under Test (DUT) with (w/) and without (w/o) heatsink connected.

In Fig. 3.23, we compared the results obtained in both SS and HS conditions with (w/) and without (w/o) the heatsink connected to the DUT. With the heatsink, the V_{TH} and R_{ON} degradations reduce (see Fig. 3.23(a) and Fig. 3.23(b)) yielding overlapped SS and HS transients at V_{PH} = 200 V. This result indicates that the observed drifts were mainly induced by SHE, becoming more pronounced in HS due to transitions performed at high I_{DS} and V_{PH}.

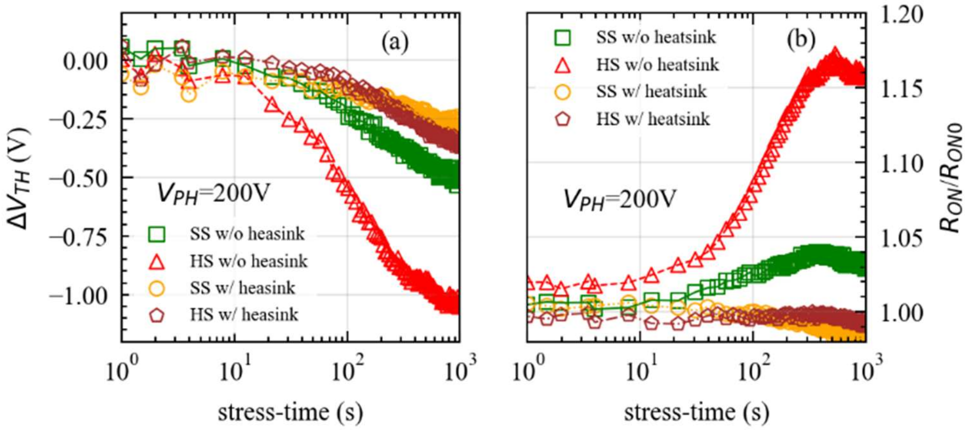

Figure 3.23: (a) ΔV_{TH} (V_{TH}-V_{TH0}) and (b) R_{ON}/R_{ON0} transients measured at R_T (R_G = 220 Ω, V_{PH} = 200 V) with (w/) and without (w/o) heatsink. V_{TH0} and R_{ON0} are the fresh V_{TH} and R_{ON} values measured before starting the stress. The differences observed between SS and HS conditions without heatsink can be ascribed to a different self-heating effect, since transients collected with heatsink are perfectly overlapped.

The fact that perfectly overlapped transients have been obtained with heatsink connected under both SS and HS conditions yields two important considerations. (i) The thermal contribution on V_{TH} and R_{ON} drifts may be significant (or dominant) in SiC devices operating in hard-switching conditions. (ii) No additional trapping/de-trapping effects were induced by HS mode operation on tested devices, a part from the thermal-dependent occupancy of interface traps, This indicates that the slow V_{TH} and R_{ON} transients obtained in HS w/o heatsink can be ascribed to the transient thermal behavior of the DUT [31] resulting from the heating up of the device. This information has to be taken into account while characterizing SiC MOSFETs under HS mode operation, in order to correctly identify the cause for parameters degradation, thus avoiding wrong data interpretations.

3.4 Study on V_{TH} instability and underlying physics

A part from the role of temperature, which affects both V_{TH} and R_{ON} parameters, the most important problem affecting SiC devices operation is the V_{TH} stability. Accordingly, in the following subsections we will mainly focus on V_{TH} drifts with some specific characterizations that aims to understand the physical mechanisms governing this undesired behaviour.

To this end, measurements were performed by means of the designed measurement setup, employing the reduced schematic configuration shown in Fig. 3.24.

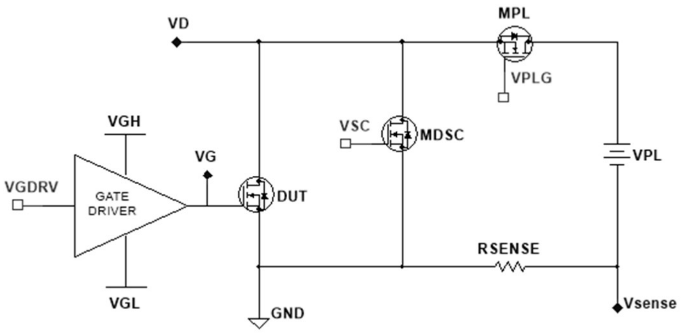

Figure 3.24: Reduced schematic configuration of the measurement setup used for the evaluation of V_{TH} instability.

3.4.1 Dits vs NIOTs

Both interface (Dits) and near interface oxide (NIOTs) traps could be responsible for V_{TH} drifts in SiC devices [30]. Particularly, charge trapping in these defects is mainly due to the gate biasing, as proven by bias temperature instabilities (BTI) studies [9]. It is thus important to discern Dits and NIOTs contributions on said V_{TH} drifts induced by gate signals applied during conventional switch-mode operations.

To this end, similarly to the studies just reported, the Device Under Test (DUT) is continuously switched on and off with a 120 µs switching period (T_S) and 6 µs T_{ON}. During T_{ON}, the transistor M_{PL} is turned-on with a 2 V drain voltage, while a ramp-like gate signal from V_{GL} to V_{GH} is applied to the DUT to reconstruct its complete I_{DS}-V_{GS} characteristic. During the off phase, DUT V_{GS} is settled to V_{GL} while V_{DS} is clamped to 0 V by M_{DSC}. Before starting the stress, a double-ramp gate signal is applied in order to capture gate-induced hysteresis on V_{TH} and fixing a reference fresh value (V_{TH0}) used for evaluating the relative V_{TH} variation during testing (see Fig. 3.25).

A 1000 s stress is then applied to the DUT, during which the V_{TH} evolution is monitored. The typical waveforms employed for the measurement are sketched in Fig. 3.2, in which we can recognize the two main phases: (i) pre-stress and (ii) stress.

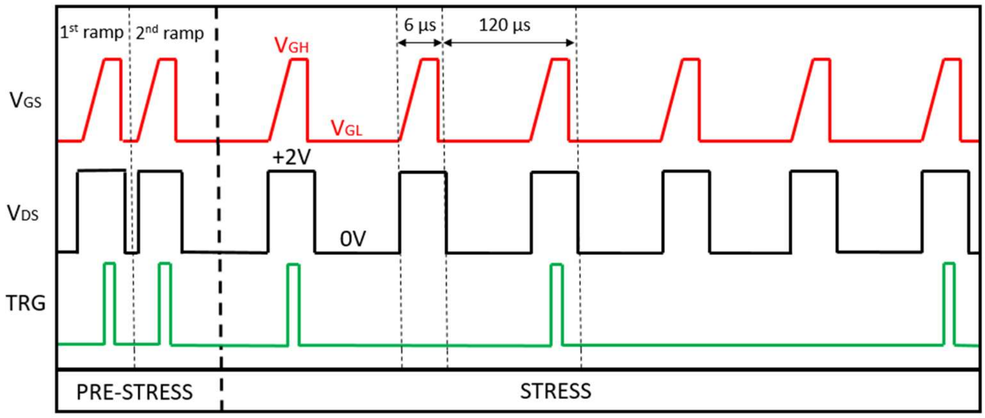

Figure 3.25: Typical measurement sequence. DUT is continuously switched on and off at every cycle with T_S=120 µs. The DSO acquisition is triggered (TRG) at logarithmically spaced time intervals to preserve time accuracy over several decades.

A different set of SiC-based power MOSFETs was considered for this study, hereby named as Type-D, presenting 1200 V breakdown voltage and 520 mΩ on-state resistance. Fig. 3.26 shows the I_{DS}-V_{GS} characteristics measured with the double-ramp in the pre-stress phase (V_{GL}=0 V; V_{GH}=15 V). Similarly, to what has been previously observed on Type-B samples, a single sweep-up of the gate voltage is sufficient to positively shift V_{TH}, as observed with the 2nd ramp. Coherently with the interpretation provided, this effect can be ascribed to the tunneling of electrons into oxide traps [17] and it is not recoverable in the short time interval preceding the 2nd ramp due to the slow nature of the emission process.

This positive V_{TH} shift is not recovered after ~100 µs off-state biasing (V_{GL}=0 V) at 30 °C, meaning that the negative charge previously captured in the oxide is still retained at the beginning of the stress phase.

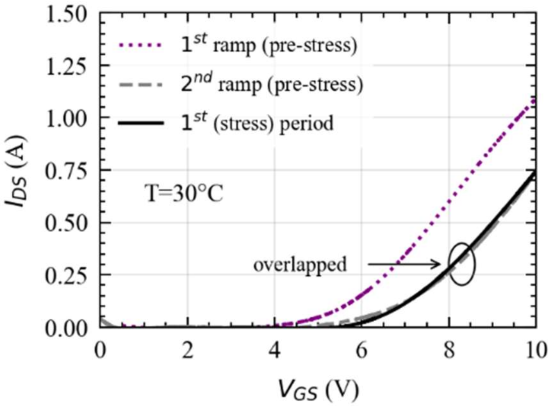

Figure 3.26: I_{DS}-V_{GS} curves acquired in the pre-stress phase with the double-ramp signal and with the 1st stress ramp. Curves acquired with 2nd pre-stress and 1st stress ramps are overlapped.

During the stress, we observe that V_{TH} increases with time, indicating the presence of an average positive-BTI (PBTI) effect induced by the positive gate voltage (+15 V) applied in on-state (see Fig. 3.27).

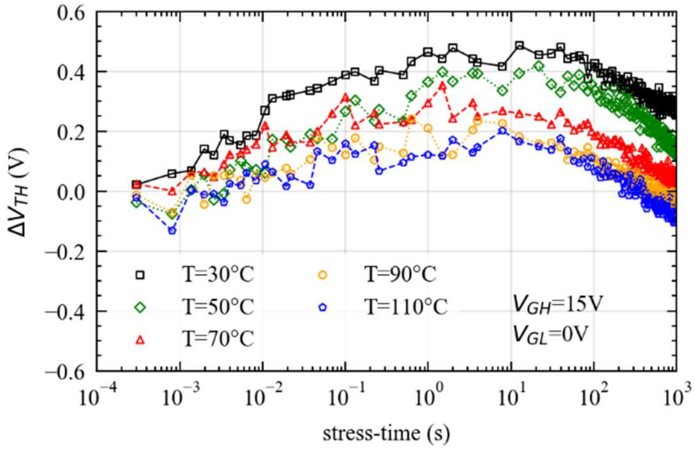

Figure 3.27: ΔV_{TH} (V_{TH}-V_{TH0}) transients measured at different temperatures with V_{GL}=0 V and V_{GH}=15 V.

This PBTI effect could be associated to electron capture into interface traps [30]. Accordingly, by increasing the device temperature (T), we do not observe any speed-up in the ΔV_{TH} transient, which would instead be indicative of a hole emission process.

On the other hand, the amplitude of the positive ΔV_{TH} transient decreases while increasing T, due to a reduced electron retention capability of interface traps [19, 30].

In order to have a more complete picture of the device behavior, we should also investigate the effect of negative V_{GS} applied in off-state (i.e., V_{GL} < 0V). In fact, a negative gate bias is typically applied in off-state during switch-mode operations, in order to prevent false turn-on when the device is switched at large drain voltages [6].

To this end, we changed the driving conditions by applying a gate ramp ranging from V_{GL}=-5 V and V_{GH}=15 V. In these operative conditions, the average PBTI effect observed with V_{GL}=0V disappears (see Fig. 3.28), indicating that the negative V_{GL} applied in off-state facilitates electron emission from interface traps.

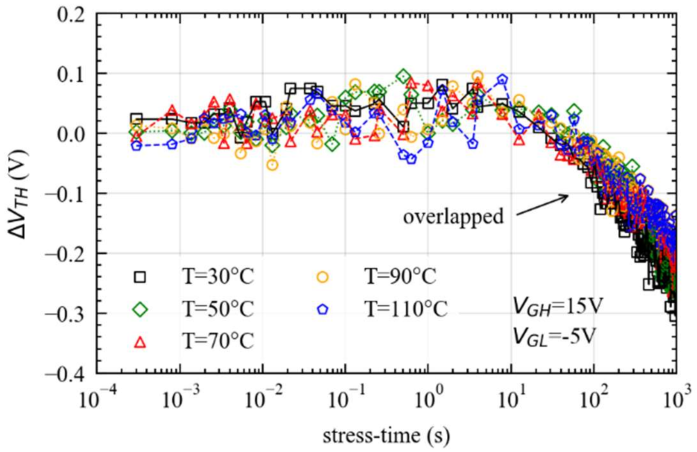

Figure 3.28. ΔV_{TH} (V_{TH}-V_{TH0}) transients measured at different temperatures with V_{GL}=-5 V and V_{GH}=15 V.

Further looking at Fig. 3.28, a negative V_{TH} drift presenting a weak temperature dependence is observed in the 1 s to 1000 s time range, yielding a perfect overlapping between transients collected at different T. This behavior could be signature of a tunneling mechanism, which is expected to be almost temperature independent [32].

This interpretation is also supported by Fig. 3.29, in which a linear-with-log-time dependence [33] was found for the slow ΔV_{TH} transient measured at 30 °C. In fact, tunneling processes typically yields a linear-with-log-time evolution of the V_{TH} drift [33].

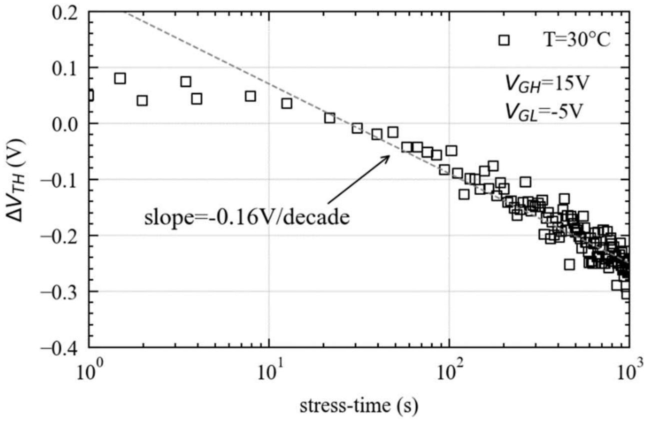

Figure 3.29: ΔV_{TH} transient measured at 30 °C (V_{GL}=-5V; V_{GH}=15V). V_{TH} drift follows a linear-with-log-time dependence (-0.16 V/decade), that is indicative of a tunneling mechanism.

The time range in which the transient appear is coherent with NIOTs dynamics [30, 32]. Accordingly, the negative ΔV_{TH} transients can be ascribed to the tunneling of electrons from near interface oxide traps (NIOTs) [32], previously filled by the 1st pre-stress gate ramp.

3.4.2 Identification of Interface states responsible for hysteresis

We have already mentioned that both short-term and long-term BTI effects can be observed in SiC devices [34], suggesting the importance to discern hysteresis effects from long-term degradations [20]. Aim of this subsection is thus to identify the interface states responsible for V_{TH} hysteresis in packaged SiC MOSFETs. To this end, we propose a novel double-ramp measurement method that allows to study the V_{TH} hysteresis induced by the gate driving voltage and, at the same time, gather information concerning the time required for a complete parameter recovery. Particularly, with this method, we evaluated the positive V_{TH} shift induced by the turn-on of the DUT.

Devices Under Test were 1200V/75mΩ TO-247 packaged SiC MOSFETs, i.e., Type-E. In order to investigate hysteresis effects induced by positive V_{GS}, we employed the double-ramp gate signal shown in Fig. 3.30.

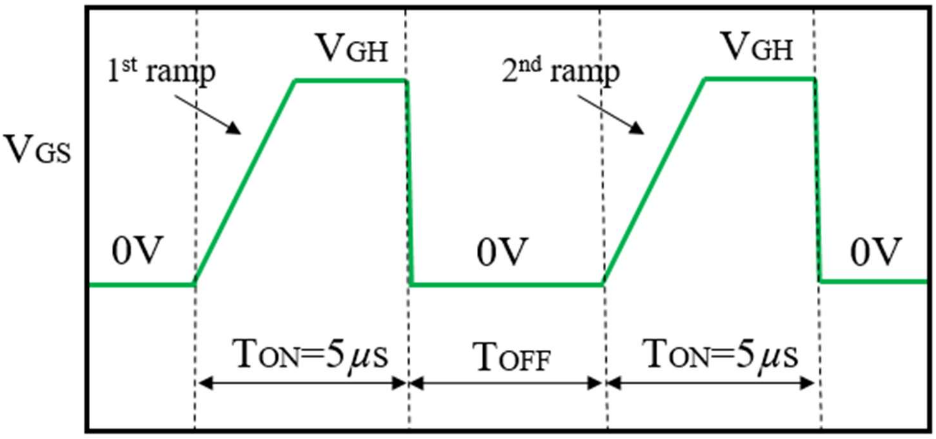

Figure 3.30: Typical waveforms employed for the measurements. During T_{ON}, a V_{DS} = 2 V is applied to the DUT, while the gate voltage (V_{GS}) is ramped from 0 V to V_{GH} in 2 μs for reconstructing the I_{DS}-V_{GS} characteristics and extract V_{TH}. A stable V_{GH} level is kept at the end of the ramp for 3 μs, yielding an overall T_{ON} of 5 μs. During T_{OFF}, the DUT is biased at V_{GS} = 0 V and V_{DS} = 0 V.

The 1st ramp signal allows to measure the fresh I_{DS}-V_{GS} characteristic of the DUT, whereas the 2nd V_{GS} ramp captures hysteresis effects induced by the 1st ramp. Accordingly, the measurement sequence consists of two on-state time intervals (T_{ON}) separated by a short off-state biasing (T_{OFF}).

During T_{ON}, a V_{DS} = 2 V is applied to the DUT, while the gate voltage (V_{GS}) is ramped from 0 V to V_{GH} in 2 μs for reconstructing the I_{DS}-V_{GS} characteristics and V_{TH} is extracted. A stable V_{GH} level is held at the end of the ramp for 3 μs, yielding an overall on-state time of 5 μs. A variable off-state time (T_{OFF}) is inserted between 1st and 2nd ramp to study the V_{TH} recovery at V_{GS} = 0 V and V_{DS} = 0 V.

In Fig. 3.31, we fixed T_{OFF} = 10 µs and we evaluated the effect of the positive V_{GH} applied during T_{ON}. A single sweep-up of the gate voltage (i.e., 1st ramp) was sufficient to positively shift V_{TH}, as observed with the 2nd ramp. This effect can be still ascribed to the capture of electrons into interface traps and it is frequently encountered behaviour that has been observed on all the SiC-based MOSFETs analyzed in this dissertation.

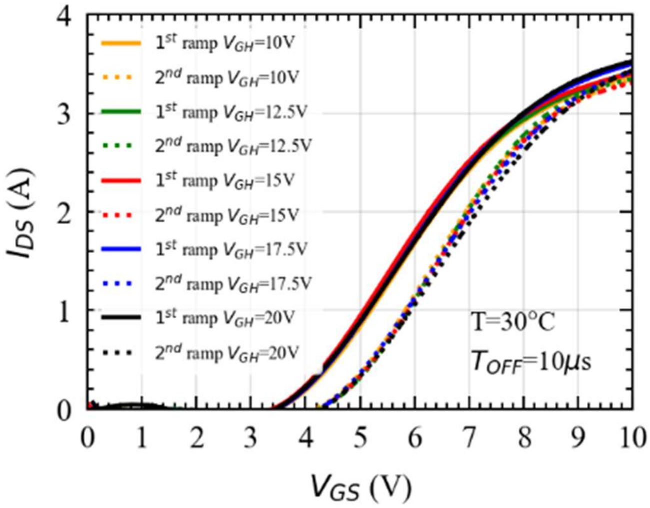

Figure 3.31: I_{DS}-V_{GS} curves measured with the double ramp gate signal for different V_{GH} with T_{OFF} = 10 µs and T = 30 °C. The positive V_{TH} drift captured by the 2nd ramp signal for T_{OFF} = 10 µs is always present, with comparable amplitudes, even if we change the V_{GH} level between 10 V and 20 V.

As shown in Fig. 3.31, the positive V_{TH} drift captured by the 2nd ramp signal for T_{OFF} = 10 µs is always present, with comparable amplitudes, even if we change the V_{GH} level between 10 V and 20 V. The fact that we do not observe any difference while increasing V_{GH} from 10 V to 20 V suggests that the observed hysteresis is not affected by the relatively high V_{GH} applied in on-state, leading us to exclude the involvement of deep oxide traps. Conversely, this drift can be ascribed to the sweep-up of the gate voltage above threshold, meaning that the channel formation is sufficient to induce the capture of electrons into interface traps and positively shift V_{TH}.

According to this interpretation, the electrons captured at the SiC/SiO_2 interface are still retained after 10 µs off-state biasing and a longer T_{OFF} would be required in order to allow a complete emission of the trapped electrons. It is thus important to investigate the effect of T_{OFF} on the V_{TH} hysteresis.

By increasing the off-state time between the two ramps, we found that the positive V_{TH} shift captured with the 2nd ramp disappears for T_{OFF} = 1 s. This means that the observed drift can be identified as a stability issue, since it does not provide any permanent degradations [35] (see Fig. 3.32).

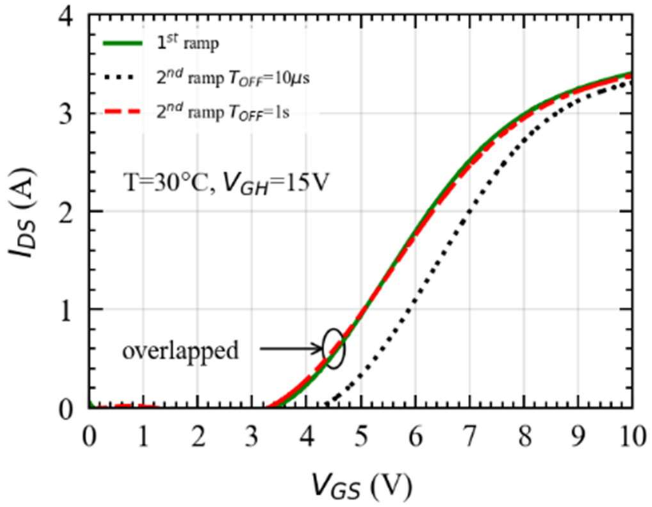

Figure 3.32: I_{DS}-V_{GS} curves measured with the double ramp gate signal for V_{GH} = 15 V and different off-state time (T_{OFF}) between the two ramps.

As shown in Fig. 3.32, after 1 s off-state biasing, the I_{DS}-V_{GS} characteristic acquired is perfectly overlapped with the curve measured with the 1st ramp, suggesting that the emission time constant (τ) of the trap states involved is shorter than 1 s. Accordingly, by varying T_{OFF} between 10 µs and 1 s we should be able explore the V_{TH} recovery dynamics.

In fact, by monitoring the hysteresis captured by the 2nd gate ramp at different T_{OFF}, we reconstructed the V_{TH} recovery transients shown in Fig. 3.33.

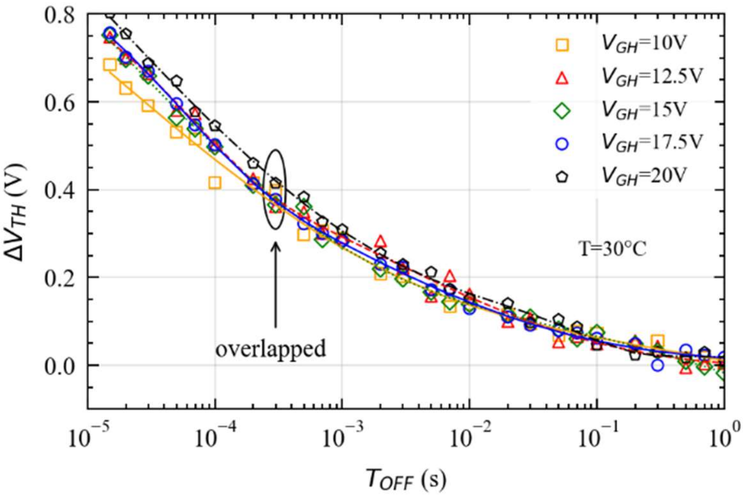

Figure 3.33. Hysteresis (ΔV_{TH}) captured by the 2nd V_{GS} ramp for different V_{GH} levels, by varying T_{OFF} between 10 µs and 1 s.

To perform this kind of measurement, we introduced 1 s off-state biasing after each hysteresis measurement in order to eliminate memory effects between consecutive acquisitions. In this way, a complete emission of trapped carriers prior to the subsequent double-ramp acquisition. The results shown in Fig. 3.31 and Fig. 3.32 find good correspondence in Fig. 3.33. In fact, a decreasing trend was obtained for the acquired V_{TH} transients, reaching ΔV_{TH}= 0 V at around T_{OFF}= 1 s. Moreover, the transients measured at different V_{GH} values (i.e., between 10 V and 20 V) are almost overlapped, further confirming that the observed hysteresis is not affected by the stable V_{GH} level held at the end of the 1st ramp. We can thus speculate that the on-state time interval (T_{ON}) is short enough to avoid deep trapping in the oxide, and the observed instability can be ascribed to traps close to the SiC/SiO_2 interface. Electron trapping into interface traps can be thus considered as the responsible for V_{TH} hysteresis in tested devices and the recovery transients in Fig. 3.33 are representative of the consequent electron emission.

It is well known that electron emission from traps is a thermally activated process. Accordingly, an increase in the device temperature (T) should facilitate the V_{TH} recovery. To verify this hypothesis, we performed the double-ramp measurement at different temperatures, varying T between 30 °C and 110 °C. Fig. 3.34 shows the effect of temperature on the I_{DS}-V_{GS} characteristics measured with 1st and 2nd V_{GS} ramps for T_{OFF}= 10 μs.

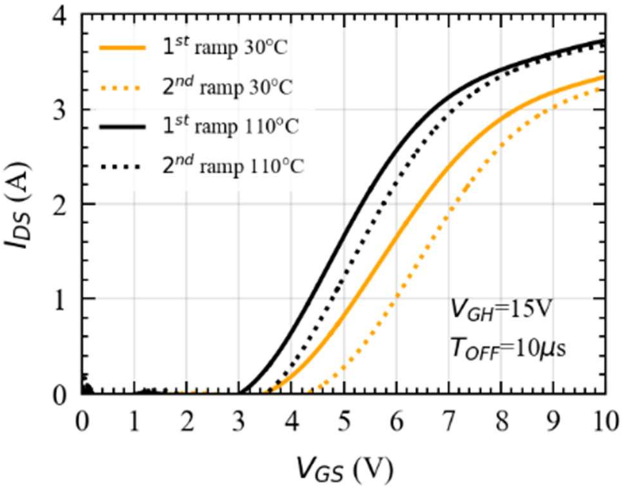

Figure 3.34: I_{DS}-V_{GS} curves measured with the double ramp gate signal for V_{GH} = 15 V, T_{OFF} = 10 μs and different temperatures (T = 30 °C and T = 110 °C).

By increasing T, for both ramps data, V_{TH} moves towards left due to fewer negatively charged interface traps [19]. Moreover, the hysteresis captured by the 2nd V_{GS} ramp at T = 30 °C is higher with respect to the one measured T = 110 °C. This is coherent with the fact that a higher T reduces the electron retention capability of interface traps [19, 30].

The effect observed in Fig. 3.34 is highlighted in Fig. 3.35, in which the V_{TH} recovery transient speeds-up while increasing T.

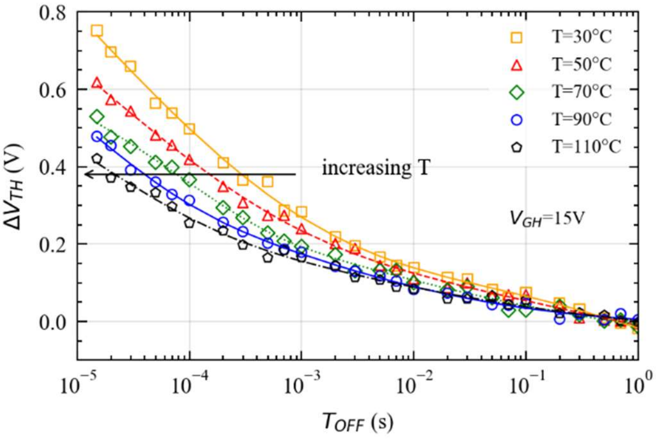

Figure 3.35: Hysteresis (ΔV_{TH}) captured by the 2nd V_{GS} ramp for different temperatures (T), by varying T_{OFF} between 10 µs and 1 s. A thermal chuck was used for setting the device temperature during the measurements.

The fact that the ΔV_{TH} measured for T_{OFF} = 10 µs reduces while increasing T, suggests that the recovery already started for shorter times which cannot be appreciated by the system. Nevertheless, the effect of temperature on V_{TH} hysteresis can be clearly appreciated, and the time range in which the thermally activated transient appears is coherent with the time constants typically presented by interface traps [30]. Accordingly, the observed instability can be ascribed to traps located at the SiC/SiO2 interface and the captured V_{TH} dynamics can be ascribed to the capture/emission of electrons from/to the SiC conduction band.

The information obtained so far provides an interesting picture of the device behavior. However, more information is required to identify the trap states involved in this process. To this end, the defects' activation energy (E_A) is extracted by means of the horizontal single point E_A extraction [36], see Fig. 3.36.

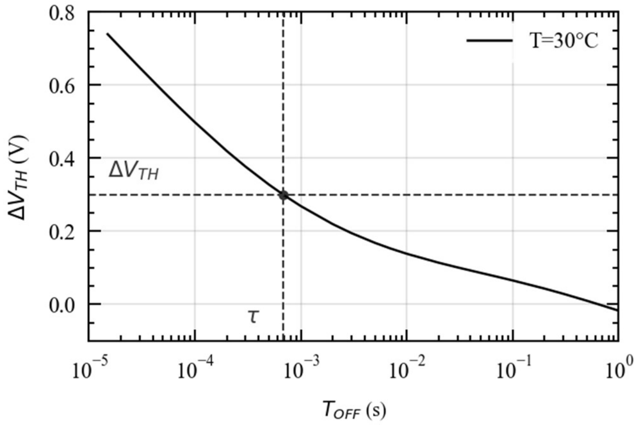

Figure 3.36: Single point method used for extracting the time constant (τ): we extract τ in correspondence to the chosen "horizontal point" (ΔV_{TH}).

The horizontal single point E_A extraction is more accurate with respect to the vertical one [36], but still depends on the choice of the "horizontal point" (ΔV_{TH}) considered for extracting the time constant (τ). It is thus important to investigate this dependence in order to verify if this method can provide reliable information on E_A. To this end, we extracted τ in correspondence to several ΔV_{TH} values (ranging between 0.2 V and 0.4 V). The corresponding values of τ are reported in Fig. 3.37.

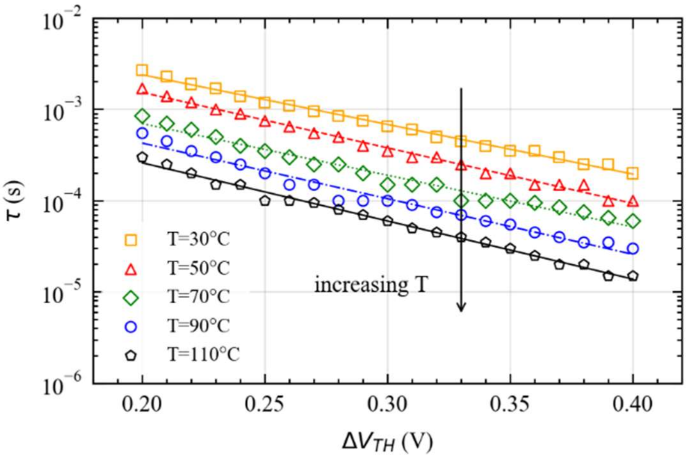

Figure 3.37: τ extracted in correspondence to several ΔV_{TH} values (ranging between 0.2 V and 0.4 V) and different temperatures (T between 30 °C and 110 °C).

This method could be effective for evaluating the activation energy (E_A), since, despite the obvious dependence of τ on the chosen ΔV_{TH} level, an increase in temperature equivalently affects the τ extracted at different ΔV_{TH}. In fact, by looking at the τ vs ΔV_{TH} plot shown in Fig. 3.37, we can recognize almost parallel τ-lines moving towards shorter times while increasing T. This is coherent with Shockley-Read-Hall theory.

In fact, the mutual correlation between τ and T is typically described by the Arrhenius equation [37], in which the emission time depends exponentially on T through the trap's activation energy. This dependence can be expressed according to the formula:

$$\tau = \frac{1}{T^2} \times \exp\left(\frac{E_A q}{kT} + C\right) \tag{3.1}$$

where E_A is the trap activation energy, C is a parameter dependent on the trap cross section (σ), k is the Boltzmann's constant, q is the elementary charge and T (expressed in Kelvin) is the temperature experienced by traps.

According to equation (3.1), the obtained τ have been then used for extracting E_A from the linear fit of logarithmic form of the Arrhenius equation [37]:

$$\ln(\tau T^2) = \frac{E_A q}{kT} + C \qquad (3.2)$$

This yielded the parallel Arrhenius plots shown in Fig. 3.38(a), whose slope corresponds to the traps activation energy.

The fact that parallel lines are obtained for different values of ΔV_{TH}, suggests that similar E_A have been extracted, independently on the chosen “horizontal point”. This result is confirmed by Fig. 3.38(b), in which E_A with negligible differences ($E_A \sim 0.3$ eV) were obtained for the whole ΔV_{TH} range considered.

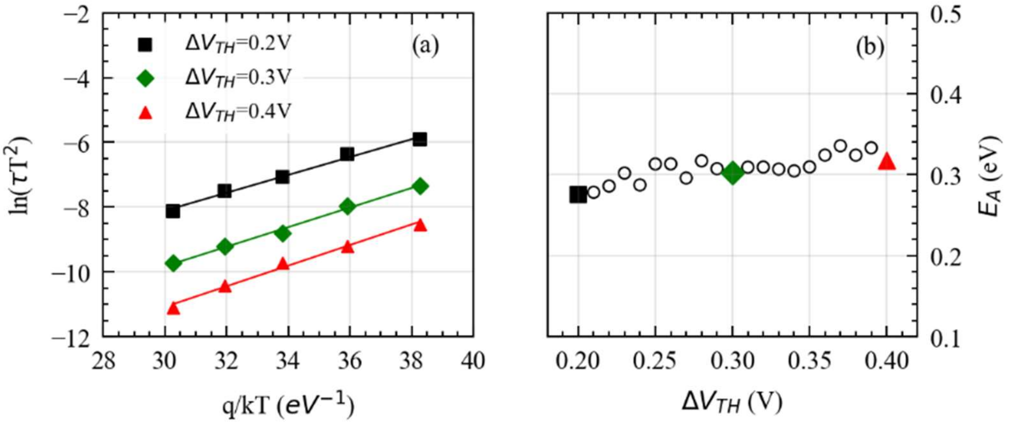

Figure 3.38: (a) Arrhenius plot obtained for the τ extracted in correspondence to $\Delta V_{TH} = 0.2$ V, 0.3 V and 0.4 V. (b) Dependence of the apparent activation energy (E_A) on the ΔV_{TH} value chosen for τ extraction. The trap state responsible for the observed V_{TH} hysteresis can be located at $E_A \sim 0.3$ eV below the SiC conduction band edge.

The trap states responsible for the observed V_{TH} hysteresis can be thus located at about 0.3 eV below the SiC conduction band edge (E_C). This is coherent with the high density of interface states located around this level [38], and could be ascribed to disorders at the SiC/SiO_2 interface [39].

However, since a continuous distribution of SiC/SiO_2 traps is typically reported [38], the observed instability is more likely to be due to a band of states rather than to a single level defect. Accordingly, the extracted E_A should be intended as the energy level presenting the peak concentration of interface states responsible for V_{TH} hysteresis in tested devices. This result is extremely important for properly modelling the device’s behavior and indicate that interfacial disorders are still a major cause of V_{TH} instability in SiC MOSFETs.

3.5 Conclusions

The results reported in this chapter indicates that the developed custom setup is able to perform accurate characterization of Packaged SiC MOSFETs under several stress conditions. First of all, the developed measurement technique was able to highlight V_{TH} and R_{ON} drifts in packaged SiC power devices, driven under conventional Soft-Switching mode operations. The observed slow negative V_{TH} shift was associated to the presence of traps at the SiC/SiO_2 interface. A direct correlation between V_{TH} and R_{ON} drifts was firstly speculated and then verified. To this end, the impact of the gate-driving voltage (V_{GH}) and of the off-state stress voltage (V_{PH}) were investigated. Particularly, two interesting results have been obtained: at relatively low V_{PH} (i.e., 100 V) the drifts can be totally ascribed to the continuous switching of the gate signal, whereas V_{PH} effect could be observed only at 500 V. This result is consistent with the vertical structure of tested devices, for which the gate potential is expected to mainly affect the dynamics of traps at the oxide-semiconductor interface. The study was further extended by introducing a double ramp method, that resulted effective in highlighting fast V_{TH} drifts caused by charge/discharge trapping phenomena beneath the gate contact as well as the slow ones affecting both V_{TH} and R_{ON}. The latter ones were studied by performing measurements for different on-state times and several triode currents, proving the role of device-self heating (SHE) in enhancing the parameters degradation. Self-Heating Effects resulted of primarily importance even under Hard-Switching mode operations, for which the usage of heatsinks resulted important to prevent excessive V_{TH} and R_{ON} drifts. Another key study concerned the role of interface (Dits) and near interface oxide (NIOTs) traps on the V_{TH} stability. Thermal dependent PBTI effects have been observed and associated to Dits, whereas tunneling form NIOTs yielded negative V_{TH} drifts on tested devices. Finally, to better investigate the physics behind interface traps, we characterized the V_{TH} hysteresis by means of time-dependent and temperature-dependent measurements. Trap states located at about 0.3 eV below E_C have been identified as the root cause for said hysteresis, associated to disorders at the SiC/SiO_2 interface.

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4 Dynamic-R_{ON} in GaN Power Devices

When GaN transistors are used in power switching converters, the most detrimental effect that directly impacts the converter efficiency is the increase in the dynamic-R_{ON} compared to its DC value [1]. This detrimental effects is due to trapping/de-trapping mechanisms that could take place both in the GaN Buffer and at the device surface [2]. While Surface trapping/de-trapping effects can be mitigated by optimized passivation and the usage of field plates [3, 4], Buffer traps are still a major cause for R_{ON} degradation as reported in by recent literature [2, 5]. With this in mind, it is important to mention that a physical mechanism leading to an increased negative charge in the GaN Buffer layer is required to induce the R_{ON}-degradation. Accordingly, both electron trapping and hole emission could, in principle, justify the dynamic increase in on-state resistance. As a relevant example, Carbon (C) dopants intentionally introduced in GaN buffer to make it semi-insulating [6], can induce peculiar trapping mechanisms, that are mainly governed by the C_N acceptor state at E_V+0.9 eV [5, 7, 8]. Particularly, holes are emitted by C-related traps within the gate-drain access region when the device is in the off state, leading to an increase in the density of negatively ionized C_N acceptors, and therefore to a dynamic decrease in the channel conductivity that yields an increased R_{ON} when the device is set back to on-state [5]. It is very important to accurately study the mechanism responsible for the R_{ON}-degradation in GaN power devices, in order to verify if hole emission can be considered as the root cause for this behaviour. To this end, we performed several measurements on tests devices which are reported in the following sections.

4.1 Tested Devices and Characterization Method

Devices tested for this study are packaged p-GaN gate AlGaN/GaN HEMTs grown by metal–organic chemical vapor deposition on a p-type Si substrate. The channel is composed of a Low-Carbon-doped (LC, ~10^{16} cm^{-3}) GaN layer of 0.3 µm. The GaN buffer layer instead is 4.7 µm thick and is highly C-doped (~10^{18} cm^{-3}). The AlGaN barrier layer is 15 nm thick with 22% Al concentration. The p-type GaN layer is 100 nm thick and has a nominal Mg doping concentration in the range of 10^{19}-5×10^{19} cm^{-3}. To define the p-Gate region, a Cl-based plasma etch was carried out [9]. The gate length is 1.5 µm. The depletion region forming due to the p-i-n diode corresponding to the pGaN/AlGaN/GaN heterostructure effectively suppresses the 2DEG when no gate bias is applied thus obtaining $V_{TH} > 0$ V. Ohmic contacts were formed by Ti/Al-based metallization defined by means of a lift-off process [10]. A schematic cross section of the devices under tests (DUTs) is reported in Fig. 4.1.

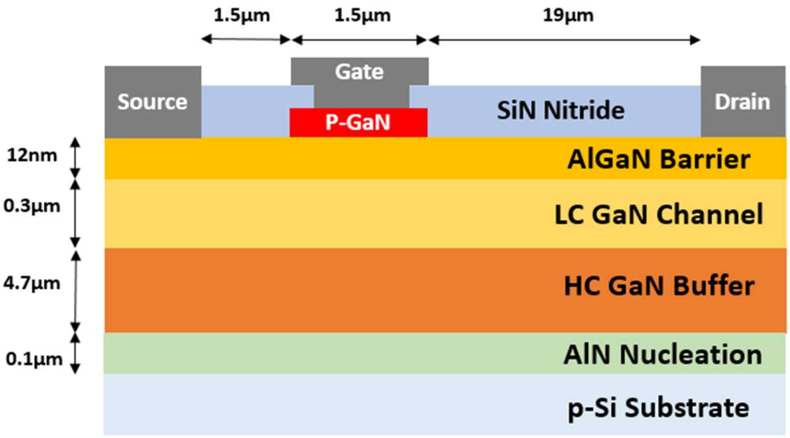

Figure 4.1: Schematic cross section of the AlGaN/GaN HEMT tested in this study.

The R_{ON} stability of devices under test (DUTs) was characterized by means of the custom measurement setup, described in Chapter 2. Before starting this stability characterization, the fresh R_{ON} was acquired at (V_{GS}, V_{DS}) = (6, 0.5) V to set the reference value (R_{ON0}). During the OFF-state stress, the DUT was periodically turned-on to monitor the dynamic R_{ON} evolution over several time decades (i.e., between 10^{-3} to 10^{3} s). To this end, a short (5 μs) low drain bias (0.5 V) was applied to the DUT at logarithmically spaced time intervals, during which V_{GS} was pulsed to 6 V to bring the DUT in its triode region (see Fig. 4.2).

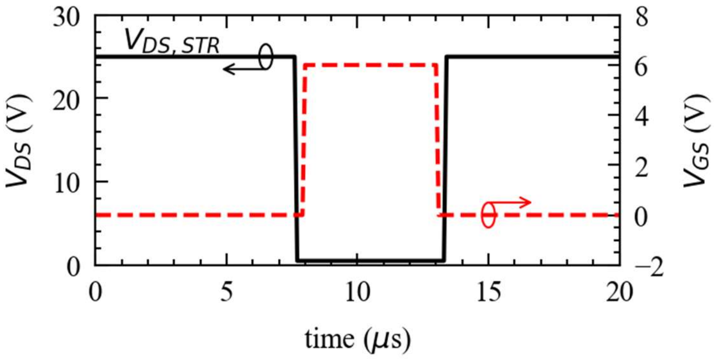

Figure 4.2: Typical V_{DS} and V_{GS} signals applied during the switch-mode characterization for monitoring dynamic R_{ON} evolution.

In this case, we did not apply a ramp like V_{GS} to reduce on purpose the delay between the OFF-state stress removal and the R_{ON} extraction. This is important in order to reduce as much as possible the relaxation time, thus preventing an underestimation of the R_{ON} degradation.

4.2 Experimental Results

The OFF-state stress characterization was performed at different $V_{DS,str}$ values in the range between 50 V and 500 V, in order to highlight the impact of the applied voltage to the dynamic-R_{ON} behavior. After 1000 s of stress-time we considered an additional 1000 s recovery-time during which the OFF-state stress was removed and the R_{ON} evolution was continuously monitored through the same V_{GS} pulse signal. The results obtained are shown in Fig. 4.3.

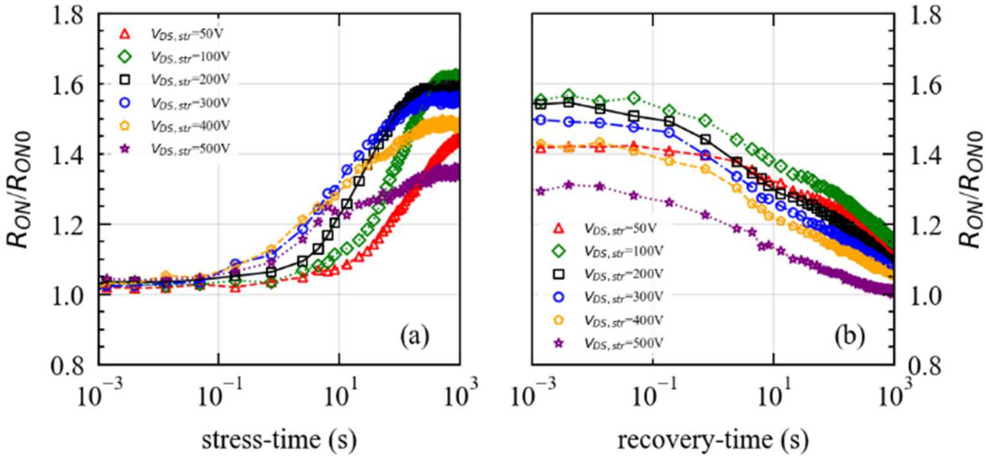

Figure 4.3: (a) Effect of drain off-state stress voltage on the R_{ON} drift during the stress with V_{GH} = 6V. (b) Monitored R_{ON} recovery at different drain stress voltages (50 V, 100 V, 200 V, 300 V, 400V and 500 V) with V_{GH} = 6 V.

During the stress phase (see Fig. 4.3(a)), we observe a dynamic increase in the R_{ON} over time, that shows up with an exponential-like transient. As we can see in Fig. 4.3(b), the induced R_{ON} drift is completely recoverable, independently on the applied stress voltage, indicating that the observed R_{ON} degradation is non-permanent and can be thus considered as a stability issue [11]. Nevertheless, it is important to identify the physics governing the observed behaviour in order to provide useful feedback for improving the device's manufacturing.

As widely pointed out in the literature, in present GaN power devices the increase in the dynamic R_{ON} compared to the static value can be attributed to the dynamics of buffer traps [12-16]. GaN HEMTs considered in this work feature a C-doped buffer, so that the prime suspect is the C_N state. To verify whether the measured dynamic R_{ON} dispersion is actually related to C-doping in the buffer, we performed OFF-state stress characterization at different temperatures. To this end, a thermal chuck (thermally connected to the device via the back metal contact of the package) was used for setting the device temperature during the measurements. A $V_{DS,str}$=25 V was adopted and the typical R_{ON}/R_{ON0} transients obtained in the 30 °C to 110 °C temperature range are reported in Fig. 4.4(a). To extract the time constants of the R_{ON} dynamics, the transients at each temperature were fitted by a stretched exponential function [17]. The associated time constant (τ) was then extracted in correspondence of the peak of the d[R_{ON}/R_{ON0}]/dlog$_{10}$t signal at each temperature, yielding the Arrhenius plot shown in the inset of Fig. 4.4(b).

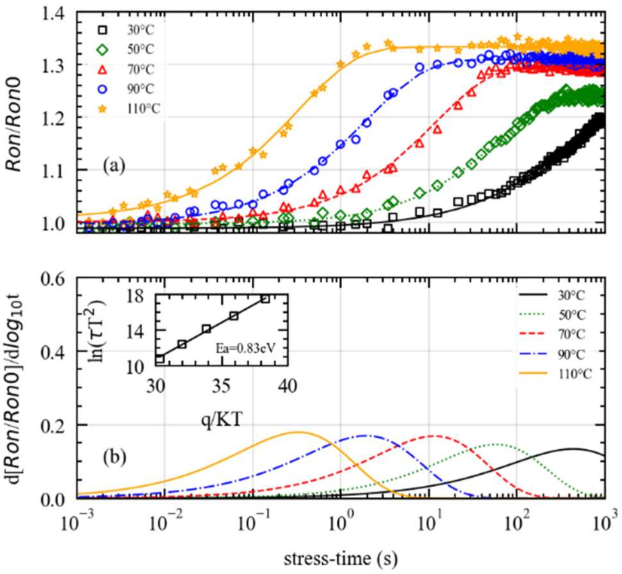

Figure 4.4: (a) R_{ON}/R_{ON0} transients measured at different ambient temperatures (from 30 °C to 110 °C, see legend) for an OFF-state drain-source voltage ($V_{DS,str}$) of 25 V. (b) Corresponding d[R_{ON}/R_{ON0}]/dlog$_{10}$t signals used for drawing the Arrhenius plot (figure inset). The linear fit of the logarithmic form of the Arrhenius equation yields an activation energy E_A=0.83 eV.

The linear fit of the points on the Arrhenius plot yields a 0.83 eV activation energy (E_A), which is consistent with values reported in the literature for the C_N states [8, 18]. Accordingly, the slow R_{ON} transients observed for tested devices can be ascribed to the emission of holes from C_N traps [8, 19].

The corresponding increase of dynamic R_{ON} during transients reported in Fig. 4.3, can thus be interpreted as being due to the negative charge build-up in the buffer layer in the gate-drain access region [1, 15, 19-21], as a result of negatively ionized Carbon acceptors.

4.3 $V_{DS,str}$ effect

Further looking at Fig. 4.3(a) we can recognize two main trends associated to the OFF-state stress voltage applied. Firstly, the amount of degradation captured after 1000 s stress-time (i.e., when the R_{ON} transient reaches its saturation) present a non-monotonic trend with $V_{DS,str}$. In fact, the amplitude of the R_{ON} transient increases while passing from 50 V to 100 V and then starts to decrease for higher $V_{DS,str}$ values. On the other hand, the R_{ON}-transient captured during the stress-phase speeds up while increasing the $V_{DS,str}$ voltage applied. This suggests the presence of a field-related mechanism that accelerates the R_{ON} degradation process.

The two effects just cited are independently addressed in the following subsections, to explain how the applied voltage could impact the R_{ON} dynamics induced by C_N states.

4.3.1 R_{ON}-transient speed-up

The first effect to be considered is the one related to the R_{ON} transient speed-up at increasing $V_{DS,str}$. As already mentioned, this effect could be associated to a field enhanced mechanism that facilitates the hole emission from Carbon acceptors. Particularly, since C_N states are acceptor-like traps located above the valence band [8], they can be modeled as Coulombic centers [22] that are negative when empty and neutral when filled. According to the theory, a Coulombic center could experience an electric field enhancement in its charge emission process due to the so called Poole-Frenkel Effect (PFE) [23, 24].

In order to verify this hypothesis, we acquired several R_{ON}-transients during the stress phase, while varying the applied stress voltage between 25 V and 300 V voltage, yielding the results reported in Fig. 4.5(a). Several $V_{DS,str}$ values have been considered in this range in order to have a more precise indication.

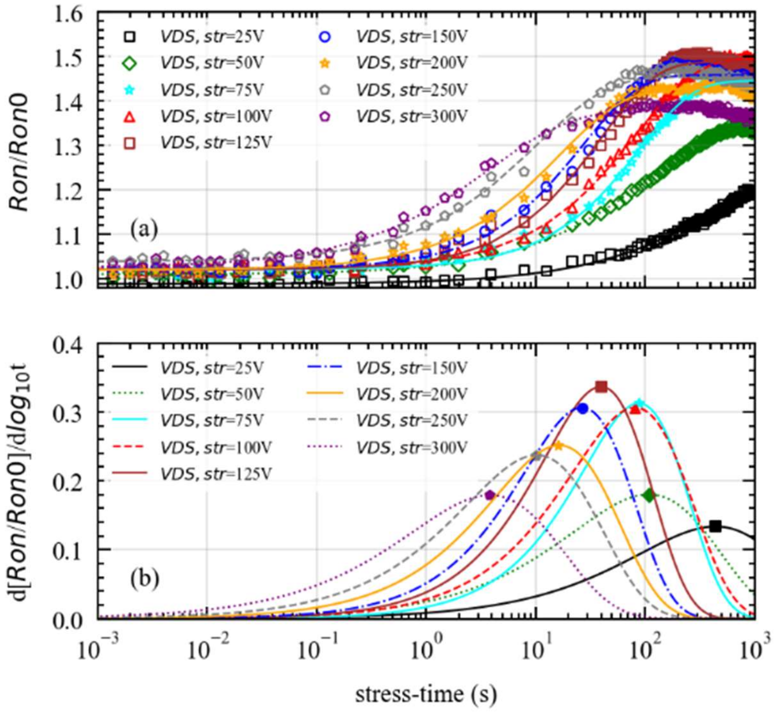

Figure 4.5: (a) R_{ON}/R_{ON0} transients measured at 30 ° for different OFF-state drain-source voltage ($V_{DS,str}$) between 25 V and 300 V. (b) Corresponding $d[R_{ON}/R_{ON0}]/dlog_{10}t$ signals used for extracting the transients time constant.

The observation made so far is confirmed by the transient measurements shown in Fig. 4.5(a) and further clarified by the derivative peaks moving towards shorter times while increasing

$V_{DS,str}$ (see Fig. 4.5(b)). Particularly, by extracting the transient's time constant in correspondence of the peak in the d[R_{ON}/R_{ON0}]dlog$_{10}$t signal, it has been possible to build the ln(τ) vs $\sqrt{V_{DS,str}}$ plot shown in Fig. 4.6.

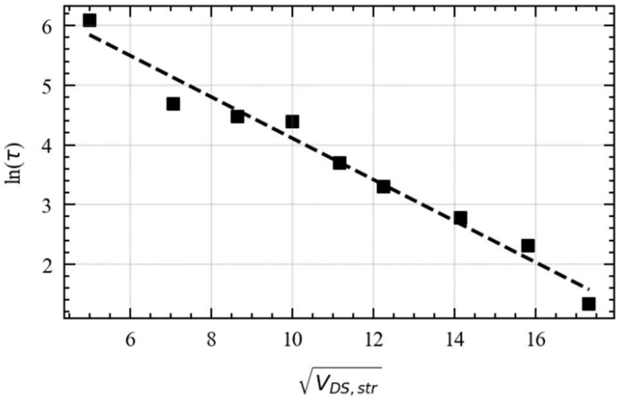

Figure 4.6: Natural logarithm of the extracted time constants (τ) from experimental R_{ON} transients vs $\sqrt{V_{DS,str}}$ at T = 30 °C. Black dashed line is the linear fit of the experimental data.

Fig. 4.5 shows that the computed ln(τ) presents a linearly decreasing trend with the $\sqrt{V_{DS,str}}$, consistently with the behaviour expected for Pool-Frenkel enhanced emission. In fact, the potential barrier lowering associated to the Poole-Frenkel Effect should result in a reduction of the emission time constant from traps according to the formula [23]:

$$\tau = \frac{1}{AT^2} \exp\left(\frac{E_A - \beta_{PF} \sqrt{F}}{kT} \right) \tag{4.1}$$

where k is the Boltzmann's constant, E_A is the trap's activation energy, F is the electric field, T is the absolute temperature while A is a constant referring to the trap emission cross section. The β_{PF} term in (4.1) refers to the Poole-Frenkel coefficient and is defined as [25]:

$$\beta_{PF} = \sqrt{\frac{q^3}{\pi \varepsilon_0 \varepsilon_r}} \tag{4.2}$$

By computing the natural logarithm of τ and assuming a linear dependence of the electric field on the applied voltage ($V_{DS,str}$), we obtain a linearly decreasing dependence (through a coefficient "coeff":

$$\ln(\tau) \Rightarrow -coeff\sqrt{V_{DS,str}} \tag{4.3}$$

Accordingly, the linearly decreasing trend observed in Fig. 4.6 can be considered as an experimental evidence of the Poole-Frenkel Effect in enhancing the charge emission process from C_N traps.

Moreover, the fact that the emission time constant extracted from R_{ON}-transients is affected by the applied $V_{DS,str}$, could explain way the extracted activation energy (i.e., 0.83 eV) differs from the theoretical value expected for C_N states (i.e., 0.9 eV). This can be clearly observed by looking at equation (4.1) since the apparent activation energy depends on the applied field (i.e., on the applied $V_{DS,str}$).

To highlight this effect, we performed the same characterization shown in Fig. 4.3 by increasing the $V_{DS,str}$ voltage to 50 V. The Arrhenius plot extracted in this condition yielded a lower activation energy with respect to the one obtained at $V_{DS,str}$=25 V (see Fig. 4.7).

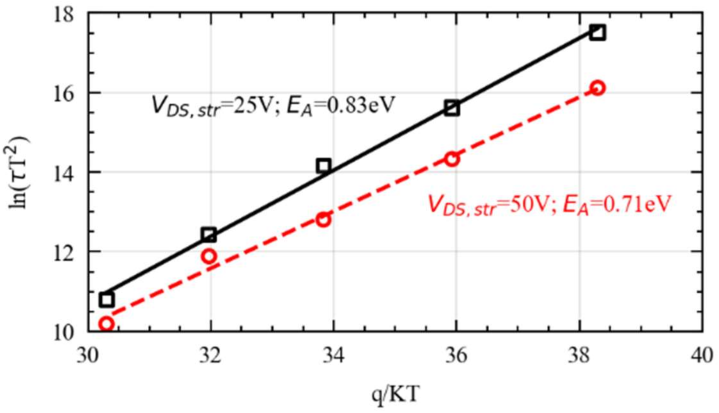

Figure 4.7: Arrhenius plot extracted from experimental R_{ON} transients at $V_{DS,str}$ = 25 V and $V_{DS,str}$ = 50 V.

This is also an important remark for the characterization of deep-levels, since the activation energy extracted from transient measurements could be seriously affected by the applied electric field in case of traps experiencing PFE [26]. This justify the choice of applying a relatively low $V_{DS,str}$ (i.e., 25 V) for extracting the traps activation energy in the previous subsection.

4.3.2 Partial recovery of dynamic-R_{ON} vs $V_{DS,str}$

A widely reported – yet not definitely assessed – result in the literature is the non-monotonic dependence of R_{ON} on the adopted off-state drain voltage ($V_{DS,str}$), that has indeed been observed in different AlGaN/GaN power HEMT technologies [12-16, 18, 27]. Some of these literature data are collected and shown in Fig. 4.8.

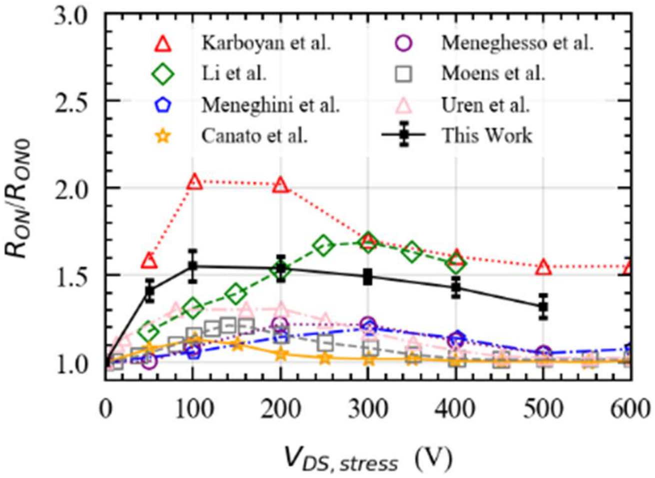

Figure 4.8: Dynamic R_{ON} vs $V_{DS,str}$ data found in the literature [12-16, 18-27] and obtained from our measurements (see legend). The partial recovery behavior is observed on different GaN power HEMT technologies.

While dynamic R_{ON} degradation is generally attributed to dispersion effects due to buffer traps, different interpretations for the observed partial recovery have been proposed:

(i) balancing of negative and positive buffer charge storage [28, 29] induced by leakage paths between the 2DEG and the carbon-doped buffer (either accounted for through heavily p-doped shorts [13, 14, 30] or band-to-band hopping transport [31]);

(ii) generation of positive charge by ionization of donor traps in the UID GaN channel layer [31];

(iii) charge redistribution within the structure due to increasing vertical drain-to-substrate leakage [32];

(iv) positive charge storage at the interface between the carbon-doped buffer and the strain-relief layers/nucleation layer due to the neutralization of ionized acceptors or to ionization of donors [14, 18, 29-31].

Nonetheless, a consistent and quantitative interpretation for the observed partial recovery of dynamic R_{ON} is still lacking.

To quantitatively interpret the observed non-monotonic dynamic R_{ON} behavior shown in Fig. 4.8, we performed 2D simulations. To mimic measurement conditions, stress was held for 1000 s at each $V_{DS,str}$ bias and then R_{ON} was evaluated after performing a fast sweep to bias the device in its triode region (V_{GS}=6 V; V_{DS}=0.5 V). Simulation results are shown in Fig. 4.9 along with measurement data points.

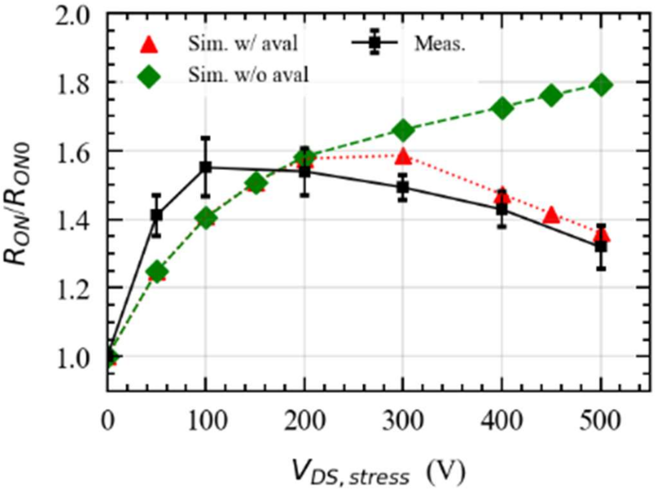

Figure 4.9: Comparison between simulated and measured dynamic R_{ON} vs $V_{DS,str}$ (see legend). Simulations were carried out with and without Impact Ionization in order to put in evidence the role of avalanche generation on the non-monotonic dynamic-R_{ON} trend.

The simulations are consistent with the observed dynamic R_{ON} decrease that occurs for $V_{DS,str} \geq 300$ V (see Fig. 4.9). Interestingly, this behavior can be accounted for by the simulations only when including avalanche generation due to impact ionization, as it can be observed by comparing the blue squares with orange diamonds in Fig. 4.9. This occurs because of the partial neutralization of negatively charged acceptors in the buffer (i.e., N_{ACC}^{-}) by impact-ionization generated holes that get trapped by these states. The partial reduction of the negatively charged traps increases the 2DEG concentration in the access region, giving rise to the observed R_{ON} reduction. Conversely, when there is no impact ionization activated in the simulations, then the ionized traps keep increasing hence impeding the partial R_{ON} recovery (see Fig. 4.9). The case without impact ionization active proves the necessity of a hole generation mechanism to reduce R_{ON} dispersion. Incidentally, we observe that the reduction of the negative charge in the gate-drain access region due to hole injection as the origin for improved R_{ON} dispersion was experimentally demonstrated in [33], further validating our interpretation.

4.4 Carbon doping Effect on 100 V AlGaN/GaN HEMTs

The results reported so far are related to 650 V GaN technology. Nevertheless, GaN devices have the potential to replace Silicon transistors even for power applications featuring lower operative voltages (i.e., between 50 V and 200 V). In this voltage range, Silicon Carbide is less competitive, giving more space to GaN technology to lead the market. Nevertheless, the increased costs related to GaN production compared to Silicon, yields the need to provide significant benefits in terms of power and efficiency to make GaN the preferred choice. Accordingly, it is important to have devices presenting low specific R_{ON} values and acceptable dynamic-R_{ON}. As already pointed out in the previous section, holes emitted by C-related traps within the gate-drain access region when the device is in the off state, can lead to an increase in the density of negatively ionized C_N acceptors, that results in an increased R_{ON} when the device is set back to on-state [5]. Moreover, traps located below the Gate terminal, could yield positive V_{TH} drifts in the DUT, which would result in a reduced overdrive voltage (V_{GS}-V_{TH}) for a given driving V_{GS} [34]. These detrimental effects could be more evident for GaN devices operating between 50 V and 200 V, since it is in this voltage range that the largest degradations have been observed [5]. Moreover, it is important to verify if the mechanism responsible for parameters drifts in 100 V GaN devices is the same occurring in 650 V samples (i.e., Buffer-related or Surface-related trapping).

With this in mind, we report a set of measurements that can be used to clearly identify the role of Carbon traps on the parameters dynamics. To do so, we compare the results obtained on 100V GaN-based devices presenting equivalent epitaxial structures but different Carbon doping in the GaN buffer layer.

4.4.1 Tested Devices

Devices Under Test (DUTs) were AlGaN/GaN HEMTs grown on Silicon substrate. Normally-off operation was obtained by means of a p-GaN gate structure presenting grown on top of the AlGaN barrier. GaN Buffer was Carbon (C) doped to obtain a semi-insulating layer and increase the blocking voltage [6]. Particularly, devices with different Carbon concentrations have been considered, labelled as Buffer A and Buffer B. The gate width was 0.4 µm, while the gate length (L_G) was less than 1 µm. The source-gate and gate-drain distance were < 1 µm and < 2 µm, respectively. A schematic cross section of the device is reported in Fig. 4.10.

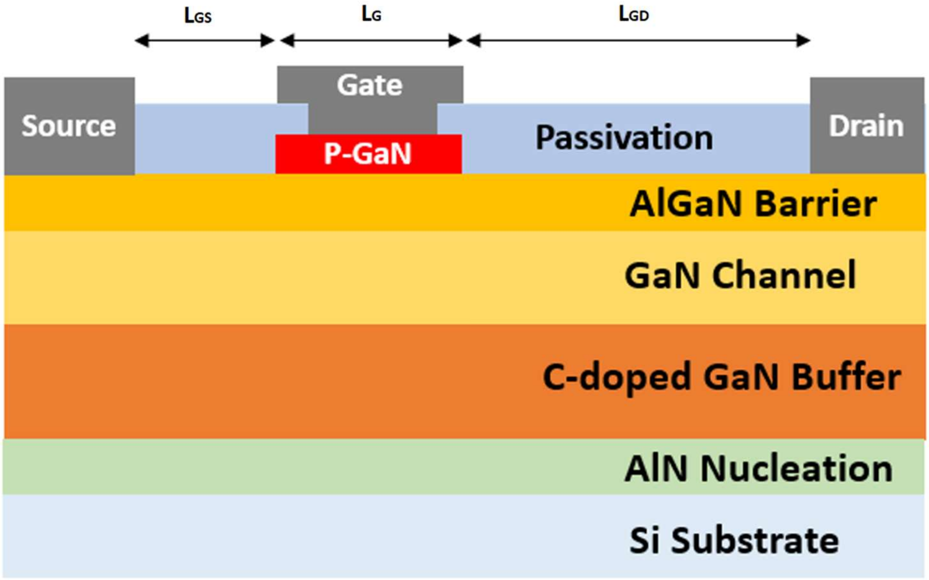

Figure 4.10: Schematic cross section of the GaN-based HEMT tested in this study.

4.4.2 Vertical isolation

Firstly, vertical leakage measurements on the test structure shown in Fig. 4.11(a) were performed to highlight the insulating properties of the vertical stack. The voltage applied on the top contact was swept between 0 V and 200 V, allowing to reconstruct the I-V leakage curves shown in Fig. 4.11 (b).

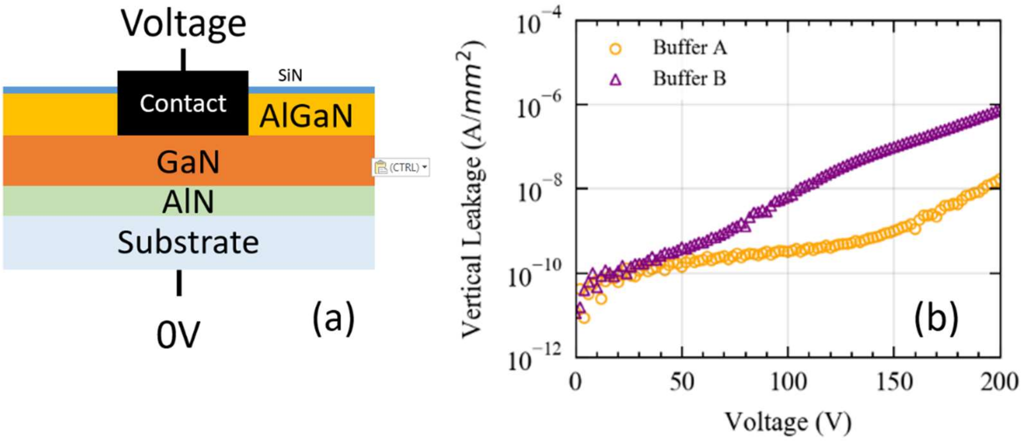

Figure 4.11: (a) Structure used to evaluate the vertical isolation (i.e., vertical leakage across the epitaxy). The substrate is grounded, while the voltage was applied on the top metal contact at increasing potential level for reconstructing the I-V leakage characteristics. The top contact was totally recessed to eliminate the 2DEG contribution on the measurement. (b) Typical Vertical leakage (I-V) characteristics measured at 25°C for Buffer A and Buffer B devices

Buffer B samples showed a larger vertical leakage with respect to Buffer A, stemming for the presence of a reduced acceptor concentration in the C-doped GaN layer Accordingly, if the dynamics of Carbon acceptors in the Buffer affects the V_{TH} and R_{ON} stability, different effects should be observed on Type A and Type B samples.

4.4.3 Buffer stability

To carry out a preliminary study on the buffer stability, the Transmission Line Measurement (TLM) structures shown in Fig. 4.12 were employed. Particularly, Back-bias stress tests were performed on both buffer types, monitoring the current between 5 µm spaced pads over several time decades. The measurement is rather simple: a 100 mV potential difference is applied between the two pads of the TLM structure in order to measure the current. A negative substrate voltage (V_{SUB}) is applied to the structure in order to induce trapping/de-trapping dynamics in the buffer. The 2DEG conductivity is monitored during the stress-phase for several time decades (e.g., between 10^{-2} to 10^{3} s) in order to get informations on the traps dynamics.

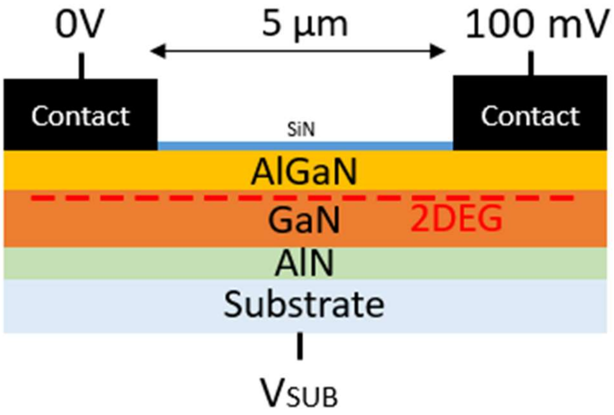

Figure 4.12: Transmission Line Measurement (TLM) structure used to evaluate the Buffer stability. P-GaN layer was removed to allow the formation of the 2DEG at the AlGaN/GaN interface. A substrate voltage (V_{SUB}) is applied to structure's back, while a 100 mV potential is forced between pads to monitor the current during stress.

Fig. 4.13 reports the current transients measured with V_{SUB} = -50 V. Acquired curves show an exponential decreasing trend, being signature of trapping/de-trapping dynamics.

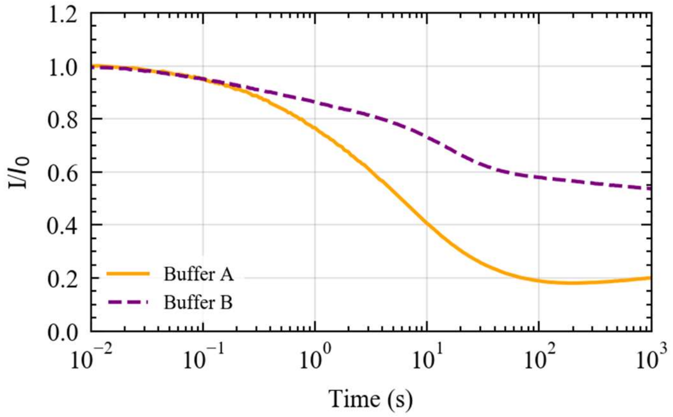

Figure 4.13: Current (I) transients acquired under substrate bias stress on TLM for Buffer A and Buffer B, considering V_{SUB} = -50 V (Temperature was set to 25 °C). Current values are normalized with respect to (w.r.t.) the current level measured at the beginning of the transient (I_o).

Different transient's amplitudes were observed for Buffer A and Buffer B, indicating a significant impact of the buffer doping on the amount of degradation. Accordingly, the dynamic decrease in the channel conductivity can be ascribed to the emission of holes from C-related traps, yielding a negative charge build-up in the buffer that partially depletes the 2-Dimensional

Electron Gas (2DEG). This hypothesis is confirmed by Fig. 4.14 in which measurements performed at different temperatures (T) show a speed-up in the transients at increasing T, coherently with a thermally activated process like hole emission form C_N states [5].

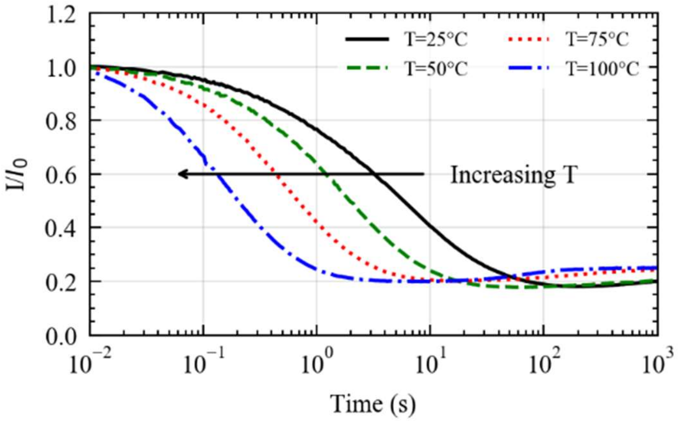

Figure 4.14: I/Io current transients acquired on TLM structures at different base-plate temperatures (i.e., between 25 °C and 100 °C). Reported data refers to Buffer A with V_{SUB}=-50 V. The current transients speed up at increasing temperature, coherently with the dynamics expect for hole emission from C_N states.

Results shown so far put in evidence the role of the Carbon doping on the buffer stability. However, these tests have been performed on simplified structures like TLM, while it is more important to evaluate the performances of the ultimate transistor. To perform this measurement on the actual DUTs, two different tests are considered as schematically depicted in Fig. 4.15.

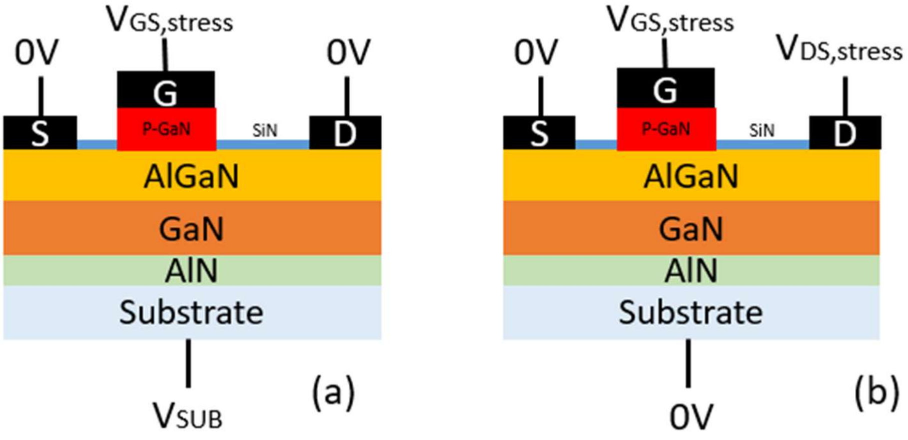

Figure 4.15: Schematic representation of (a) Negative substrate bias stress and (b) Off-state stress with grounded substrate setups. Both test method can be used to evaluate dynamic-R_{ON} on gated transistors.

Negative substrate bias stress (see Fig. 4.15(a)) allows to induce only buffer-related charging/discharging mechanisms, whereas off-state stress with grounded substrate (see Fig. 4.15(b)) allows to induce both buffer-related and surface-related trap effects [2]. To perform these two characterizations, a pulsed measurement is required to switch the DUT between the off-state stress condition and the on-state condition (during which R_{ON} is extracted). This is done by conventional characterization methods, mainly focusing on single point R_{ON} acquisition. However, it is important to monitor the drift of the complete I_D-V_{GS} characteristics, to verify if the current collapse induced by the applied stress is only related to trapping/de-trapping mechanisms in the gate-drain access region or it is also accompanied by positive V_{TH} drifts. The waveforms and measurement sequence employed for the characterization are sketched in Fig. 4.16.

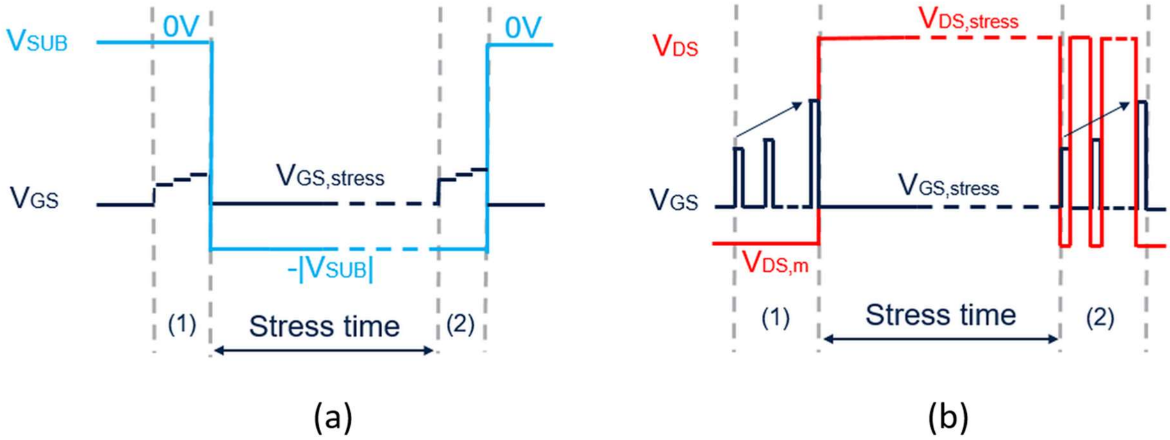

Figure 4.16: Measurement waveforms employed under (a) negative substrate bias stress and (b) off-state stress with grounded substrate.

Figure 4.16(a) reports the waveforms used for performing negative substrate bias stress on gated transistors. The stress measurement sequence is as follows: (1) The Fresh I_D-V_{GS} characteristic is reconstructed by means of a stair-like gate signal (V_{GS} from 0 V to 6 V, V_{DS} =0.5 V). Then, a 1000 s stress is performed at (V_{DS}=0 V, $V_{GS,stress}$= -2 V and V_{SUB}=-50 V). This time is sufficient to guarantee a complete emission for C-related traps [5]. (2) V_{DS} is set back to 0.5 V and the gate voltage is staired again to capture the I_D-V_{GS} characteristics after the stress.

Figure 4.16(b) shows the waveforms used for performing off-state stress measurement. The stress measurement sequence follows a similar approach to the one employed for back-bias stress. (1) The Fresh I_D-V_{GS} characteristic is reconstructed by means of a sequence of gate pulses from 0 V and 6 V with $V_{DS,meas}$=0.5 V. A 1000 s stress is then performed at V_{DS}=$V_{DS,stress}$, $V_{GS,stress}$=0 V, while V_{SUB} = 0 V. (2) Gate voltage is pulsed again to capture the I_D-V_{GS} after the stress. To limit parameters recovery, the V_{DS} is briefly pulsed to $V_{DS,m}$ with short (2 µs) on state time intervals separated by 100 µs off-state biasing. During this off-state time, the off-state stress voltage ($V_{DS,stress}$) is still applied to the DUT.

Fig. 4.17 reports the results obtained under negative bias stress on Buffer A and Buffer B.

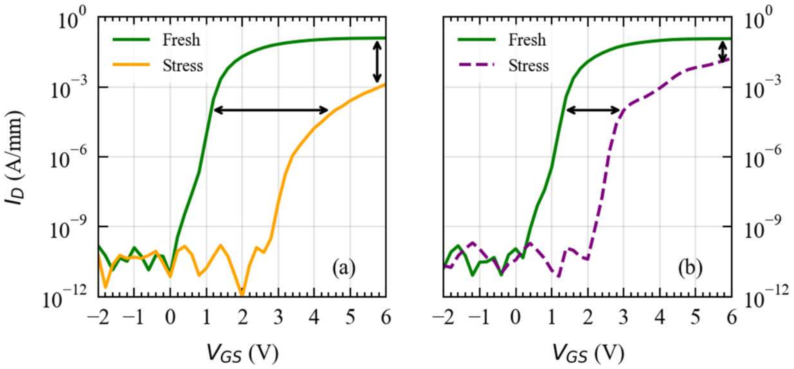

Figure 4.17: Typical results obtained after 1000 s of stress time performed under negative substrate bias stress (with V_{SUB} = -50 V) for (a)Buffer A and (b) Buffer B devices.

After 1000 s stress time, Buffer B showed a lower drift in the I_D-V_{GS} characteristics, indicating a reduced buffer traps contribution. This result is coherent with the reduced degradation observed on TLM structure. The observed behavior suggests that buffer traps located under the gate and in the gate-drain access region severely impact the dynamics of the DUT [4]. A similar effect was obtained under off-state drain voltage stress conditions (see Fig. 4.18), indicating that the degradation induced by the applied $V_{DS,stress}$ was still dominated by buffer traps' dynamics.

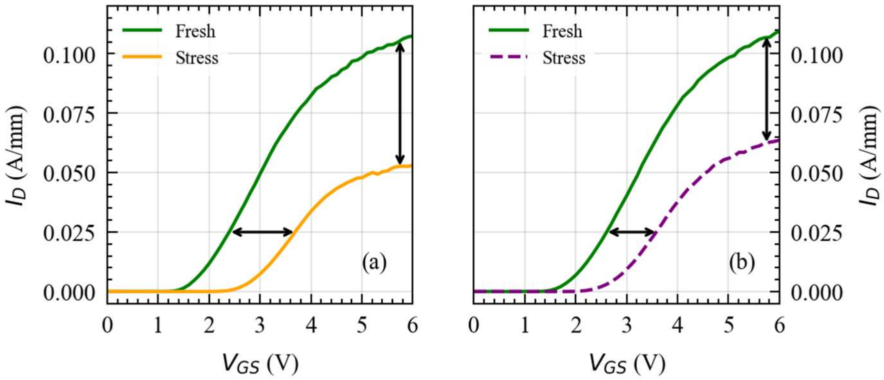

Figure 4.18: Typical results obtained after 1000 s of stress time performed under off-state stress with grounded substrate (with $V_{DS,stress}$ = 50 V) for (a) Buffer A and (b) Buffer B devices. We see a similar trend for both V_{TH} and R_{ON} w.r.t. the one observed under back-bias stress with negative substrate. This suggests a significant buffer-traps contribution even under conventional off-state stress conditions.

The measurement was performed on several samples yielding the distribution in the dynamic-R_{ON} reported in Fig. 4.19, in which a different Carbon doping in the buffer yielded a significant difference in the R_{ON} drift.

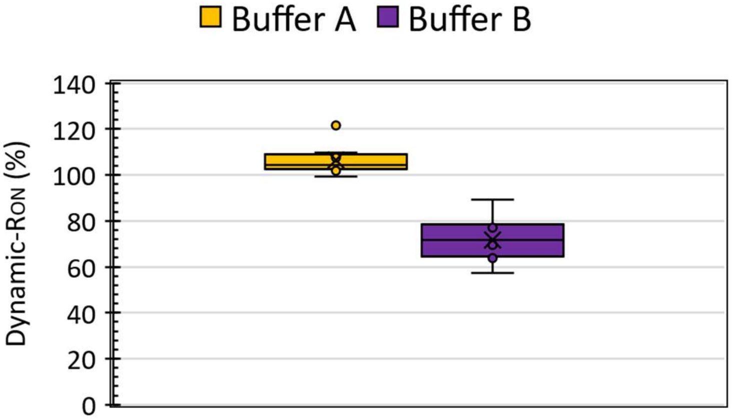

Figure 4.19: Box-plots referring to the dynamic-R_{ON} results (in percentage) obtained under off-state stress conditions on Buffer A and Buffer B devices. 10 devices have been tested for each buffer type to check the results variability.

It is important to notice that the best dynamic performances were observed on the samples presenting an increased leakage. This put in evidence a clear trade-off between dynamic performances and leakage in GaN HEMTs featuring a C-doped buffer.

4.5 Parameters drifts evaluated with AMCAD 200 PIV System

In the previous section, we have pointed out the possible role of buffer traps on the dynamic-R_{ON} of 100 V GaN HEMTs devices. Nevertheless, devices have been tested under off-state stress condition, in which a static large drain voltage is applied for a relatively long time to the device under test. This conditions is able to induce trapping/de-trapping in the DUTs, but is not the actual condition that devices will face in a power converter circuit. In order to properly characterize the device behaviour, it is important to monitor the parameters evolution in an application-like condition. Considering a conventional power switching converter application, the device is normally pulsed between on-state to off-state condition and the voltage applied in off-state depends on the operative voltage of the converter. In this study, we consider devices operating at V_{DS}=50 V.

4.5.1 Tested Devices and Characterization Tool

Devices Under Test (DUTs) were AlGaN/GaN HEMTs grown on Silicon substrate. A p-GaN gate was grown on top of the AlGaN barrier to obtain normally-off devices. GaN Buffer was Carbon (C) doped to obtain a semi-insulating layer with a nominal carbon concentration in the order of 10^{19} cm^{-3}. The gate width was 0.4 µm, while the gate length was <1 µm. Similarly to the devices tested in the previous section, the source-gate and gate-drain distance were <1 µm and <2 µm, respectively (see Fig. 4.10). Prior to passivation of the AlGaN surface, two different surface treatments were considered, herby named as Type A and Type B, whose experimental results are shown in the following.

As already mentioned, tested devices normally operate under pulse-mode conditions. It is thus important to characterize the DUT with a Pulsed IV (PIV) characterization technique. To this end, the AMCAD 200 Pulsed IV tool was employed. This pulsed system enables the usage of extremely short pulses, thus allowing to mimic the pulses that the devices experience in real applications. A picture of the measurement tool employed is shown in Fig. 4.20.

Figure 4.20: Picture of the AMCAD 200 Pulsed IV system used for the characterization.

As already discussed in the previous sections, for devices presenting a Carbon-doped buffer layer, holes can be potentially emitted by C-related traps within the gate-drain access region when the device is in the off state, yielding an increase in the negatively ionized C_N acceptors, and therefore to an increased R_{ON} when the device is set back to on-state [5]. Moreover, traps located under the gate, could enlarge the experience current reduction, due to a positive drift of the threshold voltage [34]. These effects already show up under Soft-Switching conditions in which the device is turned ON/OFF at 0 V drain voltage. Nevertheless, this represent just a relaxed scenario since devices may be driven under more severe Hard-Switching conditions, in which the simultaneous presence of high voltage and high current during transitions can result in additional degradations due to self-heating and/or hot electrons effects [35]. Accordingly, it is extremely important to study both operative conditions to have a more complete picture of the device behaviour.

4.5.2 Stress/Measurement Conditions

In a conventional characterization scheme, the device is kept in a quiescent off-state stress condition and then, after a predefined time interval, it is biased in on state to measure the R_{ON}

and evaluate the parameter degradation. Clearly, this kind of method is not able to capture the drift of the device threshold voltage (V_{TH}), since the single point measurement is typically performed for a single V_{GS} level. However, it could be interesting to monitor the drift of the complete I_D-V_{GS} characteristics, to verify if the current collapse induced by the applied stress is only related to trapping/de-trapping mechanisms located in the gate-drain access region or it is also related to charging/discharging effects below the gate terminal (yielding a positive V_{TH} drift). To this end, a stress/measurement sequence following the same idea of the one presented in Fig. 4.16(b) was implemented with the AMCAD 200 PIV system, see Fig 4.21.

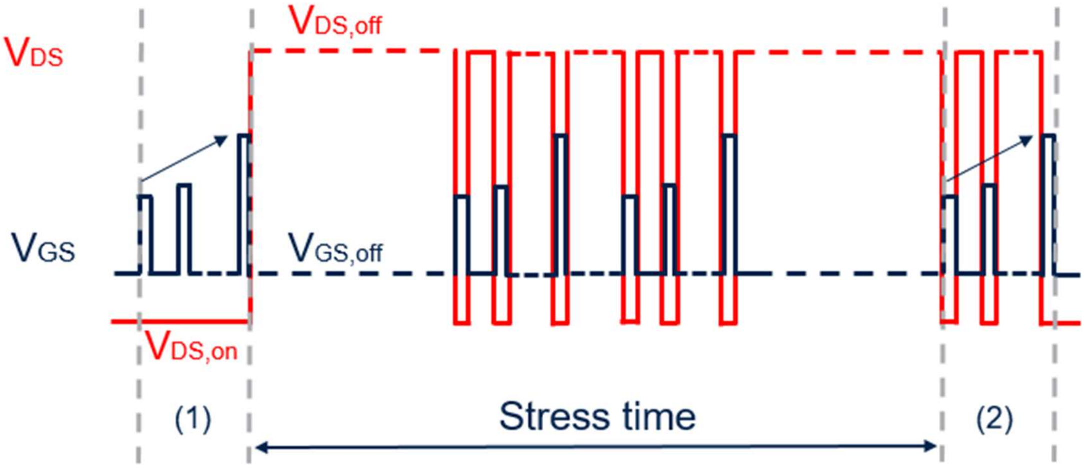

Figure 4.21: Stress/measurement sequence implemented with the AM200 PIV system.

Before starting the stress phase (1) the fresh I_D-V_{GS} characteristic is reconstructed by means of a sequence of gate pulses ranging from 0 V and 6 V with 0.1 V steps, while the device's V_{DS} is at $V_{DS,on}$=0.5 V. Then, a 1000 s stress is performed at V_{DS}=$V_{DS,off}$, $V_{GS,off}$=0 V. During the stress, the device is periodically turned on with a 100 µs switching period and 2% duty cycle in order to mimic a conventional switch mode operation. Moreover, since the same V_{GS} pulse sequence is applied even during the stress phase, the evolution of the I_D-V_{GS} characteristics can be potentially monitored, provided that the time required for the reconstruction of the complete transfer curve is not comparable with the stress time. After the stress (2), the gate voltage is pulsed again to capture the I_D-V_{GS} characteristics after the stress. To limit the parameters recovery, the drain voltage is briefly pulsed to V_{DS}=$V_{DS,on}$ with short (2 µs) on state time intervals separated by 100 µs off-state biasing. During this off-state time, the off-state stress voltage ($V_{DS,off}$) is still applied to the DUT.

It is important to notice that the chosen stress time must be long enough to evaluate a steady state degradation of the parameters of interest. Particularly, since traps in the Buffer could take several tens of seconds to reach equilibrium [5], the stress time chosen (i.e, 1000 s) is a good option for evaluating the complete degradation potentially induced by the stress conditions applied. This is coherent with time constant of the dynamic-R_{ON} transients reported in Section 4.2.

4.5.3 Experimental Results

The stress/measurement sequence just described was then used to characterize Type A and Type B devices, whose experimental results obtained with $V_{GS,off}$=0 V and $V_{DS,off}$=50 V are shown in Figure 4.22.

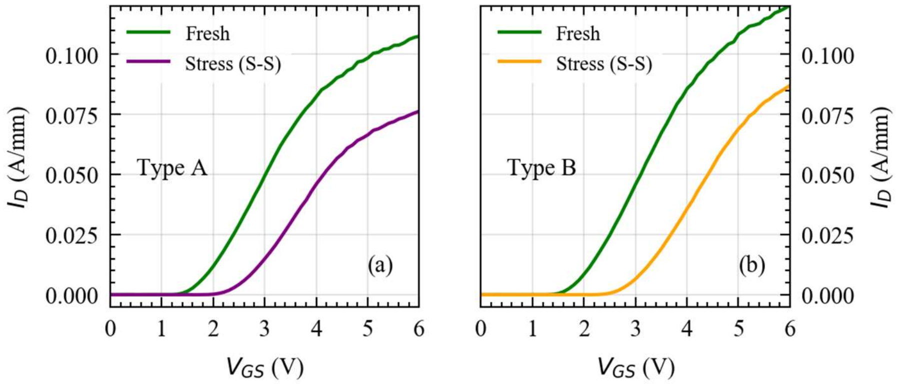

Figure 4.22: Comparison between I_D-V_{GS} characteristics obtained on fresh devices and after 1000 s stress at $V_{GS,off}$=0 V and $V_{DS,off}$=50 V under Soft-Switching (S-S) mode for both (a) Type A and (b) Type B devices.

Similar results have been obtained for Type-A and Type-B devices under Soft-Switching mode operation. This result is consistent with the hypothesis that, under Soft-Switching conditions, Buffer traps are the main responsible for R_{ON}-degradation. In fact, both Type A and Type B devices featured the same Buffer layer design, while presenting a different surface treatment. This suggests that the different surface treatments employed does not significantly affect the dynamic-R_{ON} under off-state stress conditions if Soft-Switching mode is considered. Nevertheless, the role of surface traps may be more evident under Hard-Switching mode, in which hot-electrons may come into play.

While off-state stress conditions under Soft-switching mode operation can provide interesting information on the degradation induced by Buffer-related traps, the Hard-Switching mode operation is closer to the conditions encountered in real applications and could be source for additional degradations. According to this observation, it is important to compare the results obtained for these two different operative conditions to investigate the impact of transitions on the parameters drift. To this end, the stress/measurement waveforms reported in Fig. 4.23 were considered.

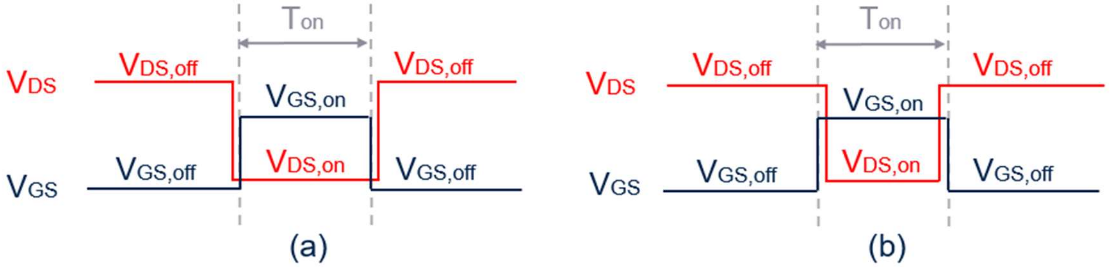

Figure 4.23: Waveforms corresponding to (i) Soft-Switching mode (i.e., in which the DUT is turned ON/OFF ant 0 V drain voltage) and (ii) Hard-Switching mode (i.e., in which the DUT is turned ON/OFF at $V_{DS}=V_{DS,stress}$).

In Fig. 4.23 we reported the V_{DS} and V_{GS} waveforms employed for pulsing the device under test between the off-state stress conditions and the on-state measurement one. In Fig. 4.23(a) the waveforms referring to Soft-Switching mode operation are reported. In this case, the high/low and low/high drain voltage transitions are performed at zero current. Conversely, the Hard-Switching mode operation is simulated by overlapping the gate turn-off and gate turn-on edges with the drain voltage edges (see Fig. 4.23(b)), yielding a non-null time interval during which the device experiences high voltages and high current at the same time. Both measurements are performed by continuously switching the device ON and OFF with a 100 µs switching period with a 2% duty cycle. The Stress/Measurement is performed for 1000 s and the I_D-V_{GS} are acquired at the beginning and at the end of the stress phase, coherently with the waveforms shown in Fig. 4.21. The results obtained on tested devices for Hard-Switching mode are reported in Fig. 4.24.

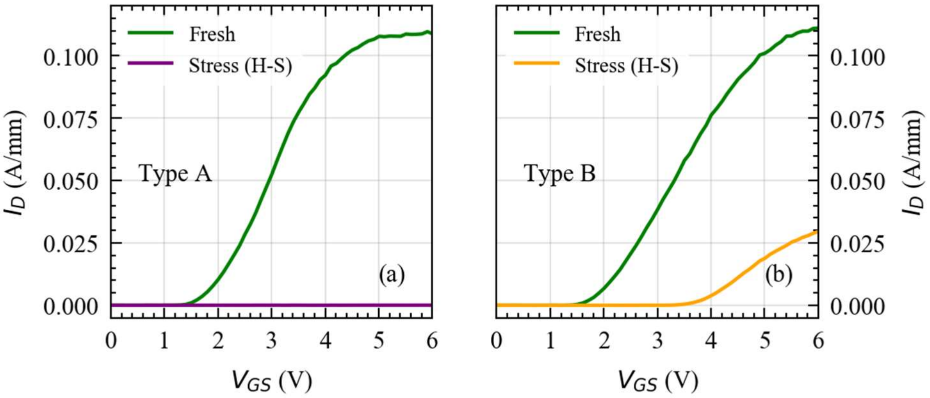

Figure 4.24: Comparison between I_D-V_{GS} characteristics obtained on fresh devices and after 1000 s stress at $V_{GS,off}$=0 V and $V_{DS,off}$=50 V under Hard-Switching (H-S) mode for both (a) Type A and (b) Type B devices.

Looking at Fig. 4.24, we can clearly see that the results obtained under Hard-Switching conditions present a larger degradation on both V_{TH} and R_{ON} parameters. This means that the presence of transitions performed at relatively high voltage and current levels introduces additional drifts that could be due to several mechanisms. As a relevant hypothesis, the simultaneous presence of a non-null current flow at high electric fields that is experienced during HS transitions could yield hot carriers effect in the DUT, justifying the additional degradation observed in this operative mode [35]. Particularly, a different behavior has been observed for Type A and Type B devices. In fact, Type A device presented a completely collapsed current after 1000 s stress, stemming for a more pronounced degradation with respect to Type B device. It is important to notice that the trapping of hot electrons could take place at the device surface and/or in the buffer layer, making it difficult to clearly state which layer is the responsible for these additional drifts. Nevertheless, the fact that different behaviors have been observed for Type A and Type B devices, suggests the involvement of hot electros trapping/de-trapping at the device's surface. In order to verify this hypothesis, a different measurement approach should be considered, in order to induce just the hot electrons contribution and clearly identify the origin of the observed degradation.

4.6 Alternative Approach for Hot-Electrons characterization

It is generally difficult to separate hot-electron effects from off-state trapping/de-trapping mechanisms and the realization of custom measurement setups is typically employed for this scope [36]. In [37] a resistive load setup with a capacitance connected in parallel to the device under test (DUT) has been used to simulate the hard-switching I-V trajectory, while in [38] a current limiting circuit was employed to govern the off/on transitions when the DUT is turned on at high drain voltages. Both approaches allow to induce hot electrons effect during switch mode operations, but requires relative complex setups to be implemented. Another approach consists in the usage of a commercial Pulsed IV system like the one described in the previous section. However, Pulsed IV systems are quite expensive and are not always available in small research centers and university laboratories.

In this Section, we propose an alternative approach to study hot electron effects, exploiting a commercially available parameter analyzer. In fact, hot electron effects can be in principle studied through relatively fast on-state stress tests, since the trapping of hot electrons requires very short times to occur [39]. This can be done by simply applying a relatively high drain voltage in on state for a short time interval. This allows to prevent the appearance of self-heating effects and the dynamic R_{ON}-increase due to off-state stress conditions, that have been reported to take several tens of seconds to reach equilibrium [2, 5]. Accordingly, this would induce only hot carriers trapping on tested devices, without introducing additional stress that could yield misleading results. Nevertheless, this trapping mechanisms could take place both in the GaN buffer and at the device surface [38], suggesting the importance to discern these two contributions to correctly study the underlying physics. To this end, the parameter recovery after stress is considered, since the emission/capture from buffer and surface traps should present different dynamics [2]. Moreover, to better identify the role of surface trapping on the observed degradation, we consider the same Type A and Type B devices considered in the previous section, i.e., featuring the same buffer design and two different surface treatments.

4.6.1 Measurement Technique

To study hot-carriers' effects during on-state stress conditions, the B1505a parameter analyzer was employed. The measurement sequence implemented is schematically depicted in Fig. 4.25.

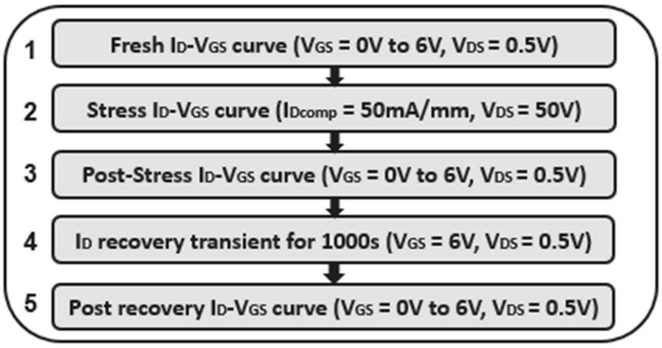

Figure 4.25: Measurement sequence to be applied for the evaluation of power-devices degradation under on-state stress conditions.

The measurement consists of five main steps:

1) Initially, the fresh I_D-V_{GS} curve of the DUT is measured to set a reference starting point for the device's parameters. To this end, V_{DS} is kept at 0.5 V, while V_{GS} is swept from 0 V to 6 V to get the information on both V_{TH} and R_{ON};
2) The on-state stress is performed by reconstructing a fast I_D-V_{GS} curve at V_{DS}=50 V. Particularly, the V_{GS} is fast increased from 0 V till a limit V_{GS} for which the chosen current compliance (e.g., 50 mA/mm) is reached;
3) The post stress I_D-V_{GS} is acquired at V_{DS}=0.5 V, while V_{GS} is swept from 0 V to 6 V to capture the hot electrons degradations;
4) The drain current is monitored for 1000 s with V_{DS}=0.5 V and V_{GS}= 6 V in order to measure the current recovery over several time decades with logarithmically spaced samples;
5) The I_D-V_{GS} curve after 1000 s recovery time is reconstructed at V_{DS}= 0.5 V to get an indication on the retained degradation. In fact, the dynamics of traps in the GaN buffer layer should present time constants shorter than 1000 s [5] thus allowing to discern the buffer contribution from the one associated to different regions.

An example of the curves acquired by the setup is reported in Fig. 4.26.

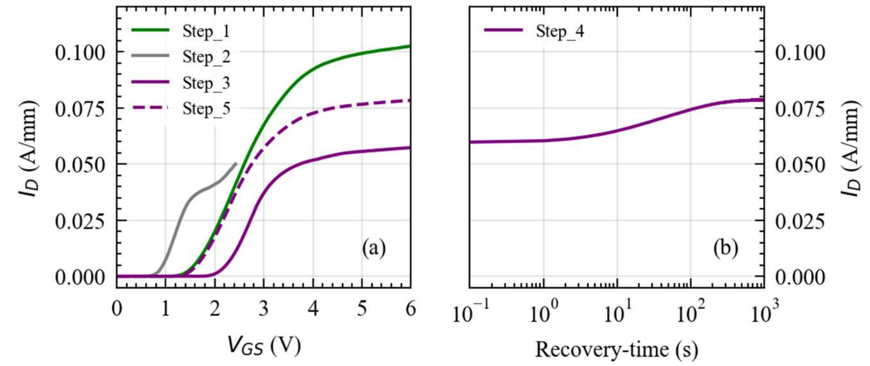

Figure 4.26: Curves measured on tested devices during the different steps of the measurement procedure. (a) I_D-V_{GS} curves captured during Steps 1-3 and Step_5; (b) current recovery transient measured during Step_4.

The I_D-V_{GS} measured at V_{DS}=50 V during Step_2 allows to emulate on-state stress conditions and induce the trapping of hot electrons. The curve reconstructed during this step present reduced V_{TH} with respect to the fresh one. This effect could be explained by the Drain-Induced Barrier Lowering (DIBL) effect [39] that could appear when short channel devices are subjected to large drain voltages. When the current compliance is reached, the on-state stress is removed and the post-stress I_D-V_{GS} is measured, showing a positively shifted V_{TH} and a reduced triode current. This indicates the presence of hot electrons trapping under the gate terminal and in the gate-drain access region. The I_D-recovery transients monitored in the following 1000 s allows to capture the dynamics of traps in the buffer layer which should present time constants in the order of several tens of seconds at 25 °C [5]. After this recovery time, the I_D-V_{GS} measured during Step 5 shows a completely recovered V_{TH}, indicating that trapped electrons below the gate terminal presents time constants shorter than 1000 s. Conversely, the trapping that occurred in the gate-drain access region can be only partially recovered after 1000 s and the fact that the current transient saturates after 1000 s suggests the presence of two different mechanisms affecting the R_{ON}-degradation, whose contributions can be discerned by the proposed measurement.

4.6.2 Surface Treatment Effect

The results obtained on devices featuring different surface treatments are shown in Fig. 4.27.

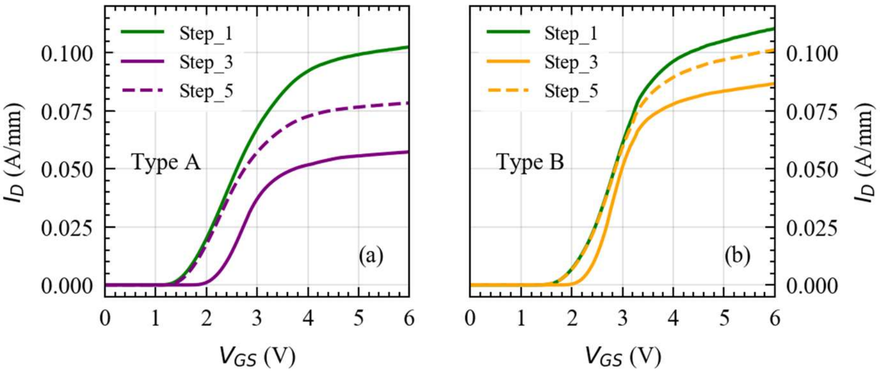

Figure 4.27: Comparison between the experimental results obtained device presenting (a) surface treatment Type A and (b) Type B.

The device featuring Type A treatment showed an evident current collapse and a positive V_{TH} drift after the application of the on-state stress (see Step_3 in Fig. 4.27(a)). On the other hand, the I_D-V_{GS} curve acquired after stress for treatment B showed a reduced parameters degradation. This evidence suggests that part of the degradation could be associated to surface traps. This is further confirmed by the fact that, the degradation retained after 1000 s recovery reduces for Type B devices, stemming for the presence of an optimized surface (see Fig. 4.27(b)). As highlighted previously, this retained degradation affects only the device' R_{ON}, whereas the device's V_{TH} is completely recovered. This suggests that the current reduction which cannot be recovered after 1000 s is due to trapping effect that take place in the gate-drain access region in the passivation layer. The different behaviour observed for Type A and Type B devices is totally coherent with the one previously captured by the Pulsed IV system, meaning the proposed approach is able, at least qualitatively, to get the same informations.

Another important aspect refers to I_D recovery transient monitored during Step_4. In fact, the current transients reported in Fig. 4.28 for the two different surface treatments showed similar time constants and amplitudes. This suggests that the physical mechanism governing the recoverable degradation is the same for both devices. Moreover, the time constant observed is compatible to the one expected for C-related buffer traps in GaN. Particularly, the current reduction associated to this process, could be due to an easier ionization of Carbon acceptors induced by hot electrons [40], that yields a negative charge build-up in the GaN Buffer which depletes the 2DEG. This observation is consistent with the presence of a heavily C-doped Buffer layer featured by the DUTs. According to this hypothesis, the recovery transient observed should be due to the redistribution of holes in the GaN buffer that takes place after the stress-removal [19], which compensates the negative charge previously exposed, thus restoring the 2DEG conductivity. The fact that similar amplitudes are obtained on Type A and Type B devices for the monitored I_D transients is in line with the fact that tested devices shared the same buffer design.

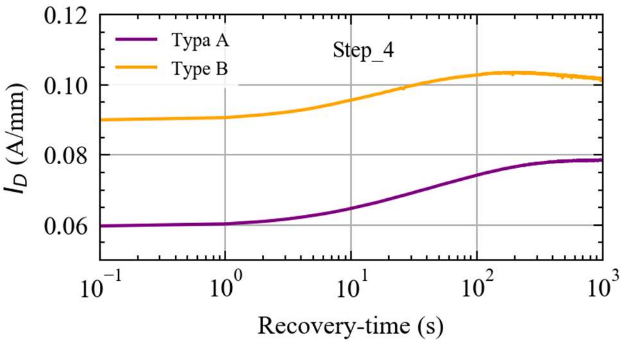

Figure 4.28: Comparison between the I_D recovery transients captured after on-state stress on devices presenting different surface treatments and the same epitaxy structure.

To have a more complete picture of the physical mechanism responsible for the observed degradation, we investigated the effect of the current compliance level set during Step_2.

4.6.3 Current Compliance Effect

The concentration of free charges that can contribute to the on-state degradation is basically set by the current compliance level. In fact, an increase in the current at which the high-voltage stress is performed, increases the probability to generate hot-electrons responsible for current collapse. According to this observation, we performed the same characterization on Type B devices for two different compliance levels (i.e., 50 mA/mm and 110 mA/mm). The results obtained are shown in Fig. 4.29.

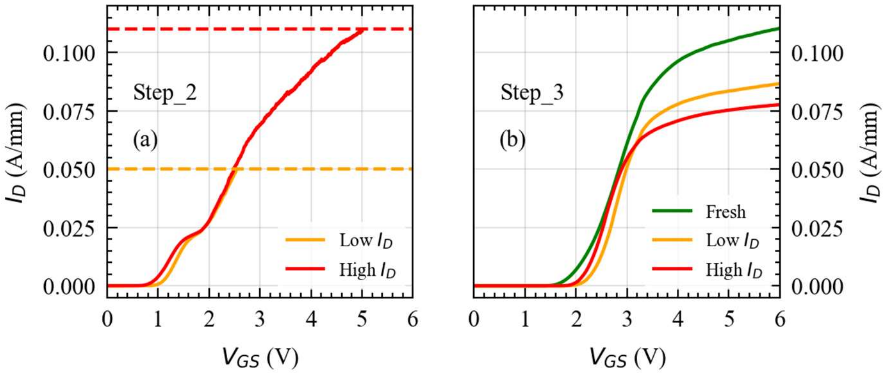

Figure 4.29: (a) I_D-V_{GS} curve acquired during Step_2 by imposing different current compliance levels. (b) impact of the current compliance level on the I_D-V_{GS} curve acquired during Step_3.

The curves reported in Fig. 4.29(b) show that an increase in the current compliance yields in increased degradation induce by the on-state stress. This is coherent with the fact that a higher current level increases the concentration of free carries that can contribute to hot electrons trapping effects. Despite this evidence, the region in which the additional charge trapping is taking place is yet to be identified. An important indication is provided by the current transients reported in Fig. 4.30, in which we represented the current variation monitored during Step_4 for the two different compliances considered. This allows to directly compare the amplitude of the captured I_D-transients.

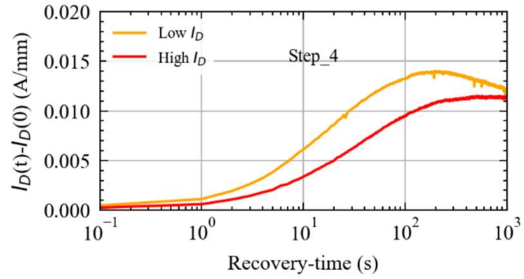

Figure 4.30: Comparison between the current transients measured after on-state stress preformed at different compliances.

As we can see, the transients obtained still presented similar time constants and amplitudes, indicating that an increase in the current density does not affect this degradation process. This is coherent with the interaction of hot electrons with buffer traps, since the trapping in the buffer layer does not require large current levels to be triggered. Conversely, the increased degradation observed in Fig. 4.29(b) at higher compliance could be associated to the capture of hot electrons at the device surface. In fact, the hot carriers' should overcome a large potential barrier in order to be captured in the device's passivation [36] and this makes this process more difficult to occur. Accordingly, an increase in the current level during the high voltage stress increases the probability for the hot electrons to be trapped in this region. This is confirmed by the I_D-V_{GS} curves shown in Fig. 4.31.

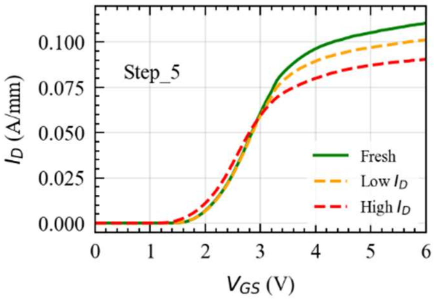

Figure 4.31: Impact of the current compliance level on the I_D-V_{GS} degradation retained 1000 s after the removal of the on-state stress.

The retained degradation captured after 1000 s from the stress removal increases while increasing the current compliance. As previously observed, the contributions related to buffer traps is already recovered after this relaxation time, suggesting that the remaining contribution should be related to a different device's location. Particularly, the fact that this degradation can be difficultly recovered is coherent with the trapping of hot electrons in the passivation, since the trapped carriers must overcome a large potential barrier to be emitted and restore the 2DEG conductivity [36]. This large potential barrier is present for both trapping and emission process, explaining the observed current compliance effect. Moreover, the fact that the retained trapped charge is located in the gate-drain access region, rather than in the whole device length, is totally coherent to the trapping of hot electrons in the passivation. Finally, this retained degradation has been proved to be strongly dependent on the surface treatment, further confirming the involvement of surface-traps.

4.7 Conclusions

In the first part of this chapter, we investigated the dynamic-R_{ON} behaviour in packaged p-gate GaN HEMTs under OFF-state stress conditions. The on-the-fly characterization performed with the custom measurement setup presented in Chapter 2 allowed us to gain insights in the R_{ON} dynamic evolution over time. Particularly, the characterization of the dynamic R_{ON} transients during OFF-state stress (at $V_{DS,str}$=25 V) allowed the extraction of a 0.83 eV activation energy that correlates well with a dominant hole trap related to C doping in the device buffer. Based on this result, the increase in the dynamic R_{ON} over its static value has to be attributed to hole de-trapping from these buffer traps within the gate-drain access region during the OFF-state phase of the pulse-mode tests. Moreover, electrical characterization of transients taken at different drain stress bias ($V_{DS,str}$) revealed two interesting effects: (i) a square-root dependence of the extracted time constants of the dynamic R_{ON} transients on $V_{DS,str}$, which is signature of PFE; (ii) a non-monotonic dynamic R_{ON} behavior with increasing OFF-state stress bias that was already observed in literature for AlGaN/GaN power HEMTs. For the latter, we observed that the R_{ON} recovery at large drain stress bias finds a straightforward interpretation by assuming that holes generated by a high electric field mechanism partially neutralize the negatively ionized acceptors. This explanation was supported by 2D numerical simulations that consistently reproduced the dynamic R_{ON} decrease for the explored $V_{DS,str}$ range only when including hole generation due to impact ionization. Consistently with this explanation, simulations predicted a monotonic dynamic R_{ON} increase without the hole generation mechanism (i.e., impact ionization) as a consequence of the increasing negatively ionized acceptors in the buffer, thus proving the necessity of a holes generation mechanism to reproduce dynamic R_{ON} reduction observed in the experiments. In the second part of the chapter, we addressed the characterization of GaN-based HEMTs operating at lower voltage levels. Firstly, the role of Carbon doping on the dynamics of tested devices was put in evidence, highlighting a clear trade-off between parameters stability and leakage. Then, the R_{ON}-degradation on 100 V samples was measured by means of Pulsed IV characterization under both Soft- and Hard-Switching mode on devices featuring different surface treatments, but the same Buffer design.

Similar results have been obtained under soft-switching conditions, whereas a significant difference was observed in Hard-Switching among the different devices tested. This suggested the involvement of hot carriers interacting with surface traps. To gain insights in the observed behaviour, an alternative measurement approach for the study of hot electrons in AlGaN/GaN power HEMTs was successfully proposed. The effect of the two different surface treatments on the current degradation was put in evidence, confirming the trends observed under Pulsed IV measurements. Moreover, the effect of the current level employed during the on-state stress was investigated, further confirming the trapping of hot electrons in the passivation as an important contribution to the observed R_{ON} increase.

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5 Study of Fe-related Buffer traps in GaN

As already mentioned, acceptor dopants are commonly introduced in the GaN Buffer layer to reduce the leakage current and increase the breakdown voltage [1]. In the previous Chapter, we already discussed the role of Carbon dopants and the main issues related to their introduction in GaN-based HEMTs for power application. However, Carbon dopants do not represent the only possible solution to increase the breakdown voltage in GaN-based devices. In fact, iron (Fe) dopants are generally adopted in GaN-based transistors for RF applications [2] to obtain semi-insulating buffer layers and increase the blocking voltage [1]. In this section, we focus on this alternative solution, reporting the main issues related to this kind of dopants.

5.1 Time-dependent V_{BR}

An important aspect that should be considered while speaking about Fe-doped GaN HEMTs is the so called time-dependent breakdown voltage (V_{BR}) [3]. In fact, Fe-dopants introduce deep acceptor traps in the bandgap whose occupancy is time dependent [4, 5] and could thus modify the buffer resistivity and electric field profile over time. In turn, this could yield time-dependent V_{BR}, seriously impacting device reliability [6].

Aim of this Section is to put in evidence the time-dependent V_{BR} in GaN-based HEMTs through pulsed I-V characterization, for which a custom measurement setup has been employed [7], allowing to properly investigate the pulse durations (T_{OFF}) effect on V_{BR}.

To pursue this study, we considered as test devices AlGaN/GaN single heterojunction HEMTs grown on SiC substrate whose nominal breakdown voltage (V_{BR}) was about 30 V. Devices presented a scaled gate length (L_G) of 0.1 µm while the gate width (W_G) was 0.6 mm. Iron (Fe) concentration in the GaN buffer presented a non-constant profile to allow the formation of the 2DEG at the AlGaN/GaN interface. The typical Fe-doping profile is reported in Fig. 5.1, along with a simplified cross section of the Device Under Test (DUT).

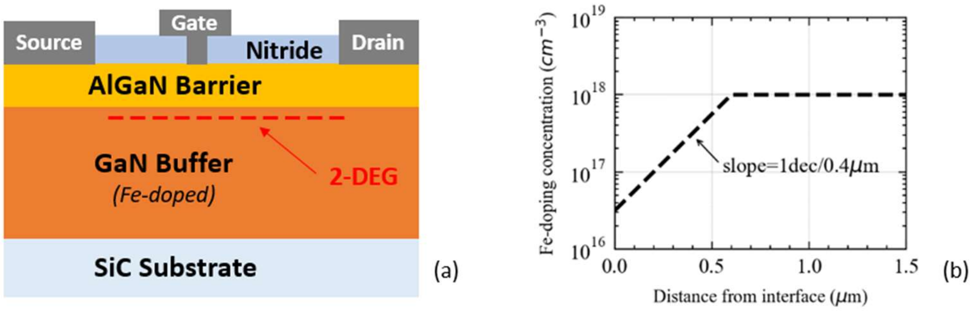

Figure 5.1: (a) Schematic cross-section of the Device Under Test (DUT). DUTs present a Fe-doped Buffer layer grown on top of a SiC substrate. (b) Fe-doping profile in the GaN buffer.

The schematic of the measurement setup employed for pulsed I-V characterization is reported in Fig. 5.2.

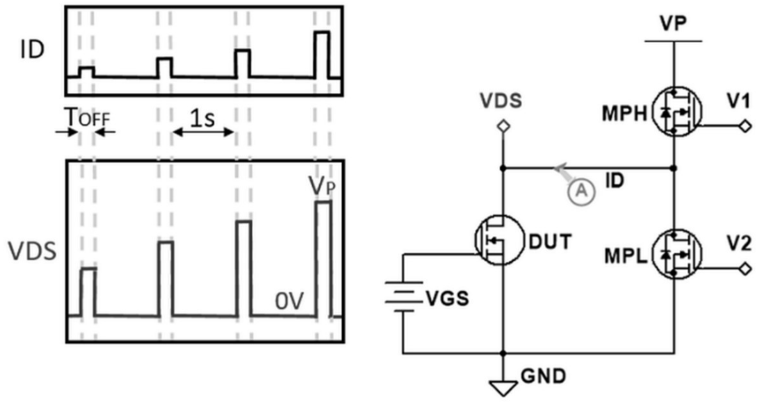

Figure 5.2: Simplified schematic of the measurement setup employed for the pulsed I-V breakdown measurement and typical measured V_{DS} and I_D signals.

During the measurement, the DUT is biased at $V_{GS} < V_{TH}$ to keep it in off-state condition while the drain voltage (V_{DS}) is pulsed between 0 V and V_P by means of two NMOS arranged in push-pull configuration. V_P pulses (each with T_{OFF} duration, T_{OFF} = 1 µs – 1 ms) are applied with 1-s delay time in order to eliminate possible memory effects during the characterization. After each pulse, V_P is increased linearly with a 0.5 V step to perform the sweep. Drain current (I_D) is measured by means of a current probe, by averaging several samples at the end of the pulse [3].

The typical breakdown I_D-V_{DS} curve acquired with the pulsed technique (T_{OFF} = 1 ms; V_{GS} = –4 V) is reported in Fig. 5.3.

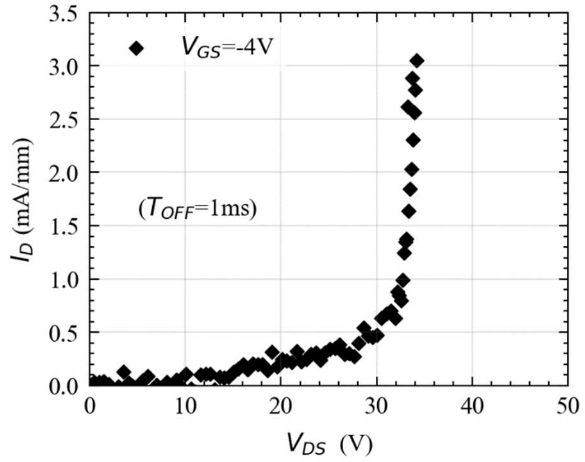

Figure 5.3: I_D-V_{DS} breakdown curve measured with T_{OFF}= 1 ms and V_{GS} = –4 V.

The breakdown voltage (V_{BR}) can be directly extracted from the I_D-V_{DS} curve in Fig. 5.3. In fact, V_{BR} can be defined as the V_{DS} for which the off-state leakage current starts to increase vertically. This is signature of avalanche generation and to trigger this condition a source of free carriers (leakage path) and a sufficiently high electric field are required simultaneously.

As we can see in Fig. 5.3, for V_{DS} above 30 V the drain current starts to increase vertically, meaning that the electric field experienced by the DUT is large enough to trigger the breakdown condition. Nevertheless, the breakdown current shown in Fig. 5.3 can be induced by several leakage paths [8]. Accordingly, to properly understand the mechanism triggering avalanche generation it is important to identify the leakage component which triggers the breakdown condition. To this end, in Fig. 5.4, we reported the leakage current components (I_D, $|I_G|$, I_S) measured at $V_{GS} = –4$ V.

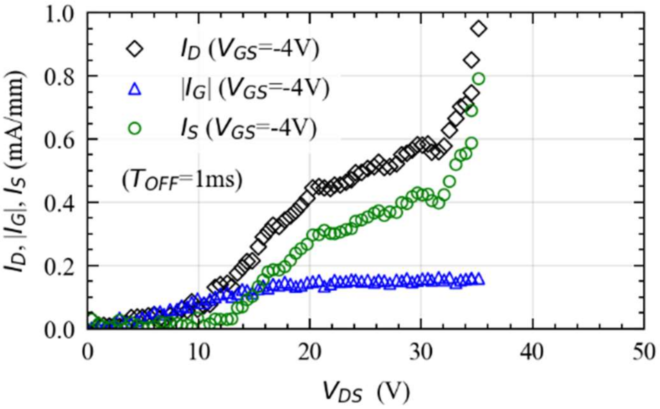

Figure 5.4: I_D, $|I_G|$ and I_S leakage currents measured with the pulsed system with $T_{OFF} = 1$ ms for $V_{GS} = –4$ V. For low V_{DS} values, the drain current is dominated by the gate leakage. At higher V_{DS}, the source current starts to increase rapidly, becoming the dominant component that triggers the breakdown condition.

From Fig. 5.4, it is clear that breakdown condition is triggered by source-injection [9]. In fact, at low V_{DS}, the drain current is dominated by the gate leakage, whereas at higher drain voltages I_S becomes the dominant component which brings the DUT in breakdown.

Since the buffer conductivity determines the breakdown condition, tested devices are good candidates for investigating the role of buffer traps on V_{BR}. In fact, these traps are expected to play a role on V_{BR}, as trapping of electrons into buffer traps is promoted by large V_{DS} applied in off-state [10], a condition typically encountered near breakdown. In addition, since charge trapping/de-trapping are time-dependent mechanisms, we expect to observe the dynamic effects of Fe-traps occupation on V_{BR} by varying T_{OFF} over several time decades. To this end, we measured several I_D-V_{DS} curves by varying T_{OFF} between 1 µs and 1 ms with logarithmically spaced time steps (see Fig. 5.5).

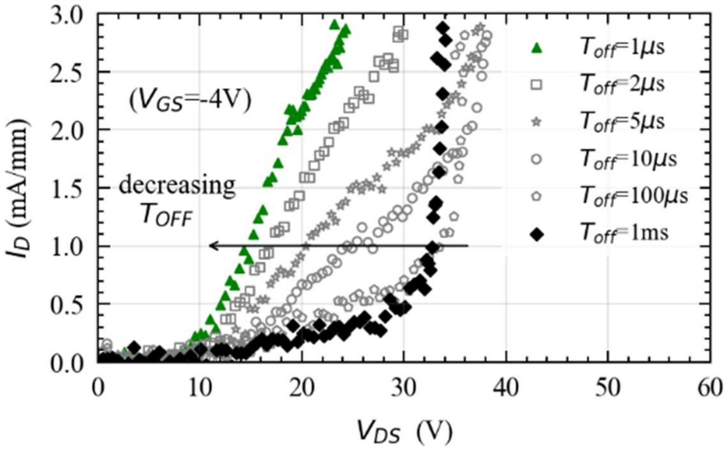

Figure 5.5: I_D-V_{DS} breakdown curves measured for different T_{OFF} in the 1 μs to 1 ms time range at V_{GS} = –4 V. The breakdown voltage reduces while decreasing T_{OFF}.

At V_{GS} = –4 V, the I-V curves move towards left while decreasing T_{OFF}, i.e., V_{BR} reduces. This effect could be ascribed to the time-dependent occupancy of Fe-traps, since a variation in the trapped carriers' concentration may change the availability of free carriers in the high field region that cause impact ionization. To validate this hypothesis, numerical device simulations have been performed as reported in the following subsection.

5.1.1 Numerical Device Simulations

Two-dimensional (2D) numerical device simulations were carried out with SDeviceTM simulator [11]. In order to obtain consistent information form simulations, I_D-V_{GS} and I_D-V_{DS} measurements on tested devices have been used to calibrate the simulation deck as shown in Fig. 5.6(a) and 5.6(b).

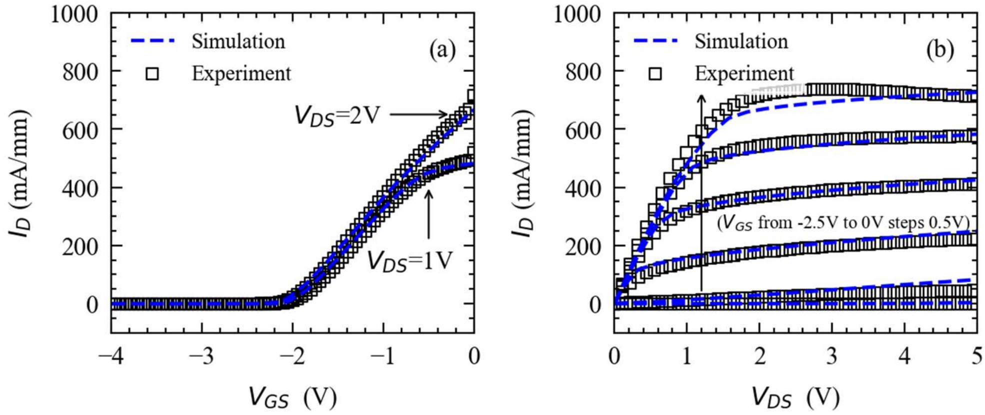

Figure 5.6: (a) I_D-V_{GS} characteristics measured at V_{DS}=1 V and V_{DS}=2 V. DUT's V_{TH} is about -2 V. (b) I_D-V_{DS} characteristics measured for V_{GS} ranging between -2.5 V and 0 V with 0.5 V step.

Fe doping in the GaN buffer was modelled by considering a deep acceptor trap at 0.52 eV below the GaN conduction band (E_C), according to the typical values reported in literature for this kind of defect [3-5, 12-17] and Fe-related traps occupation dynamics was modelled according to Shockley-Read-Hall (SRH) theory [11].

As reported in Fig. 5.7, numerical simulations indicate that the peak of ionized Fe-traps is located below the gate edge towards the drain terminal of the device [1].

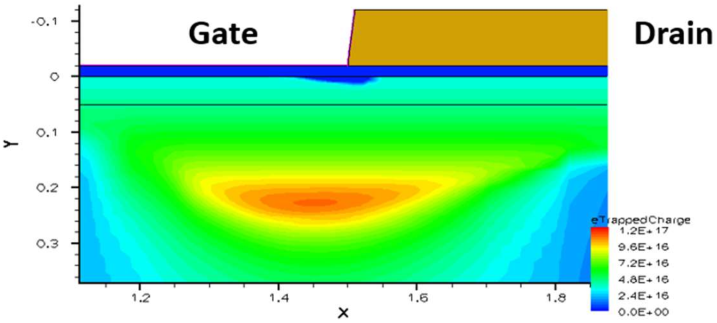

Figure 5.7: Concentration of ionized Fe-traps (V_{GS} = –4 V, V_{DS} = 10 V, T_{OFF} = 1 ms).

This information is extremely important, since this is also the region in which the electric field peaks [18]. Accordingly, the time dependent occupancy of Fe-traps modulates the free carriers' concentration in the high field region, potentially affecting V_{BR}. Particularly, for short pulses, the incomplete ionization of Fe-traps could yield a relatively high concentration of free electrons that reduces the electric field required to trigger avalanche. Conversely, at larger T_{OFF}, a higher concentration of trapped electrons in Fe-traps repulses free electrons from the high field region, yielding a reduced generation rate for a given V_{DS}. This interpretation finds good correspondence in the simulated I_D-V_{DS} curves (see Fig. 5.8).

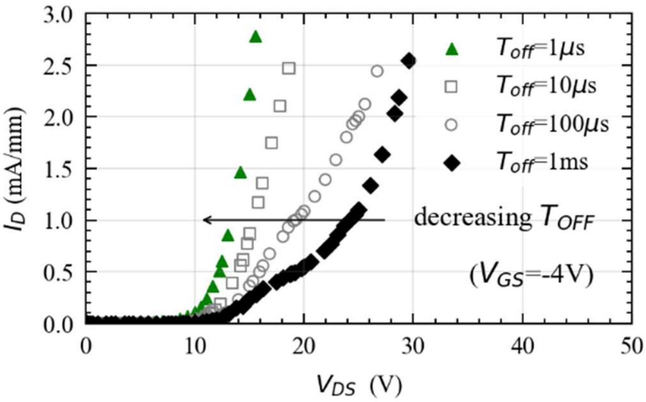

Figure 5.8: Simulated breakdown characteristics obtained for V_{GS} = –4 V and T_{OFF} in the range between 1 μs and 1 ms. The breakdown voltage reduces while decreasing T_{OFF}.

The behavior of the simulated I-V curves, showing a decrease in V_{BR} while decreasing T_{OFF}, is coherent with the one found experimentally. This can be better observed by looking at the V_{BR} vs T_{OFF} plot shown in Fig. 5.9, in which the V_{BR} values are extracted from the I_D-V_{DS} curves at the point in which I_D starts to vertically increase.

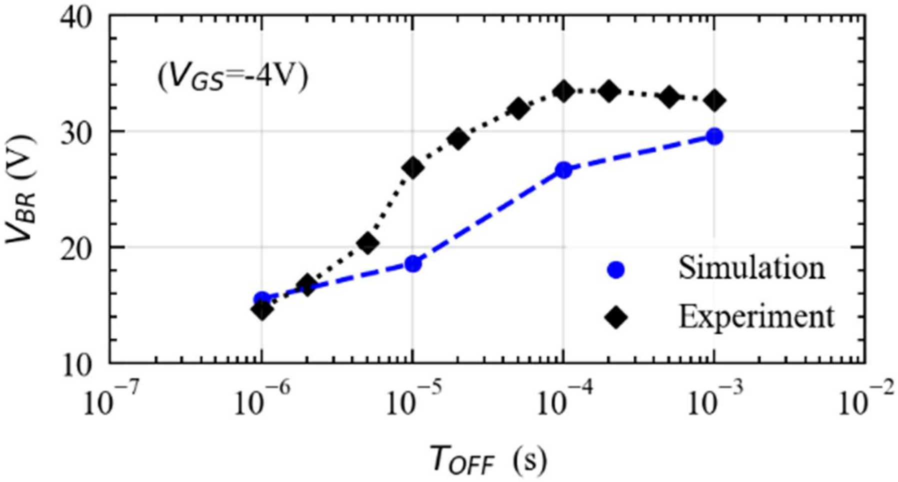

Figure 5.9: Comparison between the V_{BR} vs T_{OFF} curves obtained with measurement and simulations. V_{BR} is evaluated at the point in which the current I_D starts to increase vertically (signature of avalanche generation). V_{BR} decreases while decreasing from T_{OFF} = 1 ms to T_{OFF} = 1 μs.

Thus, the experimental trend of decreasing V_{BR} with decreasing T_{OFF}, is confirmed by numerical simulations, consistently with the dynamics expected from Fe-traps (see Fig. 5.10). In fact, at increasing T_{OFF}, the free carrier density in the high field region reduces due to an increased trapped electrons concentration. Accordingly, a larger drain voltage (i.e., larger electric field) is required to trigger the breakdown condition.

On the other hand, for short pulses (i.e., comparable with the trapping time constant of deep levels), the buffer allows for a larger source leakage current to flow, since the concentration of trapped electrons in Fe-related traps is lower (see Fig. 5.10). In this condition, the electric-field required for bringing the DUT in breakdown condition is lower. Accordingly, for the same V_{DS} value, the avalanche generation rate increases while reducing T_{OFF} (see Fig. 5.11), causing V_{BR} to decrease.

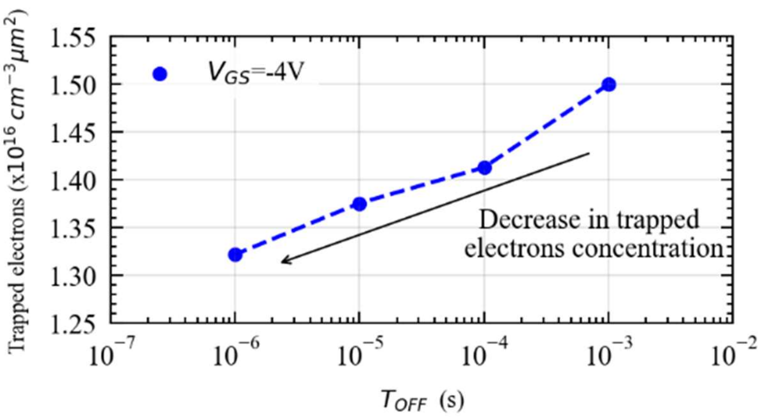

Figure 5.10: Integral of the trapped electrons concentration computed in the region under the gate edge towards the drain terminal for V_{DS} = 10 V, V_{GS} = –4 V and T_{OFF} from 1 µs to 1 ms. The trapped charge decreases at shorter T_{OFF}, thus yielding a less resistive buffer layer.

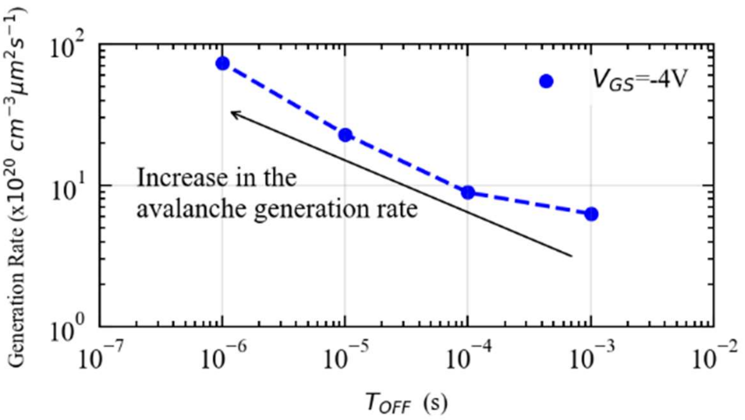

Figure 5.11: Integral of the avalanche generation rate computed under the gate edge towards the drain terminal for V_{DS} = 10 V, V_{GS} = –4 V and T_{OFF} from 1 µs to 1 ms. The avalanche generation rate increases at shorter T_{OFF} due to an increased free electrons density.

The high correlation between trapped electrons concentration and avalanche generation rate, observed at different T_{OFF}, suggests that the time-dependent V_{BR} behavior encountered in tested devices can be totally ascribed to Fe-traps occupation dynamics. This result is extremely important, since it shows that the time-dependent occupancy of Fe-traps can seriously affect the reliability of GaN HEMTs to be employed in RF communication systems, for which the switching period is comparable with the capture time constant of Fe-related buffer traps.

To gain more insights in the physics governing Fe-traps in GaN, the following Section studies the emission process from said deep levels, since it can provide much more information on the traps characteristics, that could be useful to understand the devices' behaviour.

5.2 Emission time form Fe-traps in GaN

A part from the time-dependent breakdown discussed in the previous section, the deep-acceptor related to Fe dopants at 0.5-0.6 eV from the conduction band minimum (E_C) [3-5, 12-17] represents a major cause for Current Collapse (CC) in GaN devices [19], leading to a decreased output power and consequent reduction of Power Added Efficiency (PAE) [20]. These detrimental effects have led many authors to study the nature of Fe-trap in GaN (see [21] and references therein), but a precise definition of the physics behind this deep level is still an open issue [17]. Further studies are thus required to accurately model the Fe-trap response and, consequently, the device behavior. To this end, the study of the charge emission dynamics from traps represents an effective mean to gain insights on their physics. More precisely, the emission time constants of deep levels are strongly affected by the operating conditions in terms of bias, temperature and electric field distribution and these dependences are indicative of the traps nature.

Aim of this Section is to further extend the knowledge on iron-related traps by investigating their emission rate dependence from bias conditions, temperature and electric field.

5.2.1 Device description and preliminary characterization

Devices tested in this study were single AlGaN/GaN heterojunction HEMTs grown on SiC substrate (see Fig. 5.12), presenting a 100 V breakdown voltage.

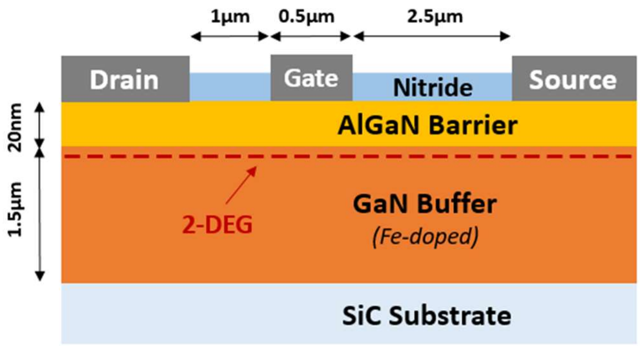

Figure 5.12: Schematic structure of tested AlGaN/GaN HEMTs.

AlGaN barrier layer was 20 nm thick with a 22% Aluminium concentration while the 2 µm thick GaN buffer was iron doped to obtain a semi-insulating layer [22]. Iron concentration in the GaN buffer starting from the SiC substrate interface is constant at 1 x 10^{18} cm^{-3} until a distance of 0.6 µm from the AlGaN/GaN interface where the iron concentration starts to decay with a slope of one decade every 0.4 µm. Device fabrication started with Ti/Al/Ni/Au Ohmic contact formation followed by device isolation by means of ion implantation. A Si_3N_4 passivation layer was then deposited followed by a CF_4-based dry etching for the opening of the device gate foot. Ni/Pt/Au gate metallization was then evaporated self-aligned, yielding an

I-shape gate contact without field-plates. Devices gate length was 0.5 µm while gate-source and gate-drain spacings were 1 µm and 2.5 µm, respectively. Three different gate peripheries were characterized, namely type A, B and C, presenting a total gate width of 10 x 100 µm, 8 x 75 µm and 4 x 75 µm respectively. Devices threshold voltage at 1 mA/mm drain current level at V_{DS}=7 V was approximately -2.8 V as shown in Fig. 5.13.

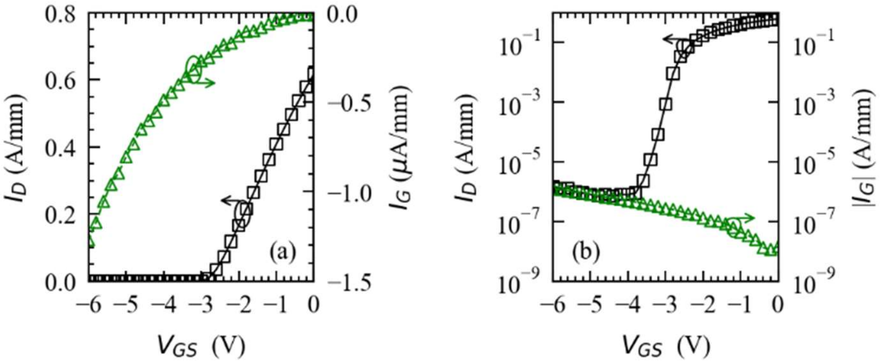

Figure 5.13: (a) I_D-V_{GS} (at V_{DS}=7 V) and I_G-V_{GS} characteristics for tested devices in linear scale. (b) I_D-V_{GS} (at V_{DS}=7 V) and |I_G|-V_{GS} characteristics for tested devices in semi-log scale.

The first characterization carried out focused on Pulsed IV measurement. Fig. 5.14 shows the typical 1µs/100µs pulsed IV characteristics obtained on a Type A device with two different quiescent baselines i.e., (V_{GSq}=0 V, V_{DSq}=0 V) and (V_{GSq}=-3.8 V, V_{DSq}=40 V). Saturated drain current (I_{DSS}) at V_{DS}=5 V is approximately 0.66 A/mm when evaluated from the (0 V, 0 V) baseline while it decreases to 0.43 A/mm when evaluated from the (-3.8 V, 40 V) bias, stemming from the presence of trapping phenomena.

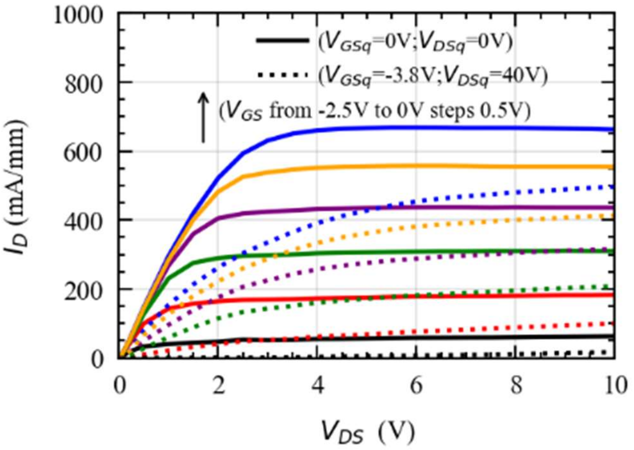

Figure 5.14: Pulsed output characteristics from two different baselines: V_{GSq}=0 V, V_{DSq}=0 V (solid) and V_{GSq}=-3.8 V, V_{DSq}=40 V (dotted). The current dispersion observed might be related to the response of iron-related trap located within the buffer.

The presence of Fe-doped buffer suggests that the observed current dispersion might be related to the response of iron-related traps located within the buffer. The kinetics of said traps was thus investigated by means of drain current transient (DCT) measurements.

5.2.2 Drain Current Transients (DCTs) measurement

DCTs induced by trapping phenomena have been measured with the double-pulse method sketched in Fig. 5.15, which allows to minimize the drain-source voltage (V_{DS}) variation during the transient [23].

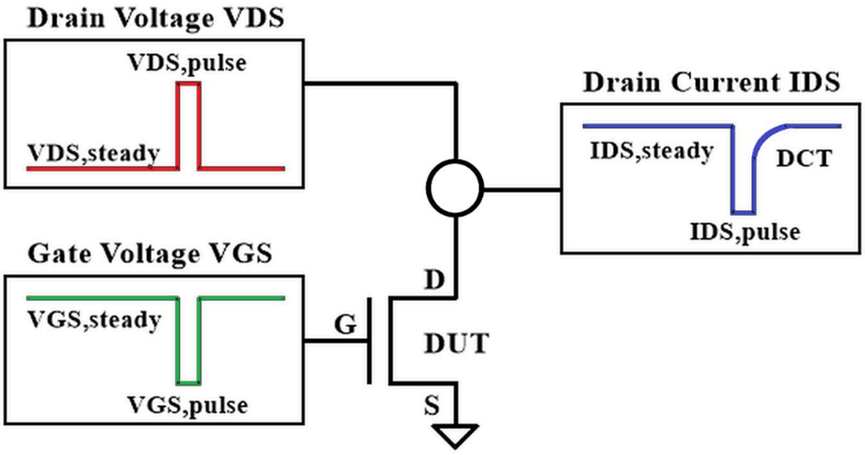

Figure 5.15: Simplified schematic of the double-pulse method used for the DCTs acquisition. A custom pulser circuit fixes the potential at the drain terminal (D), whereas a waveform generator is used for pulsing V_{GS}. V_{DS} and I_D are measured with a digital sampling oscilloscope and the recovering of the drain current (DCT) is monitored over several time decades after the application of 1µs trap-filling pulse.

The DUT is initially biased for few minutes in on-state conditions ($V_{DS,steady}$,$V_{GS,steady}$) allowing it to reach a stable $I_{D,steady}$ drain current level. A 1 µs trap-filling pulse is then applied with $V_{GS,pulse}$=-3.8 V and $V_{DS,pulse}$=40 V, ensuring the occupation of the traps [19]. Then, the device is set back to the initial ($V_{DS,steady}$, $V_{GS,steady}$) bias and the DCT is monitored over several time decades to allow for a full recovery of the initial $I_{D,steady}$ drain current value.

DCTs were thus measured at $V_{DS,steady}$=2 V while $V_{GS,steady}$ was settled in order to obtain a 50 mA/mm $I_{D,steady}$ current level. The apparently low values for both $V_{DS,steady}$ and $I_{D,steady}$ have been selected in order to reduce the influence of device self-heating which is known to affect the estimation of E_A [24]. Typical DCTs obtained on a type A device in the 30 °C to 70 °C temperature range are depicted in Fig. 5.16(a).

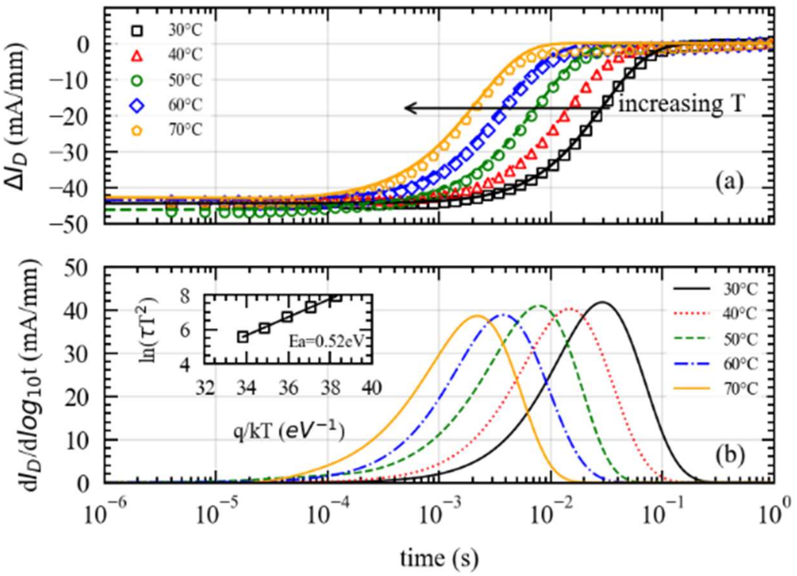

Figure 5.16: (a) DCTs measured at different ambient temperatures (from 30 °C to 70 °C) for device A. We represent the current variation (ΔI_D) with respect to the steady state current value at the end of the transient ($I_{D,steady}$). (b) $dI_D/dlog_{10}t$ used for drawing the Arrhenius plot (figure inset). The linear fit of the logarithmic form of the Arrhenius equation yields an activation energy E_A=0.52 eV.

In order to evaluate the charge emission dynamics, DCTs have been fitted by a stretched multiexponential function [25]. The corresponding $dI_D/dlog_{10}t$ signals are reported in Fig. 5.16(b) where a single and well-defined peak can be observed. The associated emission time constant (τ) has been then extracted in correspondence to the peak obtained in the $dI_D/dlog_{10}t$ signal, yielding the Arrhenius plot reported in the inset of Fig. 5.16(b). The linear fit of the points on the Arrhenius plot yielded a 0.52 eV activation energy, which is consistent with values reported in the literature for Fe-related buffer traps [3-5, 12-17].

This result proves the presence of Fe-related buffer traps in tested devices, suggesting that the DUTs can be used for investigating the impact of the bias conditions chosen on the characterization of said deep-levels.

5.2.3 Bias Conditions Effects

In this subsection, DCTs were then induced with different trap filling conditions ($V_{DS,pulse}$, $V_{GS,pulse}$) being able to highlight the effect of these parameters on the trap emission dynamics.

The first effect to be investigated is the one related to the parameter $V_{GS,pulse}$ (i.e., the gate voltage applied during the trap filling pulse). To this end, a 50 mA/mm steady state current and a $V_{DS,steady}$= 2 V were considered.

In order to assess the $V_{GS,pulse}$ effect, we fixed $V_{DS,pulse}$ at 30 V and we measured DCTs while varying $V_{GS,pulse}$ in the range between −3.5 V and −5.5 V. As we can see from Fig. 5.17(a), a variation in $V_{GS,pulse}$ does not affect significantly the DCTs shape, yielding nearly overlapping DCTs (i.e., with same amplitude) and aligned peaks in the $dI_D/dlog_{10}t$ plot, see Fig. 5.17(b).

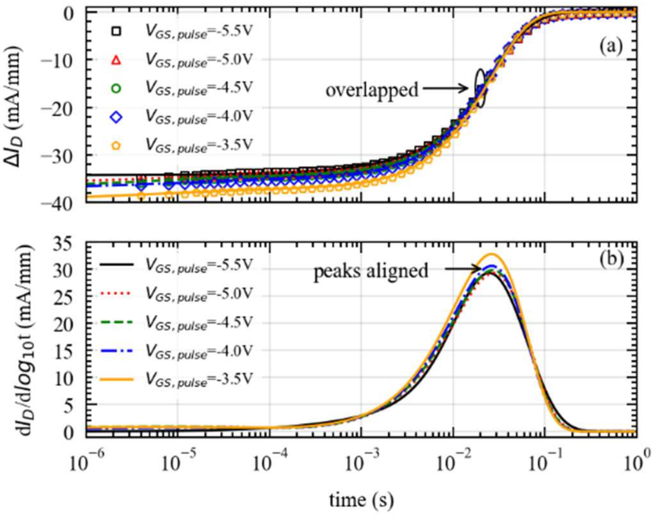

Figure 5.17: (a) DCTs measured at different $V_{GS,pulse}$ and $V_{DS,pulse}$ = 30 V. We represent the current variation (ΔI_D) with respect to the steady state current value at the end of the transient ($I_{D,steady}$=50 mA/mm). (b) $dI_D/dlog_{10}t$ used for extracting the emission time constant (τ).

This translates into approximately constant time constants (τ) as obtained from the measured DCTs, see Fig. 5.18, indicating that the extracted τ is weakly influenced by $V_{GS,pulse}$.

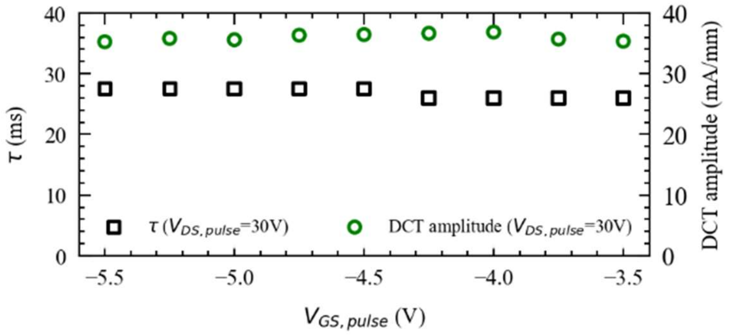

Figure 5.18: Emission time constants (τ) and corresponding DCTs amplitudes measured at several $V_{GS,pulse}$ levels and $V_{DS,pulse}$ = 50 V. Data points collected at different $V_{GS,pulse}$ are horizontally aligned in the whole range between −3.5 V and −5.5 V.

This observation is consistent with dynamics of buffer traps which is expected to be almost unaffected by the gate potential while being significantly influenced by the drain voltage [10]. According to this consideration, it is important to characterize the $V_{DS,pulse}$ effect on the traps dynamics.

To assess the effect of $V_{DS,pulse}$ on the DCTs, we kept $V_{GS,pulse}$ constant at −3.8 V (i.e., ~1 V below the device V_{TH}) while varying $V_{DS,pulse}$ in the range between 10 to 40 V. Results are shown in Fig. 5.19.

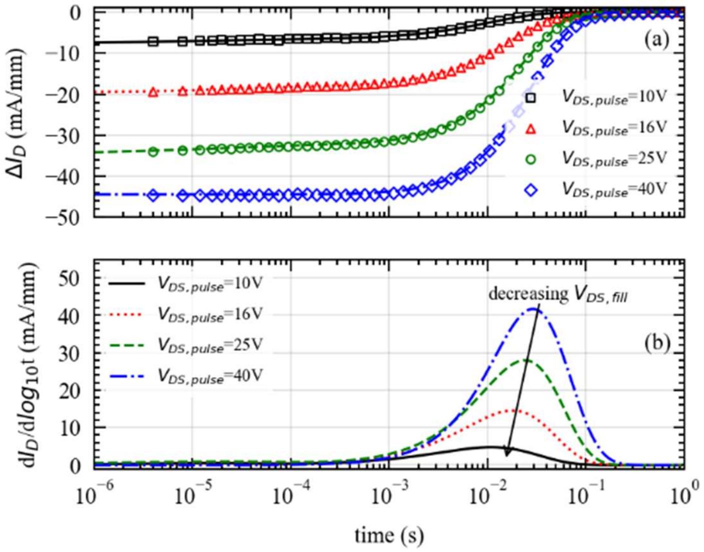

Figure 5.19: (a) DCTs measured at different $V_{DS,pulse}$ and $V_{GS,pulse} = -3.8$ V. We represent the current variation (ΔI_D) with respect to the steady state current value at the end of the transient ($I_{D,steady}$=50 mA/mm). (b) $dI_D/dlog_{10}t$ used for extracting the emission time constant (τ).

Interestingly, from Fig. 5.19(a) we observe that at lower $V_{DS,pulse}$ values, the DCT amplitude reduces with respect to the case for $V_{DS,pulse}$ = 40 V, indicating a reduced trapped charge variation as a consequence of the lower applied $V_{DS,pulse}$ [26].

At the same time, a reduction in $V_{DS,pulse}$ yields an apparent speed-up in the monitored DCTs, causing the peak in the $dI_D/dlog_{10}t$ signal to move towards shorter times, see Fig. 5.19(b).

To better understand this effect, we varied $V_{DS,pulse}$ between 8 V and 60 V, reporting in Fig. 5.20 the corresponding τ and DCTs amplitudes.

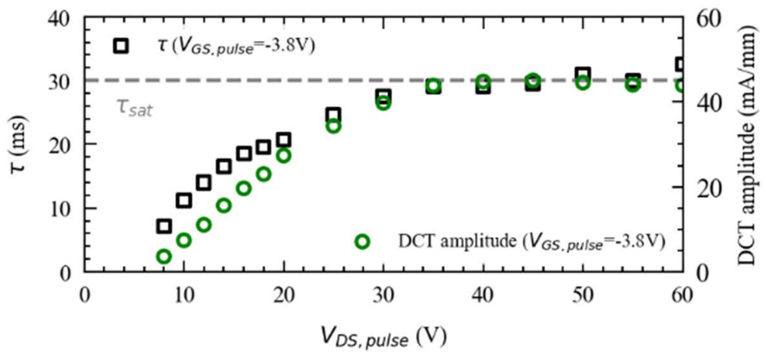

Figure 5.20: Emission time constants (τ) and corresponding DCTs amplitudes measured at several $V_{DS,pulse}$ levels and $V_{GS,pulse}$=−3.8 V. A variation on $V_{DS,pulse}$ produces a variation on both DCT amplitude and τ for $V_{DS,pulse}$ below 30 V, while data points collected at different $V_{DS,pulse}$ present weak variations in the range between 30 V and 60 V.

As shown in Fig. 5.20, a weak variation of τ and DCT amplitude is observed for $V_{DS,pulse}$ between 30 V and 60 V, suggesting that the mechanism involved vanishes at high $V_{DS,pulse}$, resulting in a "flat-τ region" (τ_{sat}). On the other hand, a variation of $V_{DS,pulse}$ from 30 V to 8 V yields a reduction in the extracted τ. This peculiar behavior apparently indicates that the emission rate could be dependent on the trap filling conditions, i.e., it increases with reducing $V_{DS,pulse}$. A similar trend was observed for the DCTs amplitude (see Fig. 5.20), suggesting a possible correlation between these two effects.

This effect can be explained by the concurrent trapping-emission processes during DCTs [5]. Accordingly, it is important to induce relatively large trapped charge variation (i.e., large DCTs amplitude) in order to monitor DCTs which are weakly affected by the capture process taking place under ($V_{GS,steady}$; $V_{DS,steady}$) bias at which the DCTs are monitored. If not, the extracted emission time constant could be underestimated, possibly yielding a wrong extraction of the traps parameter from the Arrhenius plot [5]. This point is clarified in the following subsection.

5.2.4 Impact on trap state identification

The fact that the extracted emission time constant form DCTs depends on the bias conditions and in particular on the DCT's amplitude, points out the need to investigate the impact of this dependence on the trap's parameters extraction and thus on the trap state identification.

In fact, the emission time constant extracted from DCTs acquired at different temperatures, are typically used to build the trap's Arrhenius plot and extract key parameters like activation energy and capture cross section. Particularly, the activation energy (E_A) is extracted from the slope of the linear fit of the logarithmic form of the Arrhenius equation, whereas the capture cross section is extracted from the intercept with the y-axis.

To investigate this effect, we reconstructed the Arrhenius plot corresponding to three different $V_{DS,pulse}$ values (i.e., 25 V, 16 V and 10 V) that correspond to three different DCTs amplitudes as observed in Fig. 5.20. The corresponding DCTs acquired for temperatures in the range between 30 °C and 70 °C are reported in Fig. 5.21.

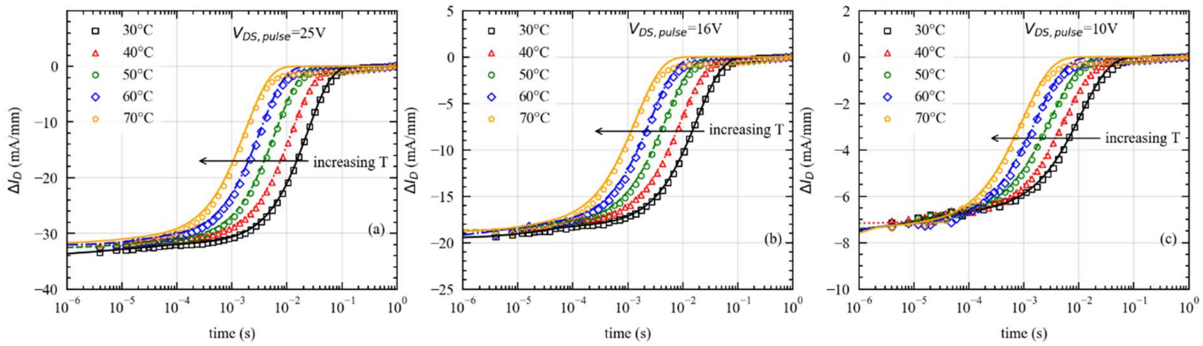

Figure 5.21: DCTs measured for temperatures between 30 °C to 70 °C with three different $V_{DS,pulse}$ values (i.e., (a) 25 V, (b) 16V and (c) 10V).

By extracting the emission time constants corresponding to the DCTs shown in Fig. 5.21, it has been possible to compare the relative Arrhenius plot to the one previously shown in Fig. 5.16 for $V_{DS,pulse}$= 40 V (see Fig. 5.22).

As we can see by looking at Fig. 5.22, different DCTs amplitude yields non-overlapping Arrhenius plots as a result of different emission time constant extracted from DCTs. Nevertheless, we can recognize parallel lines, indicating a similar activation energy extracted from the Arrhenius plots.

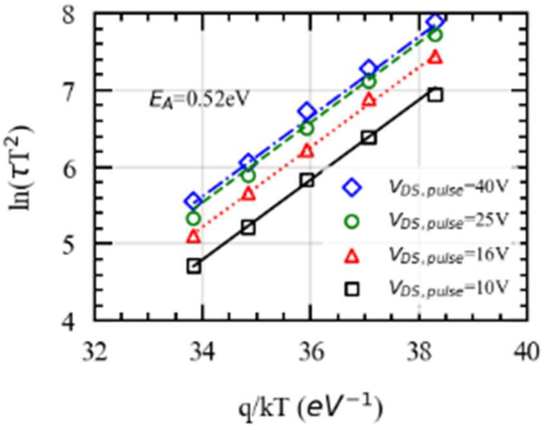

Figure 5.22: Arrhenius plots built from DCTs measurement performed at different $V_{DS,pulse}$ (i.e., 40 V, 25 V, 16 V and 10 V).

This observation is confirmed by the trap's parameter extracted and reported in Table 5.1, in which the same activation energy has been obtained while considering different trap filling bias, whereas a significant difference can be found on the estimated capture cross section.

Table 5.1: Trap's parameter extracted from the Arrhenius plots shown in Fig. 5.22.

$V_{DS,pulse}$	**40 V**	**25 V**	**16 V**	**10 V**
E_A	0.52 eV	0.52 eV	0.52 eV	0.52 eV
Cross-section	2.66×10^{-16} cm^2	2.87×10^{-16} cm^2	3.96×10^{-16} cm^2	6.05×10^{-16} cm^2

Accordingly, the choice of the bias conditions employed for the DCTs measurement could seriously impact the estimation of the trap's cross section from the Arrhenius plot. Nevertheless, the extraction of the trap's activation energy seems to be not affected by the transient amplitude, indicating that an increase in temperature equivalently affects the dynamics of the trap independently on the trapped charge variation induced by the bias conditions. Moreover, the fact that the same activation energy has been extracted suggests that the any physical mechanism that could impact this trap's parameter can be investigated by means of DCTs characterization, provided that transients featuring similar amplitudes are compared during the study.

To better clarify the nature of the trap states investigated in this study, we compared the Arrhenius plots obtained in this work for different $V_{DS,pulse}$ values, with those that have been associated to Fe-traps in previous reports [13, 16, 17, 27-29], see Fig. 5.23.

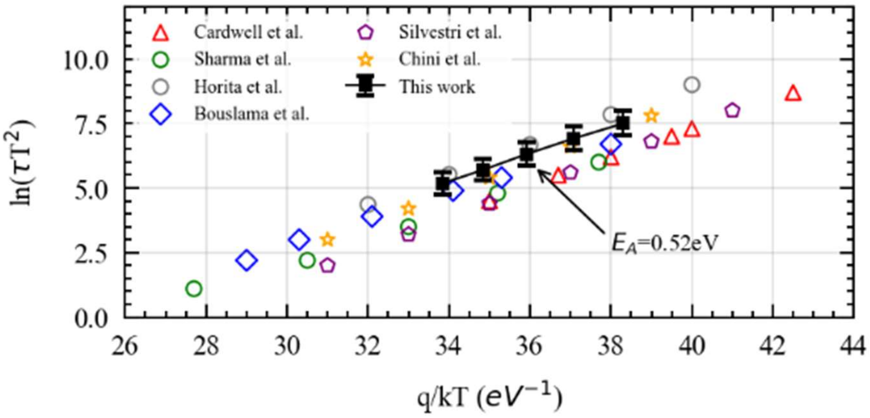

Figure 5.23: Comparison between the Arrhenius plot measured in this work and those associated to Fe-related traps by other authors. Points measured in this work well agree to those in the literature, confirming that the observed DCTs are due to electron emission from Fe-traps.

As we can see from Fig. 5.23, the activation energy, trap cross section and emission times are consistent with those largely reported for iron traps in GaN. According to this observation and to the presence of a highly Fe-doped buffer layer, we can further state that the monitored DCTs are due to the emission of electrons from traps related to iron dopants [13]. The devices tested can thus be used as test vehicles for the characterization of the iron trap under different measurements conditions, i.e., evaluate the effect device self-heating and electric field on the emission time constant of said trap.

5.2.5 Self-Heating and Electric Field Effects

Concerning thermal related effects, it is well known that the emission of an electron from an impurity level to the conduction band is a thermally activated process with emission time constant τ and activation energy $E_A=E_C-E_T$, mutually related by the Arrhenius equation [30]. Accordingly, the carrier emission rate from traps strongly depends on temperature (T) and this correlation is typically employed to extract E_A from measurements at different ambient temperatures. However, the estimation of E_A could be seriously affected by device self-heating (SHE) [24] which is known to increase the temperature in the device's active region thus accelerating the emission process [24].

Electric field plays a similar role in enhancing the emission rate yielding a potential reduction of the apparent activation energy [31]. Particularly, Poole-Frenkel Effect (PFE) is expected to dominate the field-enhanced emission for low-medium voltage levels (i.e., conventional RF operations), while secondary effects like Phonon Assisted Tunneling (PAT) and Direct Tunneling (DT) come into play only for high field values (i.e., high voltages) [32]. However, PFE affects only charged Coulombic traps [33-35], making it difficult to predict its contribution without an in-depth knowledge of the trap state involved in the emission process.

In order to investigate the dependence of the Fe-traps emission rate on SHE and electric field, Drain Current Transient (DCT) measurements [10, 36] are performed starting from properly chosen bias conditions to evaluate these two concurrent effects separately. DCTs are thus monitored for either: i) different dissipated power ($P_{D,steady}$) with constant drain-to-source bias ($V_{DS,steady}$), or ii) different $V_{DS,steady}$ with constant $P_{D,steady}$. The latter allows determining the role of PFE without increasing the device's SHE, while the former allows investigating SHE while keeping constant the electric field.

To a first approximation, the electric field intensity is directly linked to the applied $V_{DS,steady}$, whereas the $I_{D,steady}\times V_{DS,steady}$ product defines the power dissipation within the device. Steady state bias conditions were thus chosen with $V_{DS,steady}$ ranging from 15 V to 40 V with a 5 V step and dissipated power ($P_{D,steady}$) ranging from 0.4 W/mm to 2.0 W/mm with a 0.4 W/mm step for a total of 30 different steady-state bias conditions.

Prior to the actual DCT characterization, each steady-state condition was held for several minutes, i.e., a sufficiently long time to guarantee thermal equilibrium. Furthermore, the trap-filling pulse parameters were chosen to induce on purpose a relatively small current variation (~4 mA/mm) to avoid excessive perturbation of the steady-state operating point. This choice was mainly motivated by the fact that: i) a large current variation would change significantly the dissipated power during the monitored transient [24], whereas a small perturbation does not significantly alter the power set in steady-state condition, thus yielding negligible variations in the DUT's temperature; ii) a small current variation is representative of a low amount of trapped charge variation [29, 31, 37], whose dynamics is expected to not significantly alter the electric field profile during the DCT. During the 1 μs filling pulse, the devices are biased at $V_{GS,pulse}$=-3.8 V, i.e., 1 V below DUT's V_{TH}, so that the subthreshold current flowing through the channel/buffer provides the electrons to be trapped [29] and just the Fe-traps response is induced. The $V_{DS,pulse}$ level is instead adjusted for each DCT in order to induce a constant amplitude in the $dI_D/dlog_{10}t$ peak for all the acquired DCTs. This choice was adopted to guarantee the same variation of trapped charge into buffer states. In fact, maintaining a constant peak amplitude ensures a constant variation of trapped charge during the filling pulse, regardless of the steady state bias, since the amplitude of the peak is related to the amount of current dispersion caused by the trap with the considered time constant [29], i.e., to the amount of trapped electrons [26, 37].

In the experiments reported in Fig. 5.24, the self-heating effect is evaluated by fixing $V_{DS,steady}$ at 15 V while varying $P_{D,steady}$ between 0.4 W/mm and 2.0 W/mm by varying $I_{D,steady}$. In order to directly compare results obtained at different $I_{D,steady}$ values. measured DCTs are represented in terms of current variation (ΔI_D) with respect to the steady state current value at the end of the transient ($I_{D,steady}$)

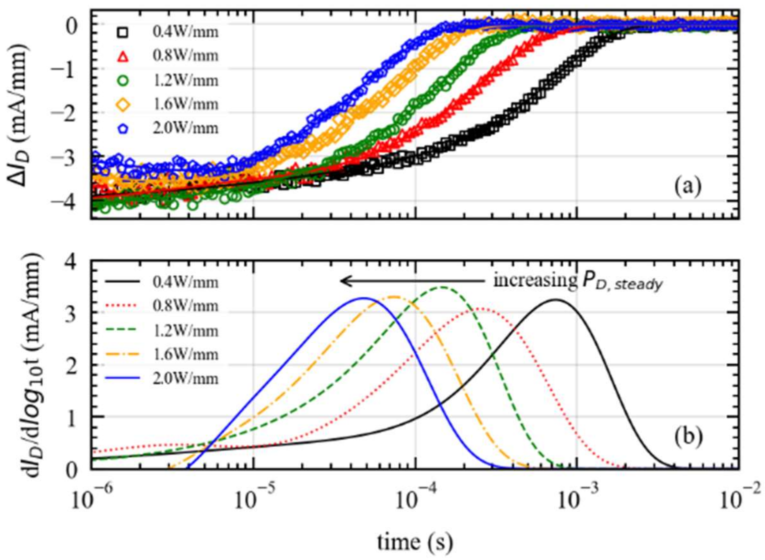

Figure 5.24: (a) DCTs measured at constant $V_{DS,steady}$=15 V (i.e., constant field) at different dissipated power ($P_{D,steady}$) for device A and (b) corresponding $dI_D/dlog_{10}t$. The charge emission process speeds-up at high $P_{D,steady}$ due to the temperature rise produced by device SHE.

As we can see in Fig. 5.24(b), the peak in the $dI_D/d\log_{10}t$ plot moves towards shorter times when increasing $P_{D,steady}$, according to the temperature rise in the device active region. The dependence of the emission rate on the SHE is consistent with expectations; in fact, the CC related to Fe-related Buffer traps is due to electron capture and the resulting DCT is due to the emission of trapped carriers to the conduction band. Since charge emission is a thermally activated process, the increase in the temperature caused by SHE is responsible for the speed-up observed while passing from 0.4 W/mm to 2.0 W/mm.

On the other hand, the electric field effect is shown in Fig. 5.25.

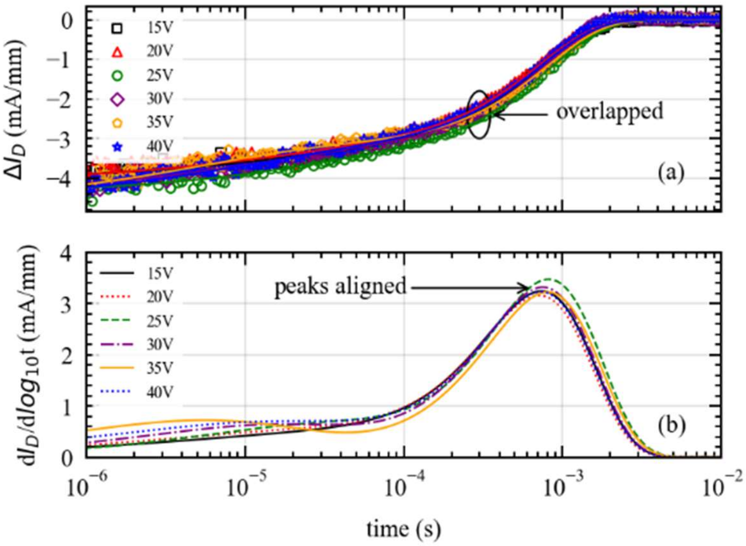

Figure 5.25: (a) DCTs measured at constant power ($P_{D,steady}$=0.4W/mm) and different $V_{DS,steady}$ for device A and (b) corresponding $dI_D/d\log_{10}t$. The field effect is negligible and the derivative peaks are perfectly aligned.

By varying $V_{DS,steady}$ in the device's saturation region between 15 V and 40 V while maintaining a constant power dissipation $P_{D,steady}$=0.4 W/mm we investigated operating points where the SHE is the same among all the DCTs considered. As a consequence, if the electric field plays any role in the emission time constant, we are expecting some variation at the increase of $V_{DS,steady}$. Fig. 5.25(a) shows that the measured DCTs at different $V_{DS,steady}$ are essentially overlapped and the corresponding peaks in the $dI_D/d\log_{10}t$ plot are perfectly aligned (see Fig. 5.25(b)). Accordingly, we conclude that the emission rate of the Fe-related acceptor is insensitive to the applied V_{DS} up to 40 V.

In order to highlight the generality of the previously discussed SHE and electric field dependencies, the characterization was performed on all the 30 steady-state bias points previously defined. Emission time constant from typical devices of type A, B and C geometries have been extracted, see Fig. 5.26(a), 5.26(b) and 5.26(c), respectively. The emission speed-up produced by SHE is always present, even if this effect is less pronounced for smaller devices, since a reduced periphery yields a lower temperature increase for the same power density. Nevertheless, for all tested devices we can see the same underlying trends. In the explored bias range, the field effect turned out to be negligible at all dissipated power values, while SHE produces a clear enhancement of the emission process, resulting in parallel lines moving toward shorter times at the increase of dissipated power.

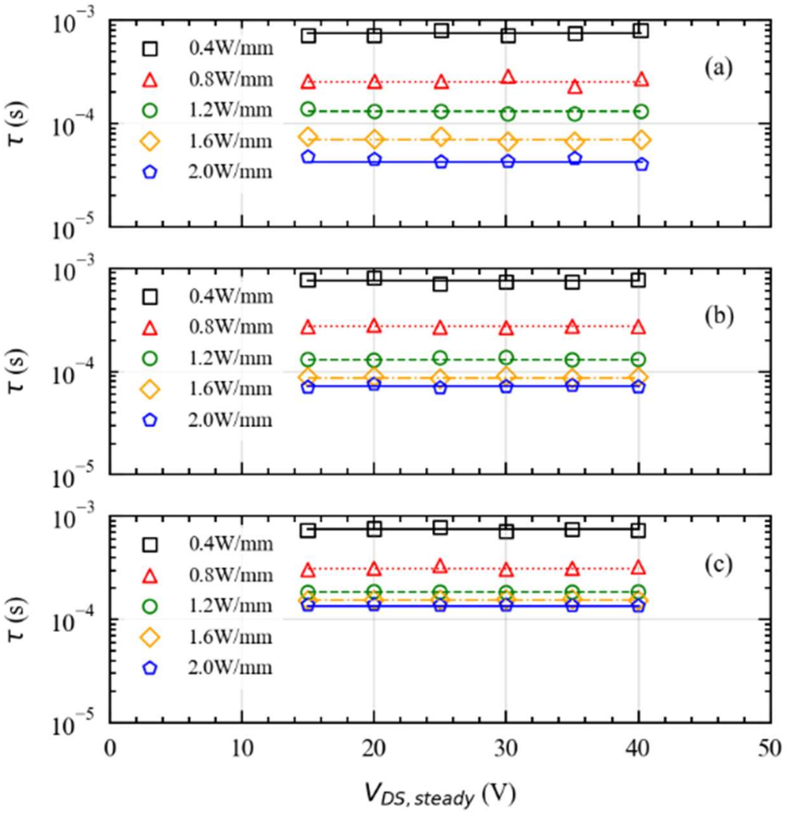

Figure 5.26: Emission time constants extracted at several $P_{D,steady}$ levels and different $V_{DS,steady}$ for (a) device A (10 x 100 µm), (b) device B (8 x 75 µm) and (c) device C (4 x 75 µm). A variation on $P_{D,steady}$ produces a readable variation on τ, while data points collected at different V_{DS} are horizontally aligned for the same $P_{D,steady}$.

Experimental data clearly shows that, in the investigate voltage range, the emission rate is not affected by electric field variations. This evidence suggests that electric field plays a minor role in enhancing charge emission from Fe-traps at medium-low V_{DS}. To better define the electric field experienced by Fe-traps in our measurements, we carried out 2-D numerical simulations using the commercial Sentaurus (Synopsis Inc.) simulator. Fe-related traps in the GaN buffer were modeled with deep acceptor-like traps at 0.52 eV below the conduction band edge, as experimentally observed by DCTs measurements.

The electric field in correspondence to the peak in the ionized trap concentration was considered as the one experienced by iron traps. Accordingly, the electric field (F) was extracted in the region of maximum trapping for $V_{DS,steady}$ between 15 V and 40 V and $P_{D,steady}$ from 0.4 W/mm to 2.0 W/mm, in order to span the whole bias range considered experimentally. The corresponding values of F are reported in Fig. 5.27, in which F ranges between 0.23 MV/cm and 0.41 MV/cm while passing from 15 V to 40 V. Particularly, the electric field experienced by Fe-traps increases almost linearly with the applied $V_{DS,steady}$, with a negligible dependence on $P_{D,steady}$.

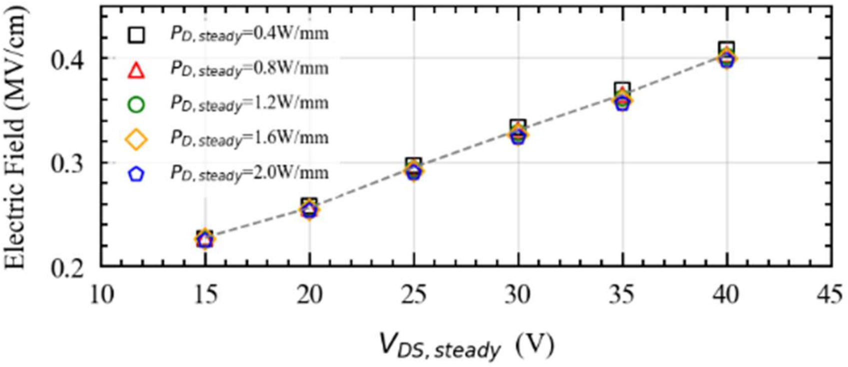

Figure 5.27: Electric field (F) values obtained with numerical device simulation for the explored bias conditions. While F increases approximately linearly with the applied voltage ($V_{DS,steady}$), it has negligible dependence on $P_{D,steady}$.

According to this observation, we can more thoroughly interpret the results obtained as follows. Even though the electric field (F) changes considerably while changing $V_{DS,steady}$ between 15 V and 40 V, this variation does not produce any appreciable effect on the emission time constant of Fe-traps in this range.

The electric field values obtained with numerical simulations can thus be used to better identify the field-related mechanisms that could affect the traps behavior in the explored bias range. Particularly, PFE is expected to affect emission rate for low-medium voltage levels [32]. The fact that we do not see any field dependence in our experimental data suggests that the traps involved, i.e., the iron related ones, are not experiencing PFE. In order to gain more insights in this behavior, we perform a simple first-order analysis to prove that if PFE would occur, completely different experimental trends would have been observed.

The PFE role in enhancing trap emission rate (e=1/τ) is given by [31]:

$$e = AT^2 \exp\left(-\frac{E_A - \Delta E_{PF}}{kT}\right) \tag{5.1}$$

where k is the Boltzmann's constant, E_A is the activation energy, T is the absolute temperature while A is a constant referring to the trap emission cross section. The ΔE_{PF} term in (5.1) refers to the Poole-Frenkel effect and is defined as [31]:

$$\Delta E_{PF} = \sqrt{\frac{q^3 F}{\pi \varepsilon_0 \varepsilon_r}} \tag{5.2}$$

where q is the elementary charge, ε_0 is the vacuum dielectric constant, ε_r is the GaN dielectric constant and F is the electric field [35].

Looking at equations (5.1) and (5.2) it is clear that an increase of F should increase the emission rate. The electric field in (5.2) can be defined according to the values reported in Fig. 5.27, since we are interested in the electric field experienced by Fe-traps in the explored bias conditions.

By taking the natural logarithm of the ratio between the emission rate (e) at a generic $V_{DS,steady}$ value (for which F is known, according to numerical simulations) and a reference e_{ref} at $V_{DS,ref}$=15 V (i.e., F_{ref} ~0.23 MV/cm), it is now possible to predict the relative e enhancement due to PFE. Furthermore, if we compare data obtained at the same $P_{D,steady}$, as it has been done experimentally, temperature variations con be assumed to be negligible thus allowing to simplifying the $AT^2exp(-E_A/kT)$ term in (5.1) highlighting in (5.3) the square root dependence on F:

$$\ln\left(\frac{e}{e_{ref}}\right) = \frac{\sqrt{\frac{q^3}{\pi \varepsilon_0 \varepsilon_r}}}{kT}\left[\sqrt{F} - \sqrt{F_{ref}}\right] \tag{5.3}$$

Despite this simplification, a realistic value for T (i.e., temperature in the device active region) should be extracted to compute (5.3). To this end, T was evaluated for device A at several dissipation levels with the McAlister's method [38], yielding a thermal resistance (R_{TH}) of 22 K/W. The extracted R_{TH} was then used to infer T for the considered bias range (i.e., $P_{D,steady}$ between 0.4 W/mm and 2.0 W/mm), according to (5.4):

$$T = 303K + R_{TH} \times P_{D,steady} \tag{5.4}$$

Since device A presented a total gate width of 10 x 100 µm, we obtained two limit cases for T: T=311.8 K for $P_{D,steady}$=0.4 W/mm and T=347 K for $P_{D,steady}$=2.0 W/mm. In order to cover the whole temperature range explored in this study, we considered both values of T in our analysis.

A comparison between the emission rate obtained from experimental data in Fig. 5.26(a) and analytical values computed with (5.3) is shown in Fig. 5.28.

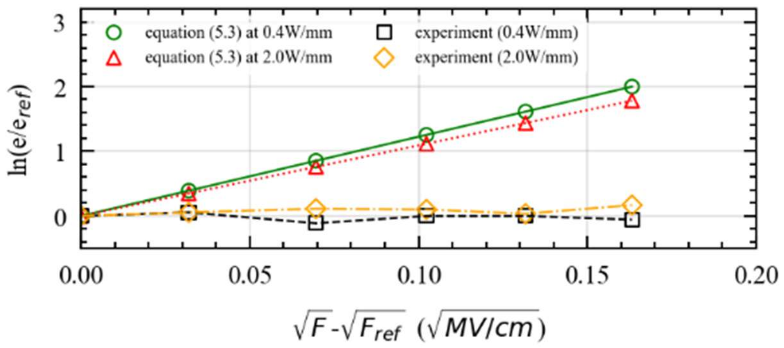

Figure 5.28: Relative variation in the emission rate produced by F on device A w.r.t. the field enhancement expected for PFE. The PFE enhancement has been estimated with (5.4) for $P_{D,steady}$=0.4 W/mm and $P_{D,steady}$=2.0 W/mm.

Interestingly, the comparison shows that the predicted behavior with (5.3) is completely different from actual data, indicating that PFE is not taking place. Rather than a rigorous comparison, Fig. 5.28 should be intended as an integrity check for the validity of the speculation that PFE does not take place for iron traps in these devices. In fact, if PFE was actually affecting emission rate, experimental data points would not lie on a horizontal line, but would rather be placed nearby the curves calculated with (5.3). For this reason, we can conclude that the PFE can be ruled out as mechanism inducing emission acceleration for Fe-traps, since in the explored voltage range it would have produced a significant V_{DS} (i.e., field) dependence, which is on the contrary absent. This evidence highlights the nature of iron traps. In fact, for a trap state to experience PFE, it must be charged when empty and neutral when it captures a carrier (i.e., donor-like) [33-35]. Conversely, iron dopants introduce a deep acceptor-like trap which is normally neutral and becomes negatively charged by capturing an electron from the conduction band [39]. The trap potential can be approximated at first-order by a Dirac well [34], for which the barrier lowering responsible for PFE would be negligible in agreement with the presented experimental results.

5.3 Conclusions

In this Chapter, we reported a study on Fe-related buffer traps in GaN. Particularly, we highlighted the correlation between the time dependent breakdown voltage experienced by Fe-doped GaN HEMTs and the occupation dynamics of iron traps. Moreover, we investigated the effect of the bias conditions on the characterization of Fe-traps by means of Drain Current transient measurements. The emission time constant extracted from DCTs was found to be dependent on the DCT amplitude, yielding possible difference in the cross section estimation from the Arrhenius plot. Conversely, this dependence was found to do not affect the estimation of the traps activation energy. To pursue a deeper investigation, we studied the role of self-heating and electric field on the emission process from iron-related traps in AlGaN/GaN HEMTs for RF applications. The adopted experimental approach, based on the monitoring of drain current transients with either constant dissipated power or constant drain-to-source bias allowed to effectively evaluate separately self-heating and electric field roles. We found that, a result of the temperature raise in the device active region, self-heating produces a significant acceleration in the thermally activated emission process. On the other hand, the experimental results revealed no evidence of the Poole-Frenkel effect (PFE), consistently with the non-Coulombic nature of Fe-related buffer traps. This yields to the conclusion that Poole-Frenkel effect can be excluded for Fe-traps in GaN, whereas thermal effects dominate the emission dynamics from these traps under conventional operative conditions. This result clarifies the behavior of iron traps in GaN HEMTs for which the absence of PFE can reduce the complexity of the simulation models used to interpret the experiments without loss of accuracy.

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6 Novel Temperature Estimation Technique

In this Chapter we present a novel technique for estimating the channel temperature in semiconductor devices. This technique exploits the thermally activated emission process from traps as physical mechanism for detecting the device temperature. Particularly, based on the considerations made in Chapter 5 on the role of device self-heating on iron traps in GaN, these defects are good candidates for the implementation of this novel technique and are thus considered as leading example to present the method.

6.1 Temperature Estimation

Thermal effects are known to seriously affect the performances of electronics devices [1, 2]. As a relevant example, an in increase in the device temperature could yield an increase in the on-state resistance in semiconductor devices that could impact the efficiency of electronic equipments. Moreover, an increase in the device temperature could seriously affect other key parameters like device's threshold voltage and breakdown, yielding both stability and reliability issues. These problem could be more evident in devices operating at high power densities (i.e., GaN-based power devices), in which the Self-Heating Effects may exacerbate the thermal-related issues [3]. Accordingly, an accurate temperature estimation is of primary importance to correctly characterize the device behaviour and define its safe operating area (SOA). Several techniques (electrical and optical) for estimating device temperature have been proposed so far [4], each of them presenting both advantages and limitations.

Concerning electrical techniques, DC characterization methods [5, 6] represent a fast and easy solution, but they are extremely dependent on the device geometry, since they are only able to determine average temperature, giving a significant underestimation of the peak temperature (T_{peak}) inside the device [7]. Moreover, DC measurements are conventionally based on I-V output characteristics obtained by sweeping the drain voltage, whose sweep-time may affect the temperature estimation due to time-dependent occupancy of traps and transient thermal response of the device [8]. To solve this issue, techniques based on pulsed I-V measurements [9] have been proposed, but these are still unable to provide a significant improvement in the accuracy of actual T_{peak} estimate over DC techniques [10]. A very promising electrical method is based on the low-radio frequency (RF) output conductance technique [11, 12], which significantly reduces the T_{peak} underestimation problem while maintaining a reasonably low complexity, also characterizing the previous methods. However, similarly to DC characterization, low-RF output conductance technique is affected by trap-induced dispersion phenomena that affect temperature estimation [13]. The best results with state-of-the-art electrical methods have been obtained with Gate RTD technique [14], but this solution is unfeasible for conventional in-package devices since it requires additional terminals for performing the measurement.

Concerning optical methods, infrared (IR) thermography and μ-Raman spectroscopy are the conventional approaches [15]. Despite its simplicity and short characterization time [16], the former technique suffers from low T_{peak} resolution [10]. On the other hand, the latter shows high spatial resolution (~1 μm) and good accuracy [17], however it requires specific sample preparation for ensuring optical access to the device's active region [16]. Moreover, μ-Raman spectroscopy cannot normally sense underneath overhangs or field plates [16], providing an underestimation of the actual T_{peak}. In fact, power dissipation under the gate edge towards the drain contact of the transistor (and also possibly under peaks in correspondence of field-plates [12]) is known to contribute to a significant degree to the total power [18, 19]. These regions cannot be easily sensed by optical methods, since metal field-plates, commonly employed for improving dynamic performance and reliability of power devices [20], impede the optical access to the hot-spots. These limitations call for different approaches to estimate the device channel temperature. To this end, we propose a novel electrical technique based on the indirect temperature estimation through the characterization of charge emission from traps.

In this study, we focus our analysis on Fe-doped AlGaN/GaN high-electron mobility transistors (HEMTs). Traps in these devices are associated to Fe-dopants intentionally introduced in the GaN buffer during the fabrication process for rendering the buffer semi-insulating and increase the blocking voltage. These traps represent a very promising option for the application of this technique. In fact, these traps are located near the gate edge towards the drain terminal of the device [21], which is the region where temperature peaks [18]. Accordingly, the temperature (T_{Fe}) activating charge emission from Fe-traps is fairly close to the hotspot, suggesting that the thermally activated emission can be used as an indirect measurement of T_{peak} in the device.

6.2 Proposed Method

As already mentioned, the proposed method exploits the thermally activated emission process from Fe-traps. It is important to notice that the emission from iron traps can be easily evaluated through DCTs measurement, thus providing an easy implementation like conventional electrical methods. This makes it relatively simple from a measurement point of view. Nevertheless, an accurate model that put in evidence the correlation between the emission time and temperature must be defined for the application of the technique. In the following, the physical-based model used for this scope is derived and the procedure to be followed for the implementation of the method is described in detail.

6.2.1 Model definition

Fe-related Buffer traps behave as deep acceptor states located 0.5-0.6 eV below the GaN conduction band edge (E_C) [22-28] and capture electrons when the DUT is biased at relatively large drain voltage (V_{DS}) [25]. When this large drain bias is removed, captured electrons are slowly emitted to E_C through a thermally activated emission process characterized by an emission time constant (τ). This parameter can be directly extracted by means of DCTs measurement and strongly depends on T. As such, the τ-T relationship can be used to indirectly extract temperature from DCTs. Assuming Shockley-Read-Hall (SRH) theory [29] applies, the mutual correlation between τ and temperature (T) is described by the Arrhenius equation [30]:

$$\tau = \frac{1}{T^2} \times \exp\left(\frac{qE_A}{kT} + C\right) \tag{6.1}$$

where k is Boltzmann's constant, q is the elementary electron charge, E_A is the trap activation energy, C is a parameter proportional to the trap cross section (σ), and T (expressed in Kelvin) is the temperature experienced by deep levels. To a first approximation, temperature in the device can be expressed as:

$$T = T_{BP} + R_{TH} \times P_D \tag{6.2}$$

where T_{BP} is the base-plate temperature, R_{TH} is the thermal resistance and P_D is the dissipated power. R_{TH} is a temperature-dependent parameter, due to the thermal conductivity dependence on temperature [31]:

$$R_{TH}(TBP) = R_{TH\_300K} \times \left(\frac{T_{BP}}{300K}\right)^{\alpha} \tag{6.3}$$

Thus, by substituting (6.2), (6.3) in (6.1) we obtain a non-linear model for τ with four unknowns (E_A, C, R_{TH_300K}, α). In order to estimate T, these unknowns must be extracted.

6.2.2 Procedure description

The procedure to be followed for the application of the proposed method is schematically depicted in Fig. 6.1 and described in detail as follows.

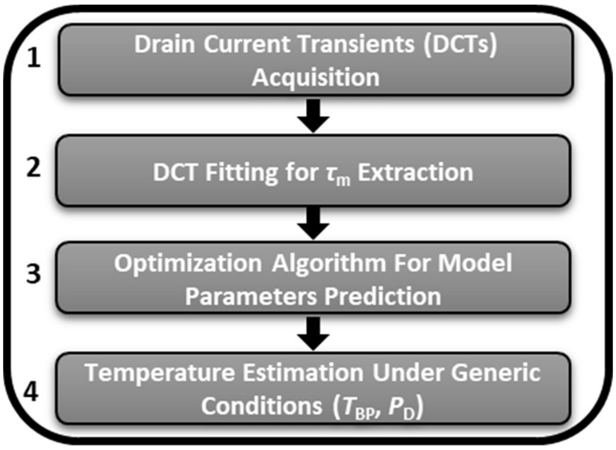

Figure 6.1: Schematic representation of the proposed technique for temperature estimation.

1) The first step consists in the acquisition of a dataset of emission time constants representing the Fe-traps behavior under different thermal conditions. This set of data is built by acquiring DCTs at several base plate temperatures (T_{BP}) and quiescent bias conditions ($V_{DS,q}$, $I_{D,Q}$) or, equivalently, P_D (since $P_D = V_{DS,q} \times I_{D,Q}$). Moreover, it is important to set the trap filling bias in order to induce DCTs presenting comparable amplitudes. This is important in order to consider DCTs featuring similar trapped charge variation (ΔQ) [25].
2) Once acquired, DCTs are fitted to extract the emission time constant (τ_m) in correspondence of the peak in the $dI_D/d\log_{10}t$ signal. Thus, for each DCT, we have two thermally related features (T_{BP} and P_D) and one 'observable' (τ_m).
3) Then, an optimization algorithm (e.g., Trust Region Reflective (TRR) [32, 33]) is applied for non-linear least squares minimization (NLLSQ) of the residuals between τ_m and the τ determined from eqs. (6.1)-(6.3) (i.e., τ_p). The least squares problem defines the cost function (CF) which has to be minimized and the optimal parameters are those minimizing this function. Actually, in CF, we consider the logarithm of τ_m and τ_p in order to uniformly weighting both short and long emission times. Thus, CF is defined as:

$$CF = \frac{1}{2}\sum_{i=0}^{n}\left[\log_{10}\left(\frac{\tau_{p,i}}{\tau_{m,i}}\right)\right]^2 \tag{6.4}$$

where, $\tau_{p,i}$ is the i-th emission time constant predicted by the model for $T_{BP,i}$ and $P_{D,i}$; $\tau_{m,i}$ is the i-th emission time constant extracted from DCT for the same $T_{BP,i}$ and $P_{D,i}$.

4) After optimization, the extracted parameters can be used in equations (6.1)-(6.3) to infer the device temperature for an arbitrary (T_{BP}, P_D) condition.

Now that the method is defined, it is important to validate it. To this end, we performed two-dimensional electro-thermal device simulations, since the simulator provides the actual peak temperature in the device's active region that can be than compared with the one estimated by the proposed method.

Simulated devices were single heterojunction AlGaN/GaN HEMTs featuring a SiN passivation and a Silicon Carbide (SiC) substrate. A schematic cross section of the simulated structure is reported in Fig. 6.2.

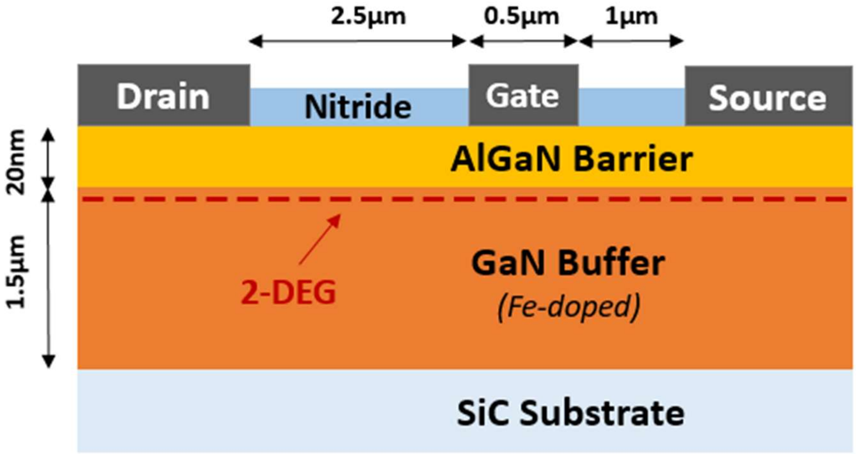

Figure 6.2: Schematic cross-section of the simulated devices. 2-DEG stands for two-dimensional electron gas.

GaN Buffer was iron (Fe) doped to obtain a semi-insulating layer. The Fe doping profile considered in this study is the one typically encountered in which the iron concentration is constant (10^{18} cm^{-3}) up to 0.6 μm from AlGaN/GaN interface, above which concentration exponentially decays with slope of 1 dec/0.4 μm. The presence of Fe-traps in the buffer layer, introduced by Fe dopants, was simulated by considering a deep-acceptor trap located 0.56 eV below the conduction band edge, consistent with the energy level reported for Fe-traps in GaN [22-28].

To apply the method, Drain Current Transients (DCTs) measurements [34, 35] are acquired at different (i) base-plate temperatures (T_{BP}) and (ii) bias conditions. The data is then used to extract the trap emission time constant (τ) allowing to estimate device temperature from the τ-T relationship described by the model just derived.

6.3 Simulation Results

In this section we present the simulation results obtained for both the McAlister method and the proposed technique.

6.3.1 McAlister Method

First of all, we applied the McAlister method on the simulated structure in order to have a mean of comparison for benchmarking the proposed technique. The method is extremely simple: (i) the saturation current is acquired at different ambient temperatures in order to build the calibration curve shown in Fig. 6.3.

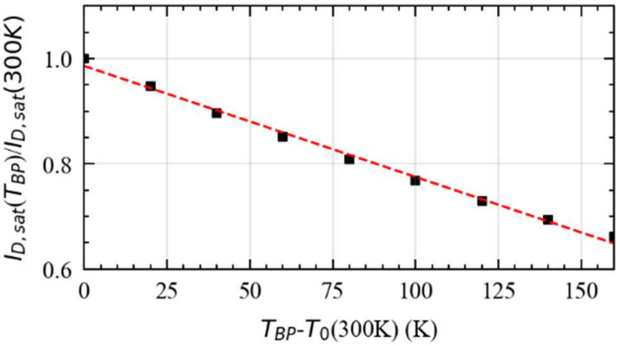

Figure 6.3: Calibration curve used for the McAlister Method.

Then, the output characteristics of the device is represented as a function of the dissipated power instead of the applied the drain voltage [5]. The comparison between the output characteristics represented in this way and the calibration curve allows to extract the thermal resistance to be used for temperature estimation under different dissipation levels. This is shown in Fig. 6.4 in which a R_{TH} (300 K) = 5.71 K/W was extracted.

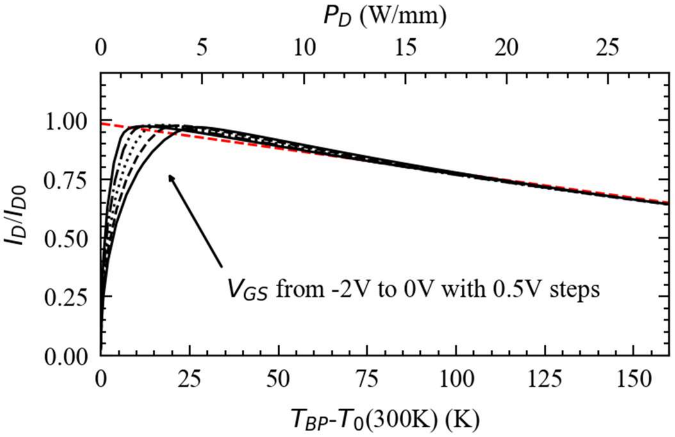

Figure 6.4: Comparison between Output Characteristics represented as a function of the dissipated power (P_D) and calibration curve.

6.3.2 Proposed Method

At this point, the proposed method was applied. In order to characterize the emission process from Fe-traps, DCTs have been adopted [34, 35]. Typical waveforms employed for this kind of characterization are sketched in Fig. 6.5.

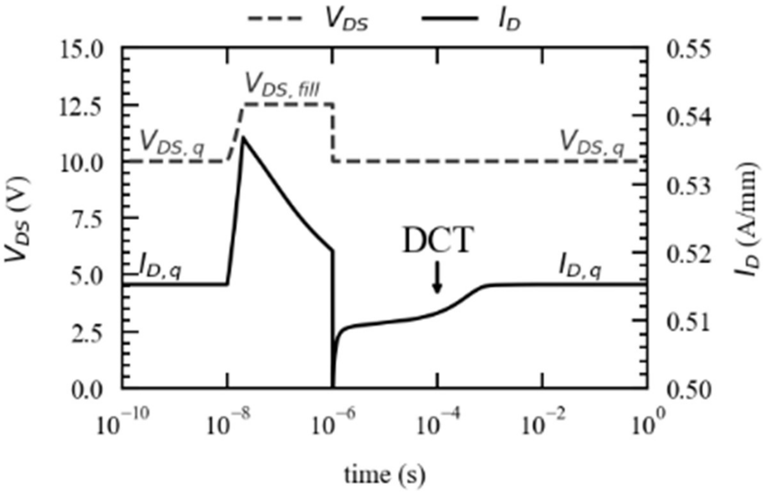

Figure 6.5: Typical V_{DS} and I_D during simulation of DCTs characterization in drain lag configuration.

The DUT is biased for few minutes in on-state at a certain (V_{GS}; $V_{DS,q}$; $I_{D,q}$) quiescent point (i.e., P_D level) to guarantee thermal equilibrium. A short (t_{fill}=1 μs) Drain-Lag trap filling pulse (V_{GS}; $V_{DS,fill}$) is then applied in order to trigger capture of electrons into Fe-related buffer traps. After t_{fill}, the V_{DS} is set back to its quiescent value and the drain current recovery transient is monitored in the 1 μs – 1 s time range to extract the emission time.

The choice of the filling pulse parameters is mainly related to the following considerations: (i) Fe-related buffer traps are filled by electrons when large V_{DS} voltages are applied to the device; (ii) the current flowing through the 2-DEG in trap-filling condition provide the electrons to be trapped; (iii) the tfill duration of 1 μs is sufficiently long to ensure trap occupation and short enough not to significantly affect the device temperature prior to the subsequent DCT acquisition.

An example of acquired DCT is reported in Fig. 6.6(a) from which we immediately observe a single and well defined transient, yielding a single peak in the corresponding $dI_D/d\log_{10}t$ signal (see Fig. 6.6(b)). The rising drain current transient is due to the emission of electrons to the 2-DEG, restoring the channel conductivity after the removal of the trap filling bias. Particularly, the steady state current reached at the end of the transient is equal to the quiescent value ($I_{D,q}$) (see Fig. 6.5), meaning that the electrons trapped into Fe-traps are completely emitted after 1 s from the removal of the trap filling pulse.

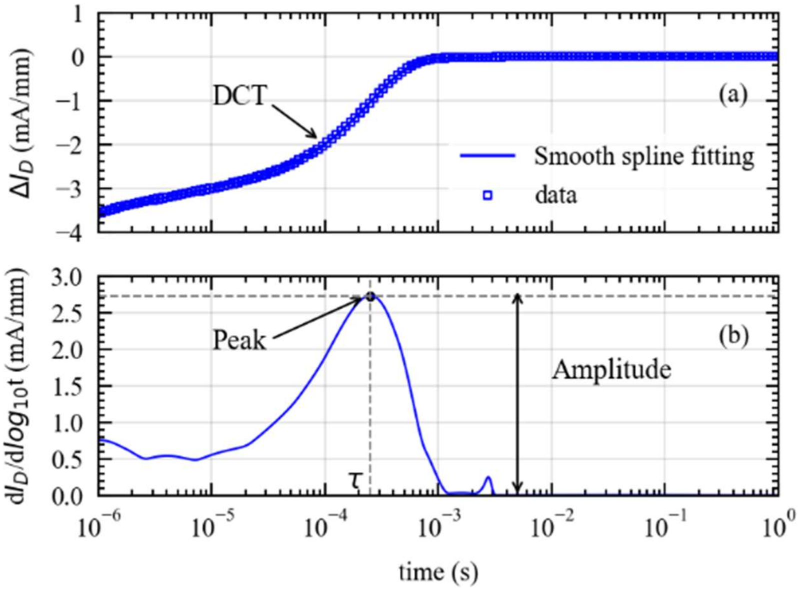

Figure 6.6: (a) DCTs measured at $V_{DS,q}$ = 10 V (T_{BP} = 300 K) $I_{D,q}$ = 0.5 A/mm. We represent the current variation (ΔI_D) with respect to the steady state current value at the end of the transient ($I_{D,q}$). (b) $dI_D/dlog_{10}t$ used for extracting the emission time constant (τ). τ and amplitude are extracted in correspondence to the peak in the $dI_D/dlog_{10}t$ signal.

In Fig. 6.7 we report the emission time constants extracted from simulated DCTs acquired at different T_{BP} and P_D. Particularly, we can see three well-spaced τ curves which correspond to the three different T_{BP} levels considered. Moreover, two main observations on τ dependencies can be made: (i) τ reduces with increasing T_{BP}, and (ii) τ reduces with increasing P_D. These dependencies are expected, since both are a direct consequence of thermal dependent emission form Fe-traps [25]. In fact, a higher P_D yields an increase in the self-heating effect, causing device temperature to increase. An increase in T produces a speed-up in the thermally activated emission process, leading to a reduced τ [36].

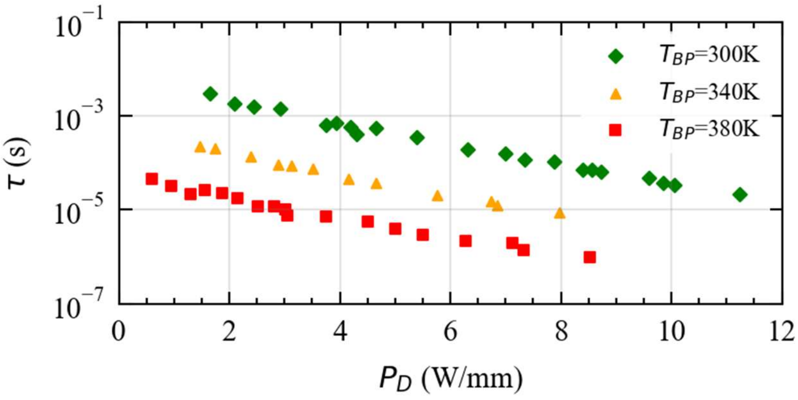

Figure 6.7: τ vs P_D extracted from DCTs.

6.4 Temperature Estimation and Discussion

At this point we employed the optimization algorithm for the extraction of the parameters of interest. To this end, Trust Region Reflective (TRR algorithm [32, 33] (implemented in Python) was applied for non-linear regression. Fig. 6.8 shows the comparison between the emission time constants directly extracted from DCTs and those predicted by the model after the optimization.

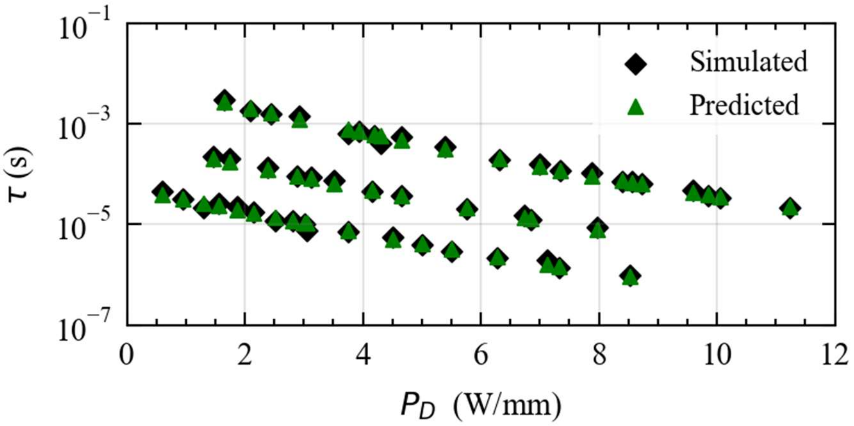

Figure 6.8: Comparison between simulated and predicted τ vs P_D.

A reasonable agreement is observed, meaning that the model parameters (minimizing CF) are a good estimate of the actual ones.

The parameters extracted with the TRR algorithm are now employed for temperature estimation. Temperature of the simulated device was also estimated by means of the McAlister method [5]. This way we provide a means of comparison for assessing the accuracy of the proposed technique. Fig. 6.9 shows the actual peak temperature (T_{peak}) provided by the simulator and the corresponding temperature estimated with the McAlister and the proposed method.

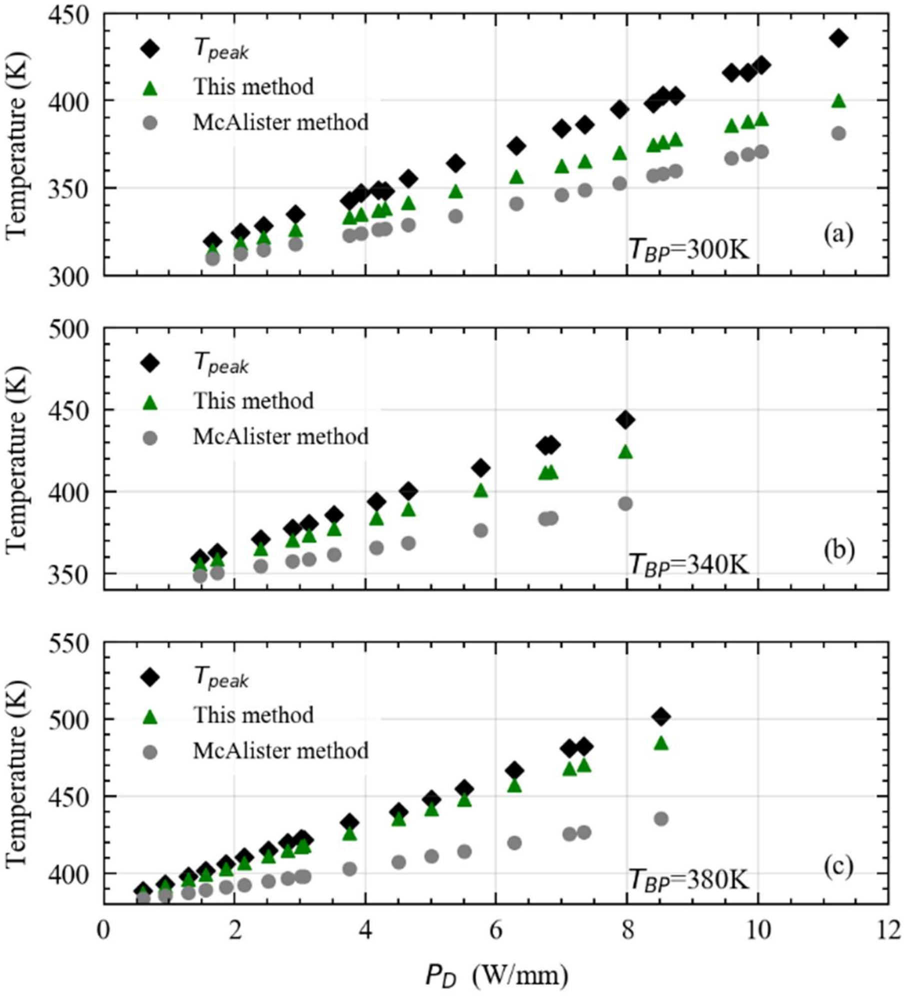

Figure 6.9: Comparison between the peak temperature obtained from simulations and the one estimated through the McAlister's method and the proposed technique for three different T_{BP}.

The McAlister method is known to significantly underestimate the peak temperature [7] and this is confirmed by the results obtained in this work. On the other hand, the proposed method allows to estimate a temperature which is closer to the peak one. However, even with the proposed method, we have an underestimation of T_{peak}. This is due to the finite distance between the ionized Fe-traps concentration peak and the temperature hotspot, which makes T_{Fe} slightly lower than the actual T_{peak}. This can be appreciated by comparing the temperature (T) and trapped charge (N_{FE}^{-}) distributions in the device's active region (see Fig. 6.10).

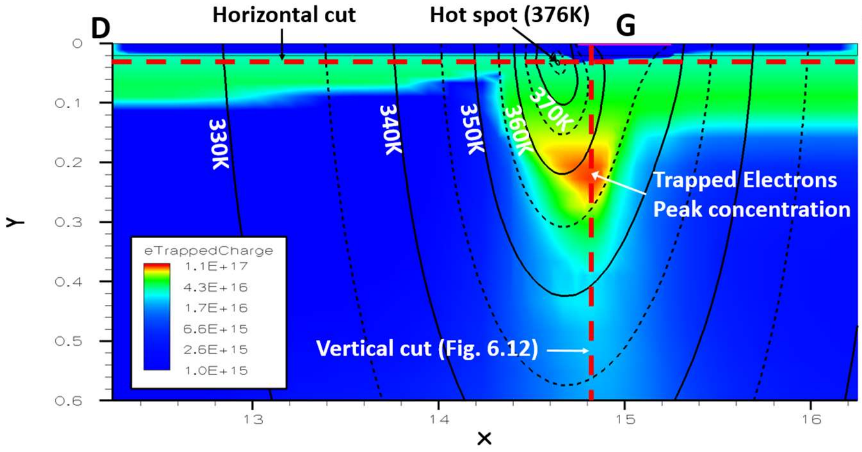

Figure 6.10: Contour Plot of temperature and trapped charge concentration in the device (P_D = 6.5 W/mm, T_{BP}= 300 K). We highlight horizontal and vertical cuts along which temperature and trapped charge profiles are evaluated.

As expected, the largest concentration of trapped charge is located under the gate edge towards the drain terminal of the device [21], close to the region where the temperature peaks [18]. However, the results in Fig. 6.10 highlight that the largest concentration of ionized Fe-traps is not perfectly aligned with the point of maximum temperature on both X and Y directions.

In order to quantify this difference, we identify the X and Y coordinates at which the peaks in T and N_{FE}^- occur. Particularly, the maximum temperature occurs close to the 2-DEG, while ionized Fe-traps are concentrated deeper in the GaN buffer layer (see Fig. 6.10). Thus, T_{peak} can be extracted from the T profile in the lateral direction (X) close to the AlGaN/GaN interface (see Fig. 6.10). This provided T_{peak} = 376 K at P_D = 6.5 W/mm, T_{BP} = 300 K as reported in Fig. 6.11.

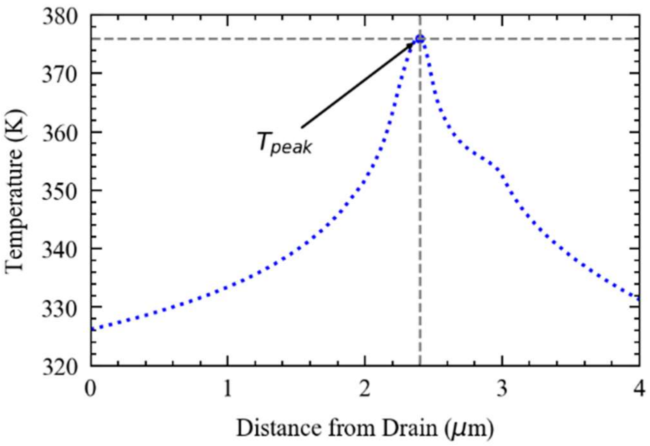

Figure 6.11: Temperature profile close to the AlGaN/GaN interface along the horizontal-cut as function of the distance from the drain terminal (P_D = 6.5 W/mm, T_{BP} = 300 K).

On the other hand, the T and N_{FE}^{-} profiles along the vertical direction (Y) can be used for estimating the temperature experienced by deep-levels (T_{Fe}).

By considering the vertical profiles of T and trapped charge reported in Fig. 6.12, we observe that the respective peaks occur at different distances from the 2-DEG.

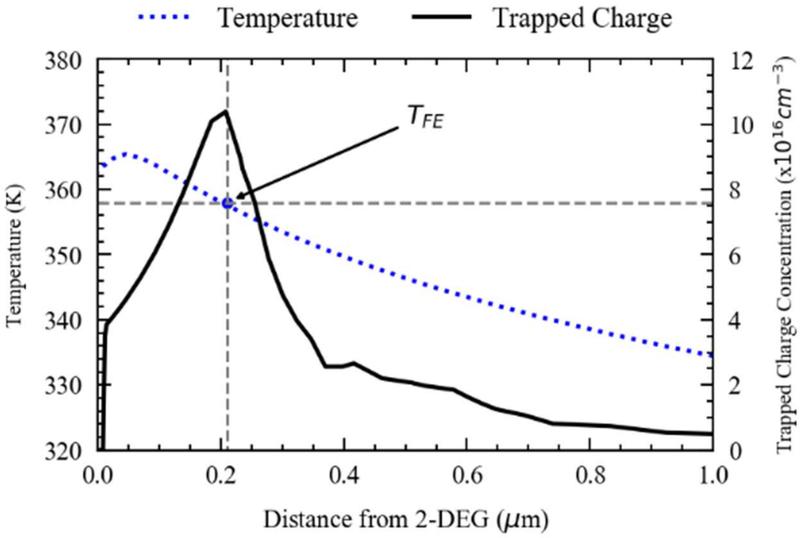

Figure 6.12: Temperature and Trapped charge profiles as function of distance from the 2-DEG (P_D = 6.5 W/mm, T_{BP} = 300 K) along vertical cut.

The misalignment between temperature and ionized trap concentration peaks, is the reason for the error in T_{peak} estimation. In fact, the actual temperature experienced by Fe-traps in the point of peak ionized trap concentration (i.e., T_{Fe}= 358 K) is ~18 K lower than T_{peak} = 376 K (T_{BP} = 300 K, P_D = 6.5 W/mm). This error is consistent with the estimation error observed in Fig. 6.9, indicating that the proposed technique accurately measures the temperature in correspondence of the Fe-traps location (T_{Fe}). This suggests that, similarly to μ-Raman technique, numerical simulations may be used to correct T_{est} (~T_{Fe}) and find a better estimate for T_{peak} [19], further reducing the estimation error.

Nonetheless, as it is, the error associated with the proposed method is relatively low compared to conventional electrical methods, (e.g., McAlister method) while it is comparable to the one of optical methods and Gate resistance temperature detector (RTD) technique [7]. To make this clearer, we reported in Fig. 6.13 the estimation error ($\varepsilon_E = T_{peak} - T_{est}$) provided by different electrical and optical methods.

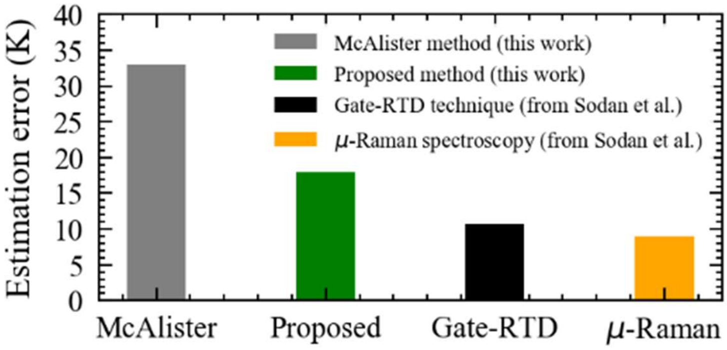

Figure 6.13: Estimation error obtained in this work for McAlister's method and Proposed method compared with those reported in literature for Gate-RTD technique and μ-Raman Spectroscopy (P_D = 6.5 W/mm and T_{BP}= 300 K).

The results shown in Fig. 6.13 indicate that the proposed method allows to significantly reduce the estimation error provided by the McAlister method. While the proposed technique shows an accuracy comparable to the one of μ-Raman and Gate-RTD techniques, conversely to these it does not require any special sample preparation; as such, it can be directly employed on both packaged and on-wafer devices.

As final remark, we observe that the proposed technique can be applied to any electron device provided that it is influenced by trap dynamics in such a way that DCTs can be clearly associated to a single carrier emission process, so that Arrhenius equation applies. To this end, specific bias conditions could be required (see [24] for the case of Fe-doped AlGaN/GaN HEMTs), which hence needs to be characterized prior to the application of this technique.

6.5 Conclusions

A novel method for estimating the temperature in semiconductor devices was successfully proposed. To the best of the author knowledge, this is the first time that the thermally activated emission process from electron traps is used for estimating the temperature in the device active region. To make it possible, two important conditions must be verified: (i) the trap states whose emission process is monitored should be located as close as possible to the point of maximum temperature in order to achieve a reasonable resolution and (ii) the mutual correlation between emission time constant and temperature must be well described by the Arrhenius equation. These conditions have been verified for the traps considered in this study, but other trap states presenting a similar behaviour could be in principle exploited for this scope. For the case presented in this dissertation, results indicate that the proposed method allows to significantly reduce the estimation error provided by conventional McAlister method, while showing an accuracy comparable to the one of μ-Raman and Gate-RTD techniques without the need for specific sample preparation. This is extremely important for the implementation of the method, making it possible to apply it on on-wafer and packaged devices.

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7 Conclusions and Outlook

7.1 Conclusions

During this thesis, the activity carried out on the characterization of WBG semiconductor devices was presented. Particularly, we focused on charge trapping analysis, which is still one of the most addressed issues in both SiC and GaN technology. Many experimental results, showed in this thesis, identify traps as the main responsible for the degradation of devices performances, stability and reliability. The traps analysis was conducted by means of different electrical characterization techniques and many original results have been obtained. A novel measurement setup for the on-the-fly characterization of V_{TH} and R_{ON} drifts in packaged SiC and GaN devices was developed, thus enabling the study the degradation of these two key parameters under conventional switch-mode operation. The results obtained highlighted V_{TH} drifts as the main source of instabilities in SiC MOSFETs, mainly due to traps at the interface between the oxide (SiO_2) and the semiconductor (SiC). On the other hand, a significant instability was observed on the on-state resistance of GaN-based power HEMTs subjected to off-state stress conditions, that was ascribed to the emission holes from Carbon-related buffer traps. The effect of the applied drain voltage stress on the R_{ON} degradation showed two interesting effects: (i) the emission process responsible for dynamic-R_{ON} speeds-up while increasing the off-state voltage applied and (ii) the magnitude of the degradation presents a non-monotonic trend with the applied stress voltage. The first effect was explained by the field-enhanced emission characterizing Coulombic centers like C-related acceptor traps, whereas the partial dynamic-R_{ON} recovery observed at relatively high voltages was explained through impact-ionization generated holes compensating negatively ionized acceptors in the gate-drain access region. This study highlighted the fact that the introduction of Carbon-dopants in the GaN buffer layer could be source of serious degradation phenomena in GaN-based power HEMTs, but it is needed for improving the blocking capabilities of power devices. A different approach that can used for rendering the buffer semi-insulating is to exploit iron-doping. Nevertheless, this type of doping still introduces deep-traps in the GaN band-gap which affects the stability of GaN HEMTs for RF applications. The role of these deep-levels on the time-dependent breakdown voltage in said devices has been studied by means of Pulsed I-V characterizations, whereas the physics governing the charge capture/emission processes from these traps have been investigated through current transient measurements. Particularly, the effect of (i) bias conditions, (ii) electric field and (iii) device self-heating on the emission process from Fe-traps were studied. The former analysis highlighted the importance to properly chose the bias conditions in order to correctly extract the traps parameters from the Arrhenius plot, while the study on the electric field effect allowed us to exclude the Poole-Frenkel effect as a mechanism affecting the dynamics of Fe-traps in GaN. Conversely, it was demonstrated that an increase in temperature due to self-heating effects could accelerate the emission process form said traps. This experimental evidence was extremely important for the development of a novel technique for estimating the temperature in semiconductor devices. In fact, the thermally activated emission process from electron traps is used for estimating the temperature in the device active region. For the case presented in this dissertation, results indicate that the proposed method allows to significantly reduce the estimation error provided by conventional McAlister method, while showing an accuracy comparable to the one of μ-Raman and Gate-RTD techniques. This makes the proposed method a valid alternative to state of the art techniques for temperature estimation in semiconductor devices, which is a very difficult task that typically requires complex systems for reaching good accuracies.

7.2 Outlook

The results presented in this thesis refers to two of the most promising WBGs technologies available at present: SiC and GaN. These technologies are expected to dominate the market for power and radio-frequency applications in the next few years, since they are reaching a good level of maturity and production costs are decreasing. Nevertheless, novel WBGs materials are coming into play, like Gallium Oxide (Ga_2O_3), Aluminium Nitride (AlN) and the more exotic diamond. These materials are typically referred to as ultra-WBG semiconductors and, theoretically, they could outperform both SiC and GaN technologies. Even if these technologies are still non-mature to compete with SiC and GaN on the market, in the future they will probably be considered as a valid alternative to the actual WBGs. Nevertheless, trapping phenomena may limit well below expectations their performances, making it difficult to reach their theoretical limit. Accordingly, an accurate characterization of these trapping effects will be of primary importance even for these up-coming technologies and novel techniques would be probably required. In fact, each technology presents its own peculiarity and it is always important to update the measurement setup in order to correctly characterize traps state and related issues. In this scenario, the characterization of WBGs and UWBGs will be fundamental in the future of power electronics, to guarantee always better performances and reduce size, costs and power consumption of electronic equipments.

List of Publications

List of published contributions covered in the PhD thesis (in chronological order).

Journal Articles

[1] M. Cioni et al., ‘Evaluation of VTH and RON Drifts during Switch-Mode Operation in Packaged SiC MOSFETs’, *Electronics*, vol. 10, no. 4, p. 441, Feb. 2021, doi: 10.3390/electronics10040441.

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Conference Proceedings

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