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UNIVERSITÀ DEGLI STUDI DI MODENA E REGGIO EMILIA

UNIVERSITÀ DEGLI STUDI
DI MODENA E REGGIO EMILIA

PhD Course in
Information and communication technologies (ICT)

XXXVIII Cycle

Characterization and TCAD modelling of GaN devices for switching applications

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Academic Year 2024/2025

Table of contents

Abstract .... **I**

1 Introduction **1**

1.1 GaN properties and AlGaN/GaN heterojunction 4

1.2 Solutions for enhancement-mode GaN HEMTs 13

1.3 Breakdown improvement (gate, buffer & field-plates) 17

1.4 Traps, dynamic effects and dynamic characterizations 23

1.5 Outline 30

References - Chapter 1 .... **31**

2 Effect of Mg activation on pinch-off voltage **35**

2.1 Devices under test 35

2.2 TCAD simulations of p-GaN effect 37

2.3 Gate capacitance measurements and interpretation 41

2.4 Experimental results 43

2.5 Conclusions 50

References - Chapter 2 .... **52**

3 High-temperature behaviors **54**

3.1 Devices under test and experimental setup 56

3.2 High Temperature Behavior of Static Ron 57

3.3 Temperature Effect on Dynamic RON-degradation 65

3.4 Conclusions 69

References - Chapter 3 .... **70**

4 Drain and gate static reliability study **72**

4.1 TCAD simulation study of HTRB-induced current collapse 72

4.2 Screening method for preliminary gate robustness assessment 78

4.3 Conclusions 88

References - Chapter 4 .... **89**

5 Bidirectional p-GaN HEMTs **92**

5.1 DC simulation & characterization 95

5.2 AC simulation & characterization 102

5.3 Gate robustness 111

5.4 Conclusions 112

References - Chapter 5 .... **112**

6 Conclusions **114**

List of Publications……………………………………………………………...........116

Abstract

In this work, simulations and experimental characterizations of normally-off p-type gate GaN-based HEMTs for switching power applications are reported and analyzed, in order to get more accurate understanding of the underlying physical mechanisms resulting in the macroscopic behavior of devices under test. In particular, the first portion of the thesis deals with the main properties characterizing Gallium Nitride and the discussion about the relevance of studying GaN-based devices and their behavior. On the second part, the focus is posed on 100V p-GaN HEMTs and the role of magnesium doping is deeply investigated through TCAD simulations and experiments. Indeed, p-doping of the gate module is obtained through magnesium doping, but the effect of its level and its electrical activation is of great relevance to fully comprehend the device performances both in off and on states. To this purpose, chemical analyses of some samples are also presented since their results are key to integrate the understanding obtained from simulated and experimentally measured electrical data. Another important topic that is discussed in the following chapter is the study of on-state resistance at high temperatures both in static and dynamic conditions. In fact, when switching devices are working in power applications at high frequencies, they suffer both from conduction and switching losses that lead to self-heating of the device itself. Therefore, the accurate analysis of the factors that can influence the temperature behavior of the on-resistance (which is one of the main figures of merit) is crucial to the improvement of the actual high-temperature performances of p-GaN HEMTs during application conditions. Different solutions are proposed in order to reduce the de-rating of the R_{on} at high temperatures, and it is proved that, at steady state, the relative dynamic increase of the on-resistance induced by high drain voltage is insensitive to temperature, in the case of single buffer-related degradation mechanisms like carbon-induced hole redistribution. In the last two chapters, the focus is shifted towards 650 V rated p-GaN HEMTs. In particular, the drain and gate reliability of these devices are investigated: at first, TCAD simulations are exploited to understand experimental results coming from drain reliability tests performed on different families of devices; then, a gate screening procedure for the preliminary evaluation of the gate robustness is presented and applied to p-GaN HEMTs with different fabrication process flows, showing advantages and drawbacks. Finally, two-gate devices, namely bidirectional p-GaN HEMTs are presented and DC/AC TCAD simulations on these devices are performed and described. Then, the simulated data are compared to experimental measurements, showing also the comparison with the results obtained on one-gate unidirectional p-GaN HEMTs.

1 Introduction

In the context of the semiconductor industry, Silicon is still by far the most used primary material for chip fabrication, due to its natural abundance, good elecro-mechanical and optical properties, high quality native oxide and very good manufacturability maturity coming from years of research, development and production. However, for some specific applications like power/RF electronics, requiring high efficiency and high-power density, new materials, namely wide bandgap (WBG), are nowadays gaining increasing interest and market share, thanks to their better intrinsic properties, fabrication cost reduction and performance/reliability improvement. The two most relevant WBG semiconductors as of today are both binary compounds: the first and most mature in the market is the Silicon Carbide (SiC) while the second one, already available in the market but still less present, is the Gallium Nitride (GaN), as shown in Figure 1.1.

Figure 1.1: Market shares of Silicon, SiC and GaN devices, actual data up to 2025 and expected trend up to 2030 [1].

Even if the market presence of GaN devices is still dominated by consumer applications (mainly fast chargers), significant growth in the market request for GaN-based devices is expected for the upcoming years, mainly driven by automotive (e.g., car electrification), data centers (e.g., cloud and servers for artificial intelligence), renewable energy applications and 5G/6G base stations, as reported in Figure 1.2.

Figure 1.2: Market segmentation for GaN-based devices, actual data up to 2025 and expected trend up to 2027 [1].

The study of GaN-based devices and their behavior under determined conditions is the focus of this thesis, which represents one of the many efforts (as shown in Figure 1.3) in the improvement of the global understanding of this technology, aimed at a more efficient implementation of the same.

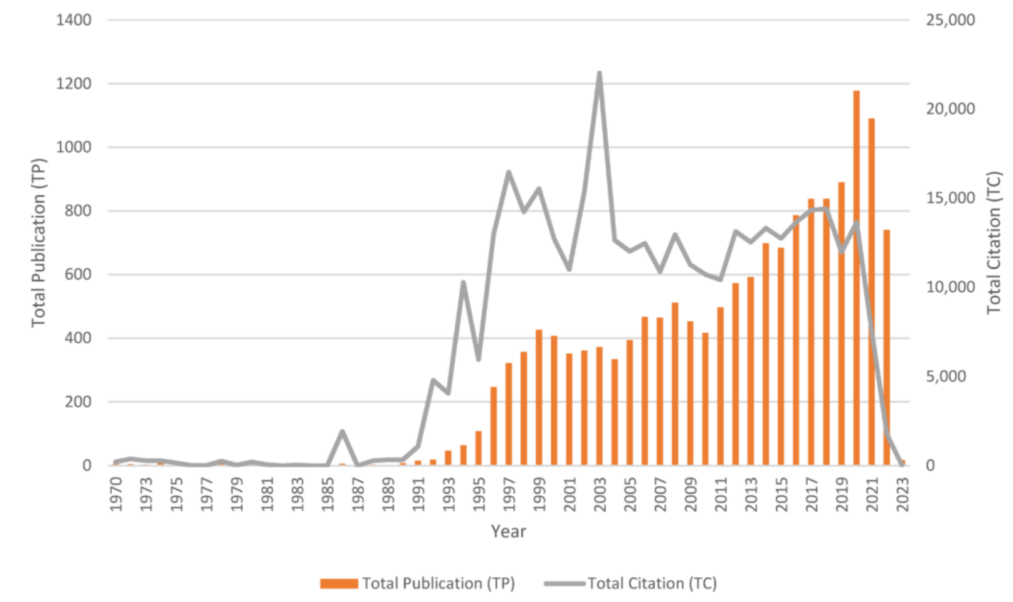


Figure 1.3: Number of publications and citations about GaN-related topics up to 2022 [2].

To start, it is worth giving some historical information regarding the chronological development of GaN technology [3], showing the main milestones and achievements that allowed improvements in theoretical understanding and the overcoming of some technical limitations in the practical realization of GaN-based devices:

- 1932: The very first polycrystalline GaN was synthesized by making react ammonia and liquid gallium metal at high temperatures (900-1000 °C) [4].
- 1972: Pankove group realized the first gallium nitride-based blue light detector [5]
- 1986: Amano et al. obtained the growth of epitaxial GaN layers from metalorganic chemical vapour deposition (MOCVD) with good crystallographic quality by introducing an AlN nucleation layer at the interface with substrate [6].
- 1989-1992 Amano et al. obtained p-type conductivity in GaN by activating Mg dopants by low-energy electron irradiation [7]. Moreover, annealing above 600 °C in nitrogen atmosphere was also found to induce electrical activation of p-GaN layers [8].
- 1991-1993: Asif Khan et al. realized the first AlGaN/GaN heterojunction through MOCVD and observed the first 2DEG [9].
- 1994: Nakamura group obtained the first high brightness blue LED, using InGaN/AlGaN double-heterostructures [10].
- 1996: The first blue laser diode, LD, (405 nm) based on InGaN quantum wells (QWs) was reported by Nakamura et al. [11].
- 1997-1999: Bernardini et al. determined the spontaneous and piezoelectric polarization constants of nitrides [12]. Ambacher et al. proposed a model to analytically describe the 2DEG properties in AlGaN/GaN heterostructures [13].
- 2005: Nitronex Corp. introduced the first depletion-mode RF HEMT transistor made with GaN grown on silicon wafers.
- 2006: Sony released Blu-ray Disc format based on 405 nm LDs.
- 2007-2009: Uemoto et al. from Panasonic demonstrated the first normally-off HEMT based on the p-GaN gate technology [14]. EPC announced the commercialization of the first devices based on this technology.
- 2012: AlGaN/GaN heterostructures grown on 200 mm Si(111) substrates were demonstrated by Tripathy et al. [15]. The possibility to grow such heterostructures on large-area Si wafers opened the way to integrate GaN HEMT device fabrication in Si CMOS fabs.

- 2014: The Noble Prize in Physics was assigned to Isamu Akasaki, Hiroshi Amano, and Shuji Nakamura for “the invention of efficient blue light-emitting diodes which has enabled bright and energy-saving white light sources”.

- 2015–2017: The first high-voltage (600 V) normally-off GaN HEMT solution, based on the “cascode” configuration, is released to the market by Transphorm. Moreover, the progresses in the technology of p-GaN gate HEMTs resulted in the first fully industrial qualified “true” normally-off devices from Panasonic and Infineon. HRL Laboratories in Malibu, California demonstrated a GaN power IC to realize the full benefits of GaN electronics at a low cost [16].

- 2025: Navitas Semiconductor released the world's first production-released 650V bi-directional GaN HEMTs integrating two back-to-back GaN switches into a single IC with an active substrate clamp for high efficiency.

As briefly summarized before, the journey of GaN technology is almost 100 years old but still some aspects need further investigation, and improvements are being made year after year with the contribution of many scientists all over the world, companies and startups.

1.1 GaN properties and AlGaN/GaN heterojunction

Gallium nitride is a compound semiconductor formed by Gallium (atomic number 31, group III of the Mendelev periodic table, show in Figure 1.4) and Nitrogen (atomic number 7, group V of the Mendelev periodic table).

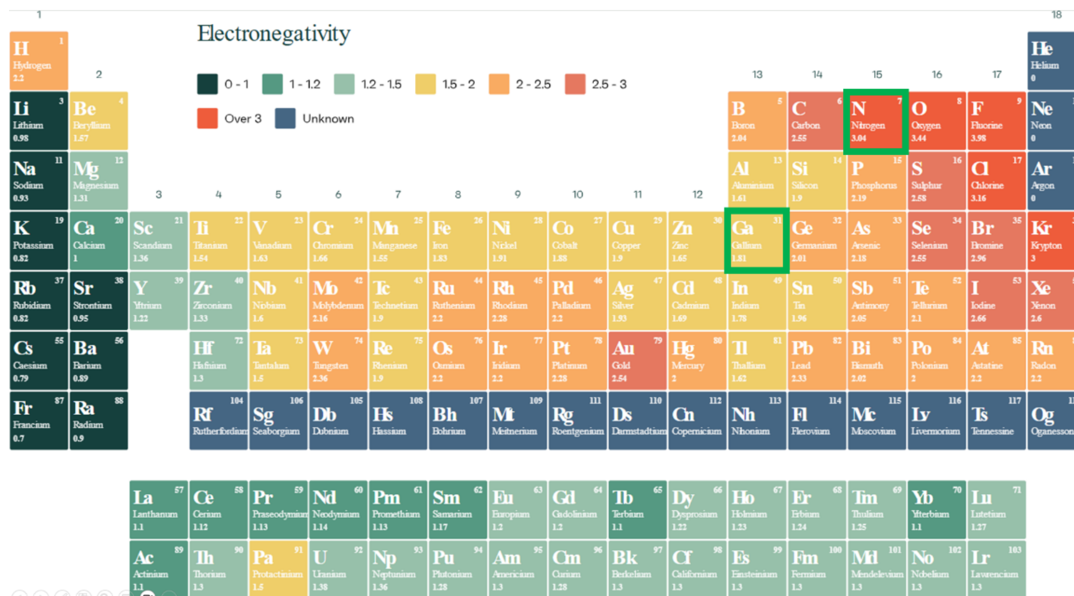


Figure 1.4: Periodic table of elements with heat map of electronegativity, highlighting Gallium and Nitrogen [17].

It belongs to the class of III-V semiconductors, which involves other compounds whit similar characteristics, also used in electronics, like GaAs, AlN, InP, etc., usually characterized by a direct bandgap (useful in optoelectronics). GaN itself is a direct bandgap material and this explains how it has been used in photonic applications to begin with.

The crystal structure of the GaN compound is formed by gallium and nitrogen atoms arranged in a hexagonal structure, called wurtzite (show in Figure 1.5), which lacks inversion symmetry. The noncentrosymmetric lattice structure together with the electronegativity difference between Gallium and Nitrogen is the responsible of the spontaneous polarization effect making GaN a polar semiconductor.

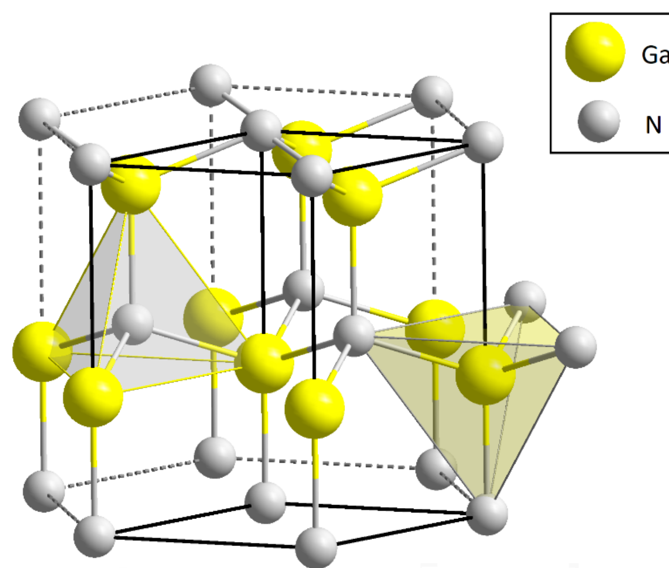


Figure 1.5: Hexagonal (Wurtzite) crystal structure of Gallium Nitride [18].

In particular, depending on whether the termination surface is represented by Gallium (Ga-polar or Ga-face) or Nitrogen (N-polar or N-face), different physical, chemical, and electrical properties characterize the surface of GaN. Figure 1.6 schematically reports these two different crystal polarities. In the following, the reference will always be the Ga-face, unless specified otherwise.

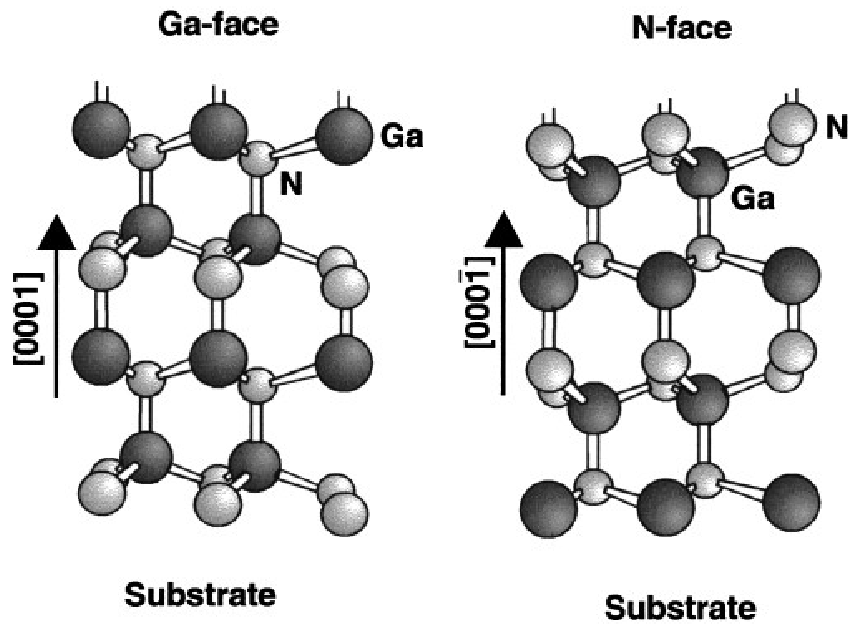


Figure 1.6: Crystal lattice structure of Ga-face and N-face Gallium Nitride [19].

GaN is very well-suited for building high voltage and high frequency transistors: this is because it is characterized by high saturation velocity, high thermal stability and high breakdown voltage (thanks to its wide bandgap $E_g \approx 3.4$ eV, leading to high critical electric field) as shown in the radar chart of Figure 1.7. Here, it is worth mentioning that the reported material properties may vary between different references. However, the graph gives an idea of the great potential of this material.

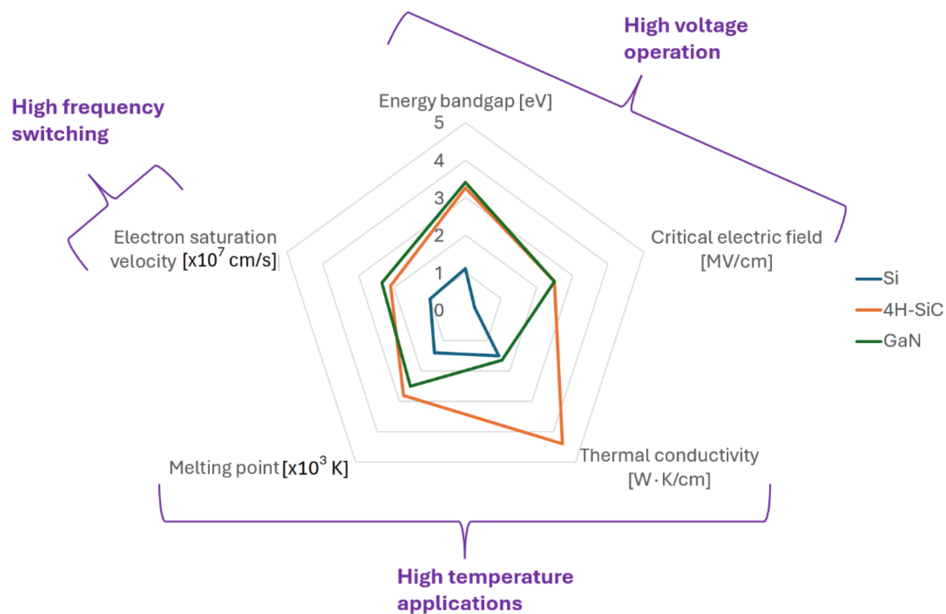


Figure 1.7: Radar chart with comparison of main material parameters for GaN, 4H-SiC and Silicon.

In order to to have a better comparison between different semiconductors, two figures of merit (FOMs) are usually adopted, namely the Johnson FOM [20] (for benchmarking high frequency devices) and the Baliga FOM [21] (for comparing high power devices). In particular, Johnson's figure of merit (JFOM) is defined as:

$$JFOM = V_B \cdot f_T \approx \frac{E_{crit} \cdot v_{sat}}{2\pi} \quad (1.1)$$

While Baliga's figure of merit (BFOM) is expressed as:

$$BFOM = \epsilon \cdot \mu \cdot (E_{crit})^3 \approx \frac{4V_B^2}{R_{on,sp}} \quad (1.2)$$

The values of both JFOM and BFOM normalized to Silicon are reported and compared in Table I. Also in this case, reported values may slightly differ based on the references.

Figure of merit	Si (baseline)	4H-SiC	GaN
Baliga	1	300-800	800-3000
Johnson	1	15	30

Table I: Comparison of Johnson and Baliga FOMs for GaN, Si and 4H-SiC.

These metrics clearly show the superior properties of GaN and SiC with respect to Silicon in both high speed and high voltage applications, with GaN having an edge on both FOMs. Actually, given the specific geometry of existing GaN and SiC device structures (lateral vs vertical), GaN is often preferred for lower voltage/higher frequency and SiC for higher voltage/power. Another metric which is usually considered for comparing different semiconductor materials is the Baliga relationship between on-resistance and breakdown voltage, in the approximation of a unilateral and abrupt junction, which was first studied in silicon devices [22]. This metric defines which is the minimum on-resistance for a given breakdown voltage depending on material characteristics, like the critical electric field and the carrier's mobility (the larger the critical E-field or the mobility, the lower the on-resistance):

$$R_{on,sp} \approx \frac{4V_B^2}{\epsilon \cdot \mu \cdot (E_{crit})^3} \quad (1.3)$$

This relationship allows to easily compare the RON-VB trade-off for different materials, as

reported in Figure 1.8.

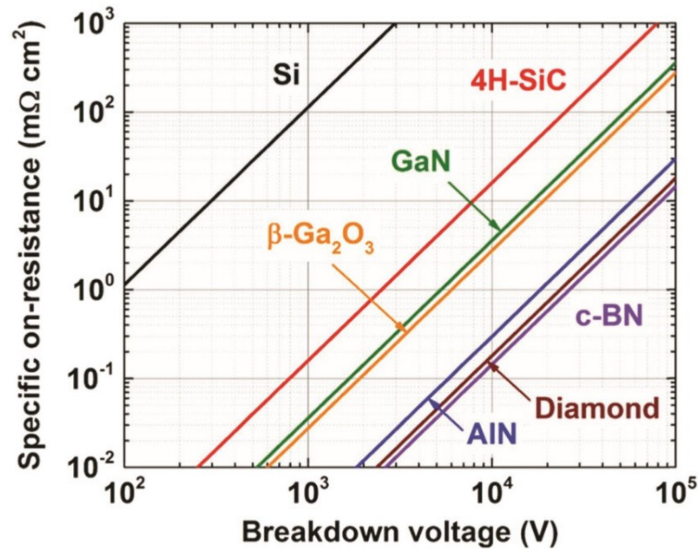


Figure 1.8: Specific on-resistance vs breakdown voltage for different semiconductor materials [23].

As can be seen, wide bandgap or ultra-wide bandgap (Ga_2O_3, AlN, Diamond) allow higher breakdown operation at the same on-resistance or lower on-resistance at the same breakdown voltage. This is obtained thanks to their large bandgap which results in higher critical electric field: in fact, the critical electric field and the bandgap are intrinsically linked, as the energy required to initiate avalanche breakdown is directly proportional to the energy gap between the valence band and the conduction band. Figure 1.9 depicts the critical breakdown electric field versus the bandgap for various semiconductor materials.

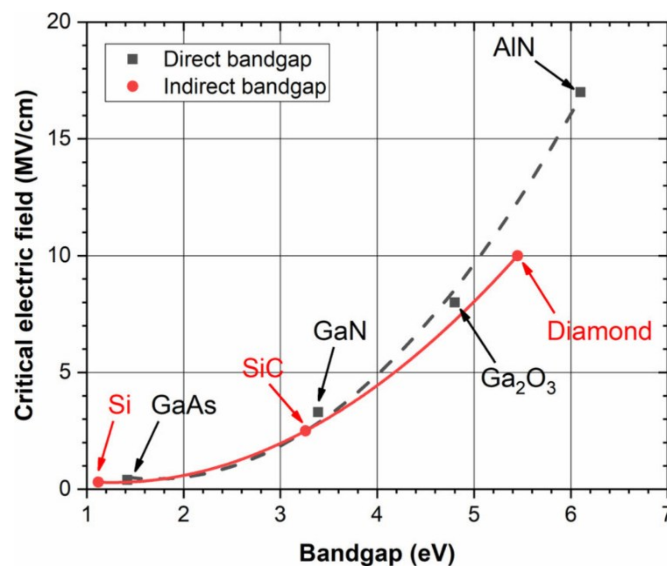


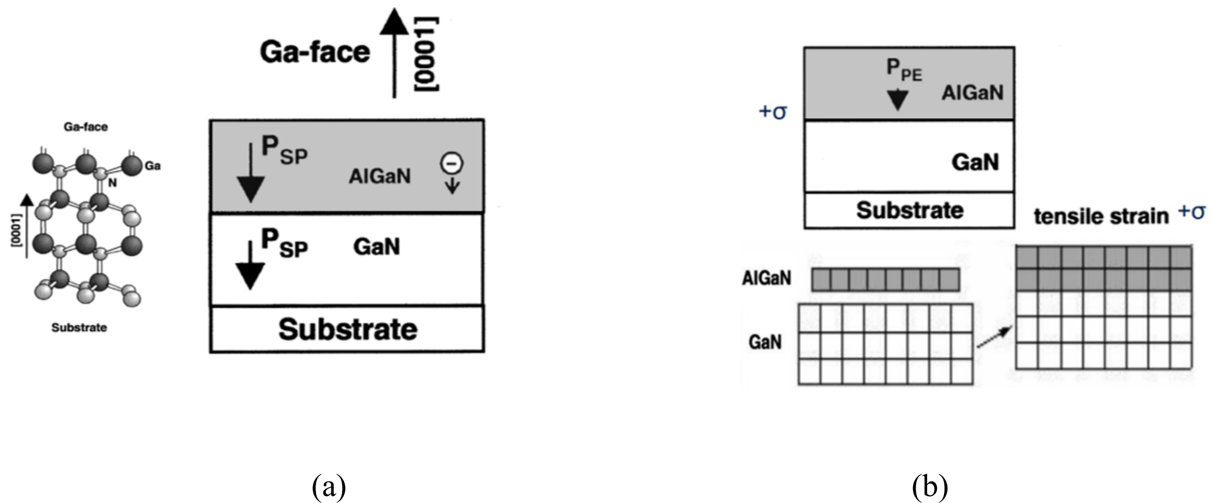
Figure 1.9: Relationship between critical electric field and energy bandgap for different semiconductor materials [24].

N-type conductivity transistors based on GaN are realized making advantage of the heterostructure for building the electron channel and the resulting devices are so called HFET (Heterostructure FET). The most common material used together with GaN for the heterostructure is the AlGaN, a ternary compound where some Gallium atoms are substituted by aluminum atoms (atomic number 13). Aluminum is characterized by a slightly different electronegativity with respect to Gallium and more importantly it features a different energy bandgap and a lower lattice constant. Consequently, when a thin AlGaN layer is grown on top of a thicker GaN buffer, a mechanical strain will be applied to the AlGaN. Therefore, for the AlGaN/GaN heterostructure, two polarization contributions must be considered:

1) **Spontaneous**, due to the crystal lattice structure and the electronegativity (slightly different between GaN and AlGaN).

2) **Piezoelectric**, due to the tensile stress applied to the thin AlGaN layer (induced by the difference in the lattice constants of AlGaN and GaN).

Figure 1.10 highlights both the spontaneous polarization and the piezoelectric polarization, in case of tensile strain on the AlGaN barrier layer.



(a) (b)

Figure 1.10: (a) Spontaneous and (b) piezoelectric polarization for AlGaN/GaN heterostructures [13].

Since AlGaN and GaN are then characterized by different overall polarization, a gradient exists at the heterointerface, which results in a positive charge density. This fixed positive charge creates a strong internal electric field that causes the energy bands to bend sharply. The band bending combined with the bandgap discontinuity between AlGaN and GaN creates a triangular-shaped potential well in the GaN layer right at the interface. As a result, a sheet electron concentration (two-dimensional electron gas, “2DEG”) is induced at the interface, as shown in

Figure 1.11.

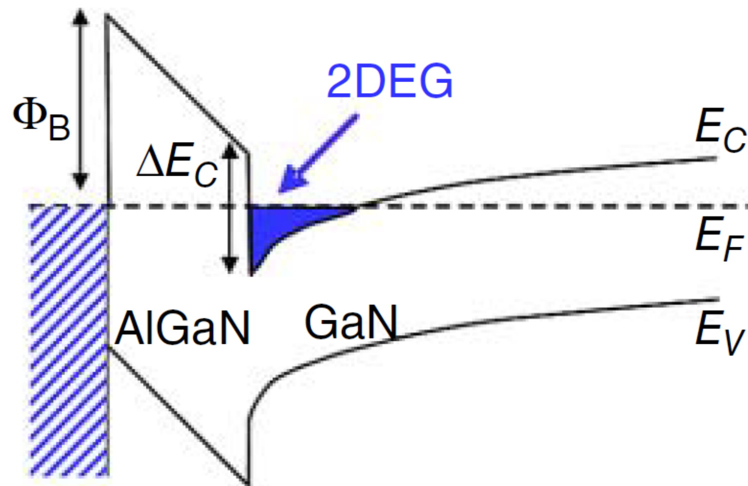


Figure 1.11: Energy band diagram of the AlGaN/GaN heterostructure with 2DEG formation at the interface.

The main advantage of the AlGaN/GaN system over other heterostructures (e.g., GaAs) is the fact that high 2DEG densities can be obtained even without intentional doping. This effect results in reduced carrier scattering and allows for very high electron mobility. Depending on the Aluminum content of the AlGaN layer and on its thickness, the induced 2DEG density can be modulated: in particular, increasing the Al content and the AlGaN thickness allows to obtain higher 2DEG concentrations, as shown in Figure 1.12.

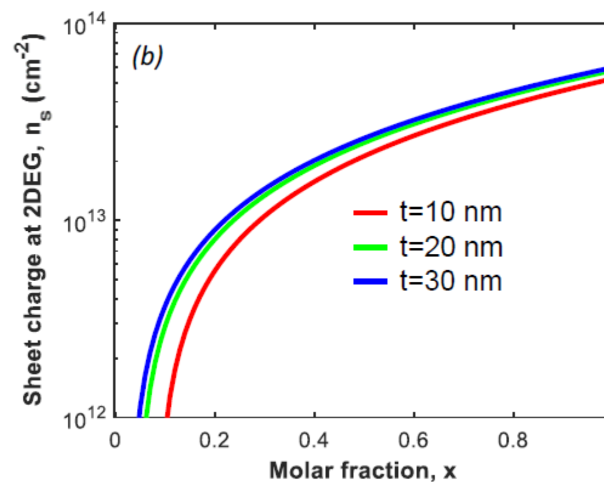


Figure 1.12: 2DEG density versus Al content in AlGaN for different AlGaN thicknesses [25].

Another important piece of information about the 2DEG that can be evaluated is mobility: as described in Figure 1.13, for low interface roughness, 2DEG mobility can reach up to 2000 $\frac{cm^2}{V\cdot s}$ at room temperature.

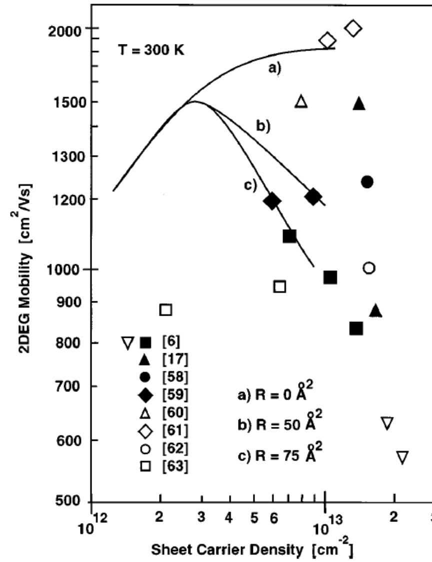


Figure 1.13: 2DEG mobility versus 2DEG density for different interface roughness [13].

Table II shows the comparison of typical electron mobility values at 300 K for GaN, Silicon and 4H-SiC: GaN exhibits the best performance (about +30% with respect to Silicon) and this is the reason why HFET are also called High Electron Mobility Transistors (HEMT). The specified ranges are just an indication since many factors can modify the actual mobility values.

Material	**Electron mobility [$cm^2/(V\cdot s)$]**
Si	1300-1500
4H-SiC	600-900
GaN	1500-2000

Table II: Comparison of electron mobility of GaN, Si and 4H-SiC.

By adding the three contacts (gate, source and drain) to the AlGaN surface, a full AlGaN/GaN HEMT can be obtained, as shown in Figure 1.14.

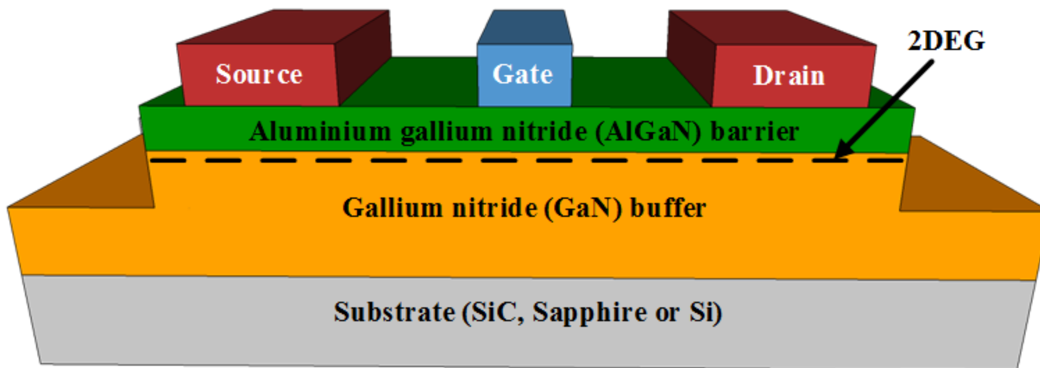


Figure 1.14: Schematic cross section of a GaN-based HEMT.

Another important advantage of GaN HEMTs over other transistors based on Silicon or SiC is the reduced value of capacitances (mainly output and reverse capacitance) which is reflected on lower switching losses (thanks to lower charge amount to be "moved"). In fact, high mobility enables much lower on-resistance for a given device size, allowing the realization of smaller transistors. Smaller physical size directly translates to lower parasitic capacitances (gate-drain, drain-source). Moreover, the 2DEG regions account for reduced capacitive contributions given their two-dimensionality. Figure 1.15 reports all the capacitive couplings among device terminals and 2DEG.

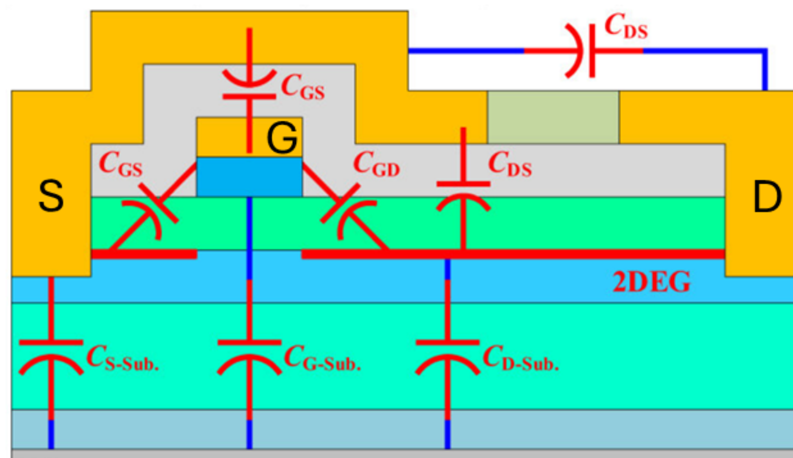


Figure 1.15: Schematic cross section of a GaN-based HEMT with details of capacitive contributions in off state at zero drain bias [26].

As mentioned before, given the polarizations effect at the heterointerface, the 2DEG will be present without the need of any gate bias. This means that the simple AlGaN/GaN heterostructure described fore leads to normally-on (depletion-mode, “D-mode”) devices, if no other technological tailoring is performed. In fact, even if the threshold voltage can be modified by changing AlGaN barrier thickness and Al content, this is not enough to tune the threshold voltage towards positive values.

1.2 Solutions for enhancement-mode GaN HEMTs

Normally-off (enhancement-mode, “E-mode”) devices are usually preferred for power applications, given their intrinsic fail-safe operation and compatibility with already existing Silicon drivers. Figure 1.16 includes the comparison between normally-on and normally-off devices in terms of I_D-V_G curve and threshold voltage. Driven by this important application requirement, four main solutions have been developed to achieve normally-off operation, i.e., to obtain a positive threshold voltage, for GaN-based HEMTs. In the following, the solutions are briefly described, discussing advantages and drawbacks.

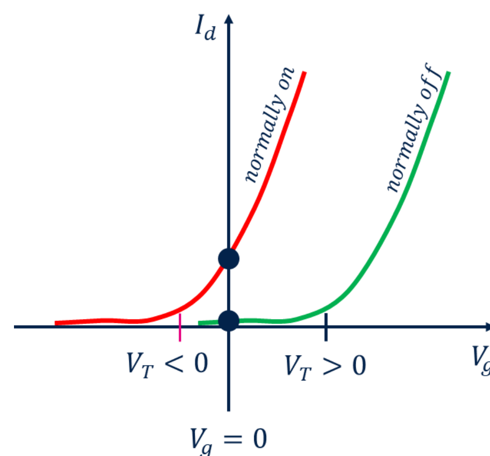


Figure 1.16: Comparison between linear transfer IV characteristics of depletion- and enhancement-mode transistors.

1) **Fluorine plasma treatment** (Figure 1.17): in this case, the idea is to apply a CF_4 plasma treatment in a reactive ion etching (RIE) system in order to selectively treat the gate region with negative fluorine ions. In fact, as soon as fluorine ions reach the AlGaN layer, the electrons of the 2DEG are depleted because of electrostatic repulsion. This solution has been proposed initially to move the threshold voltage towards positive values, but it is not used in practice because of many limitations. For example, in order to obtain a sufficiently positive threshold voltage, too high plasma power would be needed but, in that case, the etching damage of the process would increase scattering at the AlGaN/GaN interface, thus decreasing the 2DEG mobility and reducing too much the transconductance of the device. Moreover, fluorine ions can easily become trap centers

and strongly worsen nominal device performance.

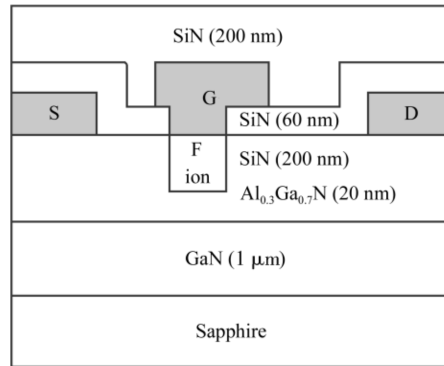


Figure 1.17: Schematic cross section of normally-off GaN HEMTs obtained through Fluorine implant [27].

2) **Recessed gate approach** (Figure 1.18 and 1.19): in this case, a trench is opened on the gate region into the AlGaN layer either reaching the heterointerface or leaving a very small thickness of AlGaN such that the induced 2DEG density is extremely low. In some embodiments, a dielectric layer is formed inside the trench prior to the gate metallization, in order to obtain a MIS-HEMT (Metal-Insulator-Semiconductor HEMT) structure with improved gate control. Given the relationship between 2DEG density and AlGaN thickness, the etch depth can be directly used to control the threshold voltage and high positive values can be easily obtained. Moreover, this solution offers wide gate voltage swing and reduced gate leakage. However, also in this case, there can be non-negligible detrimental effects, like the trade-off between on-resistance value and threshold voltage due to high channel resistance contribution and dynamic R_{on}/V_{th} increase due to interface quality and etching-induced damage.

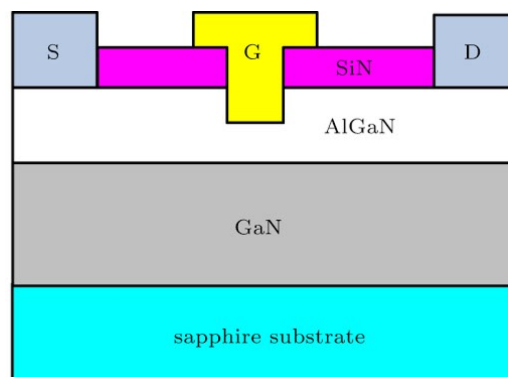


Figure 1.18: Schematic cross section of normally-off recessed-gate GaN HEMTs [28].

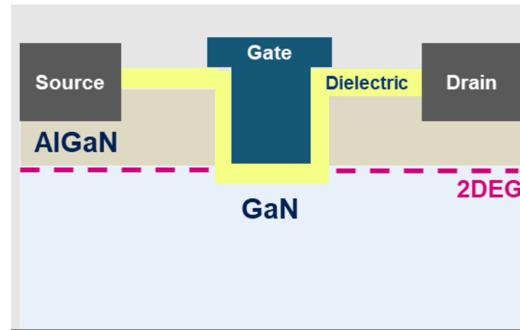


Figure 1.19: Schematic cross section of normally-off recessed-gate GaN MIS-HEMTs.

3) **Cascode configuration** (non-technological solution, Figure 1.20): this approach involves the connection of a high-voltage, normally-on GaN HEMT with a low-voltage enhancement-mode Si MOSFET, offering a high threshold voltage, making it an interesting solution for high-voltage applications (>200V). The same current flows in both devices when they are switched in on state and the blocking voltage is distributed between them when they are both turned off. This solution rather simplifies gate driving because it avoids direct driving of the GaN gate by cascading the GaN HEMT with a Si MOSFET, such that the output (drain-source) voltage of the MOSFET determines the input (gate-source) voltage of the GaN HEMT. However, this combination adds package complexity, introduces parasitic inductances impacting high frequency performance (limited to 1 MHz).

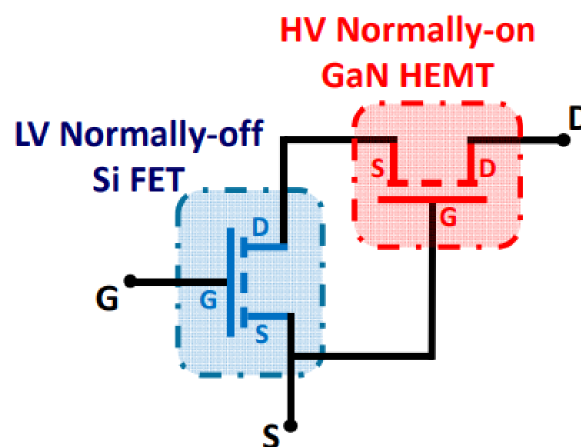


Figure 1.20: Schematic cross section of normally-off cascode GaN HEMTs [29].

4) **p-GaN gate** technology [29] (Figure 1.21): in this approach, a p-GaN layer (usually Mg-doped) is grown on top of the AlGaN layer and selectively removed outside of the gate region. In this way, the conduction energy band is lifted above the Fermi level at zero gate bias, meaning depleted 2DEG in the gate region. When the gate voltage is increased, the 2DEG under the p-GaN can be restored, achieving low on-state resistance. This is the most widely adopted solution but also in this case, some issues can be faced. First, the selective etching of the p-GaN layer can damage the AlGaN surface, affecting the 2DEG in access regions (gate-drain and gate-source). Then, magnesium doping can introduce trapping effects and defects, potentially increasing leakage current and limiting device reliability. Finally, it is worth mentioning that gate leakage is higher in the general case of Schottky contact between p-GaN and gate metal with respect to a MOS or MIS structure. Some embodiments leverage on this apparent drawback by making it a key feature of the HEMT, like in the case of ohmic contact between p-GaN and gate metal, where the gate leakage becomes really high (see Figure 1.22): in this case, the resulting devices (Gate Injection Transistors, "GITs") are turned on and off by gate current modulation and not by gate voltage control (gate driver must provide steady current).

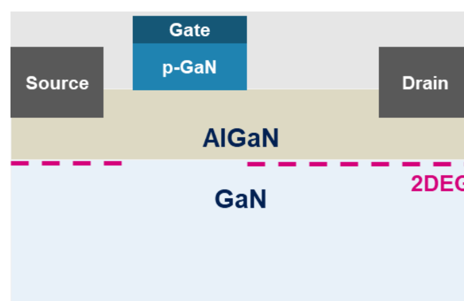


Figure 1.21: Schematic cross section of normally-off p-GaN HEMTs.

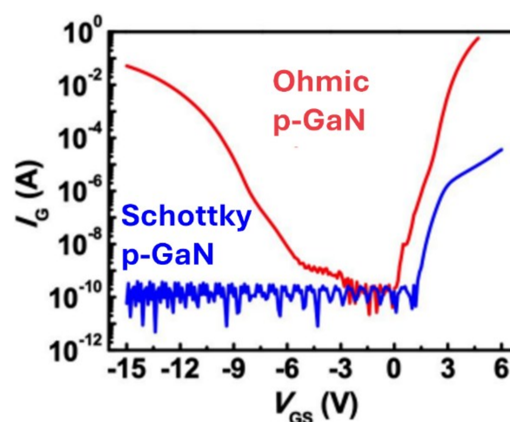


Figure 1.22: Comparison between typical gate leakage of Schottky and GIT p-GaN HEMTs [30].

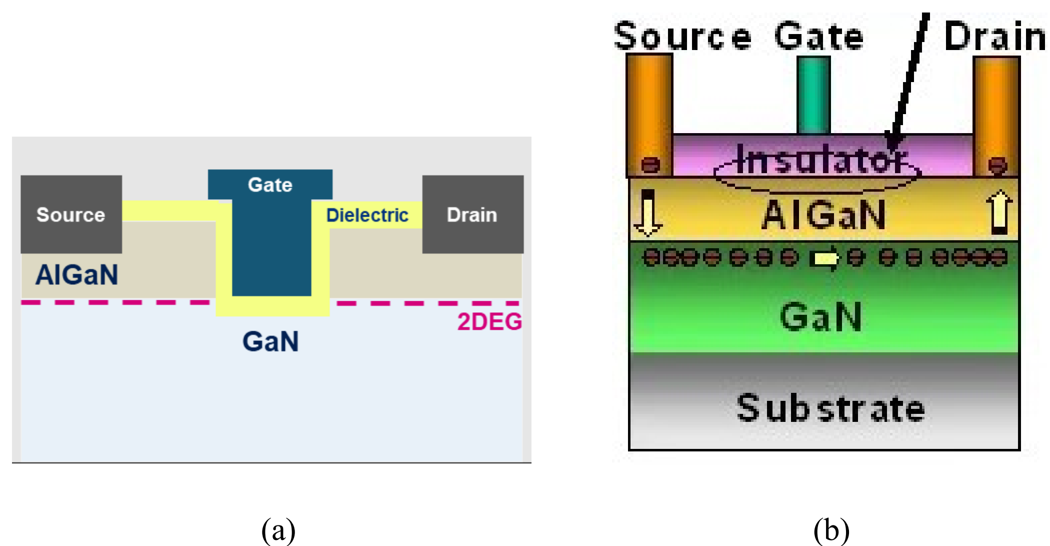
As of today, most semiconductor companies have chosen for either cascode or p-gate, with recessed technology still confined to research level.

1.3 Breakdown improvement (gate, buffer & field-plates)

In this section, different strategies to tune the breakdown and/or the leakage of either the gate or the drain of a GaN HEMT structure will be discussed.

1.3.1 Gate breakdown → MIS or insulated-gate HEMT

As mentioned before, the addition of an insulator under the gate metal is a very effective method for reducing gate current leakage (by several orders of magnitude, with respect to non-insulated gate HEMTs), both for recess-gate MIS-HEMT and for depletion-mode MIS-HEMT (Figure 1.23). This modification also results in significant increase of the gate breakdown voltage, as gate failure mechanisms are mainly related to the dielectric breakdown instead of avalanche or diode-like failures observed in Schottky gates. Therefore, depending on the dielectric permittivity and thickness, insulated gate GaN HEMTs can reach up to about 30 V of forward breakdown voltage, allowing a quite large voltage swing (e.g., 15 V). Another advantage of the gate insulation is that it allows to withstand larger electric fields peaks at the gate edge for high drain-source voltages in off state. Typical high-k materials, such as Al_2O_3, Si_3N_4 and HfO_2, can be used to create the insulated stack [31]. Of course, while gate breakdown can be improved, the dielectric interface can introduce trapping states, leading to threshold voltage shifts or unwanted hysteresis during high voltage switching. Regarding p-GaN HEMTs, gate reliability is a major concern since no gate insulation is present: this will be one the topics of the following chapters.



(a) (b)

Figure 1.23: Schematic cross sections of (a) E-mode MIS-HEMT and (b) D-mode MIS-HEMT structure.

1.3.2 Drain breakdown → Field-plates (FP)

The introduction of field plates is a common technique used in GaN-based devices [32]. A field plate consists of an extension (connected to the gate or source) of metal over a dielectric, as shown in Figure 1.24.

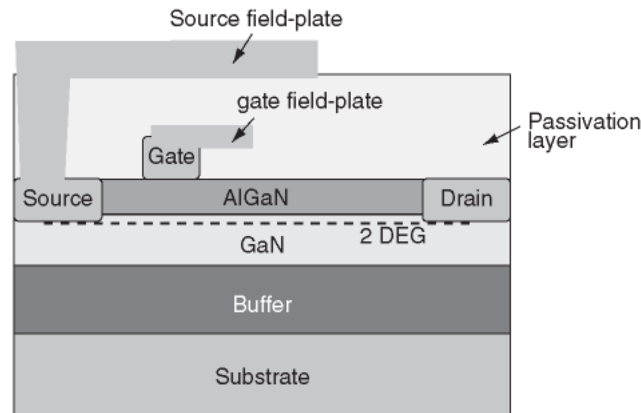


Figure 1.24: Schematic cross section of a GaN HEMT with gate and source field plates.

The role of field plates is to reshape the electric field in the structure, reducing the field peaks by spreading the potential drop over a larger distance. In a standard HEMT, at high drain-source voltage, the electric field is characterized by a sharp peak at the drain-side edge of the gate, a weak spot where device can fail. Therefore, it is important to limit large field peaks in order to improve the static and long-term robustness of GaN HEMTs. Figure 1.25 shows the effect of field plate introduction on the electric field.

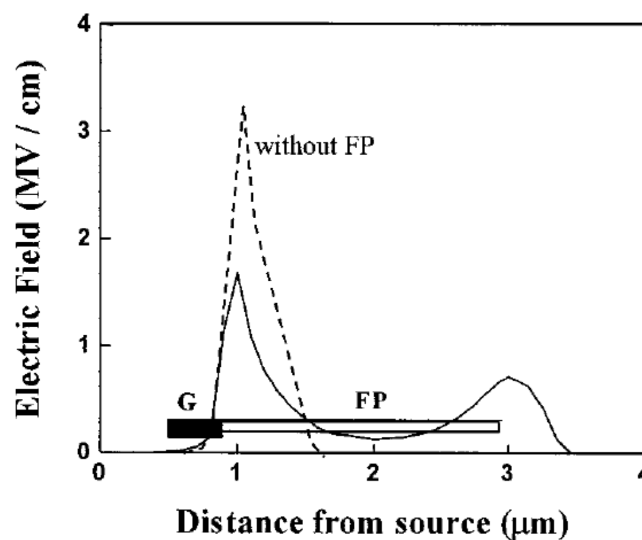


Figure 1.25: Electric field comparison along gate-drain distance with and without field plate introduction [33].

Moreover, a large electric field peak close to the gate can be the root cause of undesired threshold voltage shifts during switching. Therefore, this technique allows for drain breakdown voltage improvement and also limited drain-induced threshold voltage variations. As a rule of thumb, increasing the overlap length between FP and AlGaN surface and reducing the FP insulator (e.g. Si_3N_4) thickness further helps in reducing the electric field peak. A common solution for high-voltage GaN devices is to design multiple stepped field plates (Figure 1.26) [25] in order to convert the single high peak at the gate into multiple smaller peaks, one at the edge of each step.

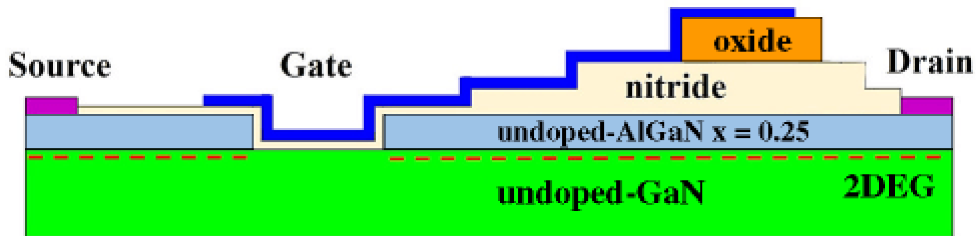
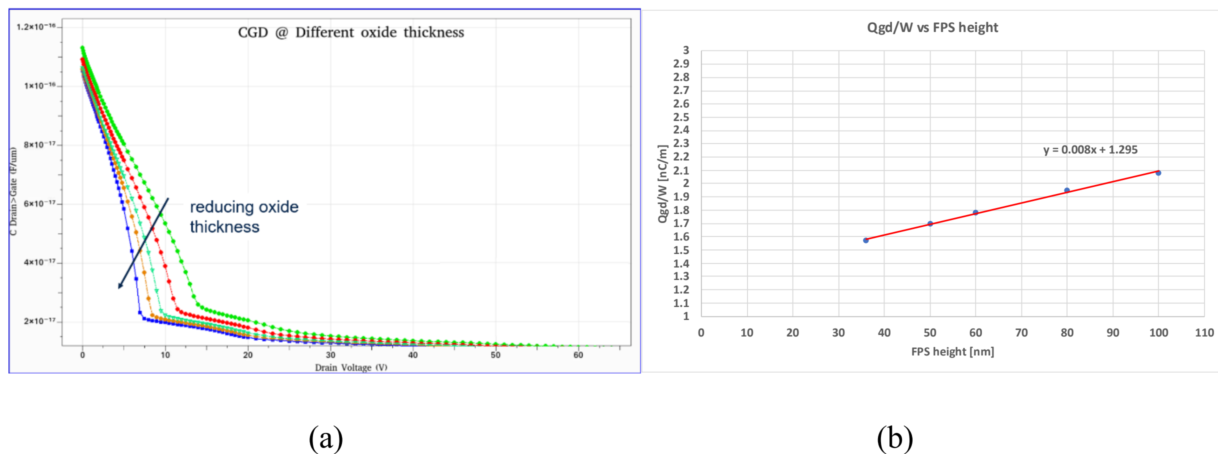


Figure 1.26: Schematic cross section of GaN HEMTs with multi-stepped field plates.

Field plate structures have also the effect of inducing a change in the depletion of the 2DEG when the drain voltage is increased. This depletion affects the shape and the value of output and reverse capacitance for GaN HEMTs; hence field plate design can be also optimized for improving capacitances. Figure 1.27 includes the TCAD simulations results on C_{RSS} (and extracted Q_{GD}) for different field plate distance from the AlGaN surface, performed on 100V structures calibrated on the DUTs of chapter 2: reducing the height of the field plate results in lower capacitance and gate-drain charge.



(a) (b)

Figure 1.27: (a) CRSS vs VDS and (b) QGD for GaN HEMTs with different thickness between source field plate and AlGaN surface (TCAD simulations performed on DUTs of chapter 2).

This example shows how TCAD simulations can be a powerful tool to analyze the effect of field plates on the electric field and on the capacitive contributions of GaN HEMTs.

1.3.3 Drain breakdown → Buffer improvement (AlGaN grading, carbon/iron doping, superlattice)

As mentioned at the beginning, one of the major advancements in the epitaxy growth of GaN was the introduction of the AlN nucleation layer at the interface with the substrate. Actually, the complete epitaxial stack from substrate up to actual AlGaN/GaN heterostructure is usually rather complex and it is known as “buffer” layer. For example, after the nucleation layer, other AlGaN transition layers with decreasing Al content (AlGaN grading) are generally grown (Figure 1.28): this allows to obtain a smoother change from the lattice constant of the substrate (Silicon, Al_2O_3, SiC, etc…) to the Gallium Nitride one. This allows reducing the mechanical stress, avoiding too large variations that would result in high defectiveness of the grown layer and poor performance. These layers are usually called “Strain-Relief Layers”, SRLs.

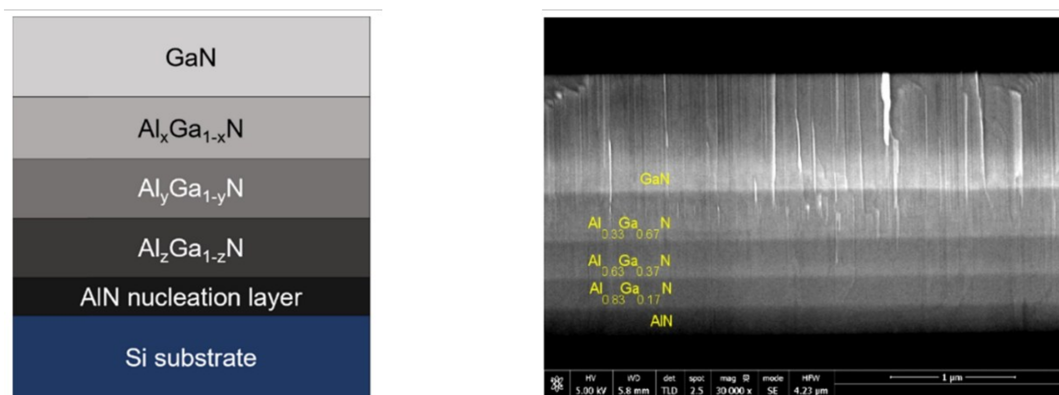


Figure 1.28: Example of GaN buffer structure including AlGaN step-grading [34].

Even after the introduction of SRLs, GaN HEMTs still suffer from high vertical conductivity due to threading dislocations (due to lattice mismatch with substrate), shown in Figure 1.29, and uncontrolled impurities (in fact, GaN is unintentionally n-type doped by MOCVD chamber elements like oxygen, nitrogen and silicon, which act as shallow donors and are known as background donors). This high leakage must be carefully limited also to avoid unwanted punch-through effects and early breakdown of the structure.

Figure 1.29: Microscopical image of threading dislocations inside the GaN buffer of high-voltage DUTs discussed in Chapter 4.

Different solutions have been proposed to reduce the vertical leakage of the GaN buffer, and they can be also combined in most cases to get an optimum effect. The most well-known approach is the intentional introduction of acceptor dopants in the buffer in order to compensate for the unintentional n-doping coming from excess carriers. This technique is effective in reducing buffer leakage by several orders of magnitude (making it semi-insulating), therefore limiting one of the causes of breakdown, ultimately leading to an increase of the breakdown voltage. Two dopants are generally adopted for acceptor doping of GaN buffers: the first one is iron [35] and it is more common in Radio-Frequency (RF) applications (thanks to relatively shallow acceptor level below conduction band leading to minimized dynamic Ron increase also at high frequency); the other one is carbon, which is primarily used in power switching applications, due to the deeper acceptor level above valence band resulting in superior leakage suppression and enhanced vertical breakdown [36]. However, the C-doping of the buffer must be carefully traded-off with dynamic on-resistance effects induced by hole emission from C-traps, that is one of the main issues affecting GaN HEMTs with respect to traditional Silicon MOSFETs. For this reason, C-doping must be confined to a deeper region of the GaN buffer while the GaN layer close to the AlGaN/GaN heterostructure (the GaN channel) must be undoped, as shown in Figure 1.30.

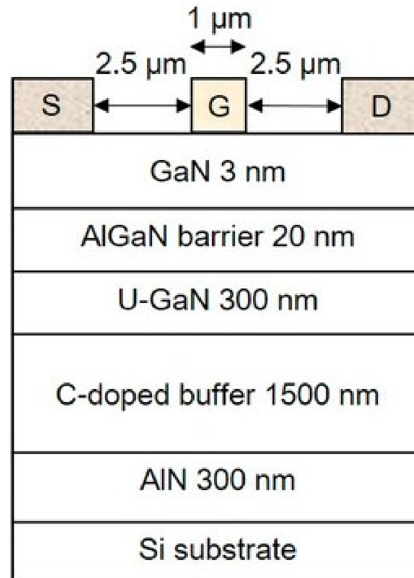


Figure 1.30: Schematic epitaxial GaN HEMT stack including C-doped buffer [37].

Another common technique for improving high voltage GaN epitaxies is the so-called superlattice structure [38]. In this case, an alternating repetition of thin layers (e.g., AlN/GaN or AlGaN/GaN) is grown in the buffer region (Figure 1.31) reducing the stress from substrate up to GaN. This results in a reduction of threading dislocations thus leading to enhanced reduction of vertical leakage and great breakdown voltage improvement. The disadvantage of this approach is the increase in complexity and in cost of the overall epitaxy.

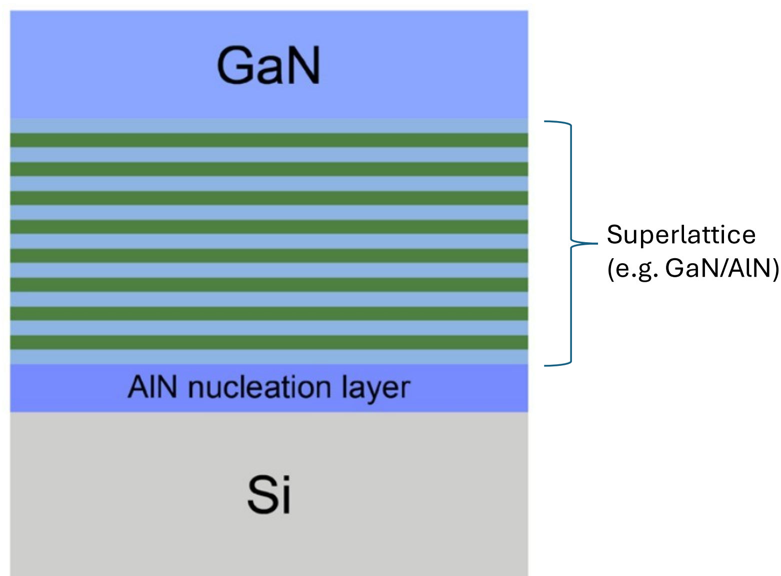


Figure 1.31: Epitaxial GaN buffer stack including superlattice [39].

Other know solutions to improve the buffer involve the introduction of AlGaN back-barriers, p-GaN buried layers and the use of SOI substrates.

1.4 Traps, dynamic effects and dynamic characterizations

1.4.1 Traps and dynamic effects

As anticipated in the previous sections, GaN devices usually suffer from dynamic current collapse phenomena, generally induced by trap states located either in the buffer or at the surface of the device (Figure 1.32), coming from impurities or defects.

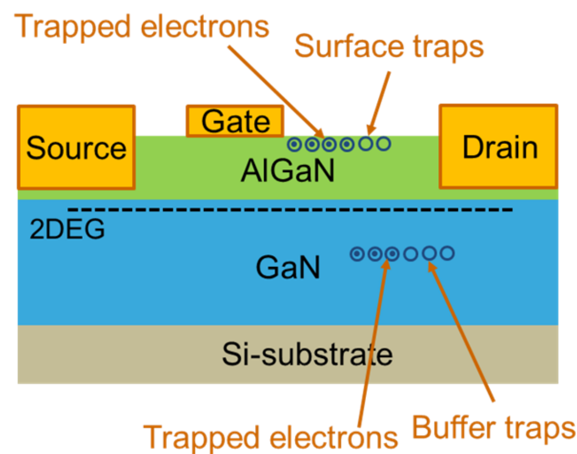
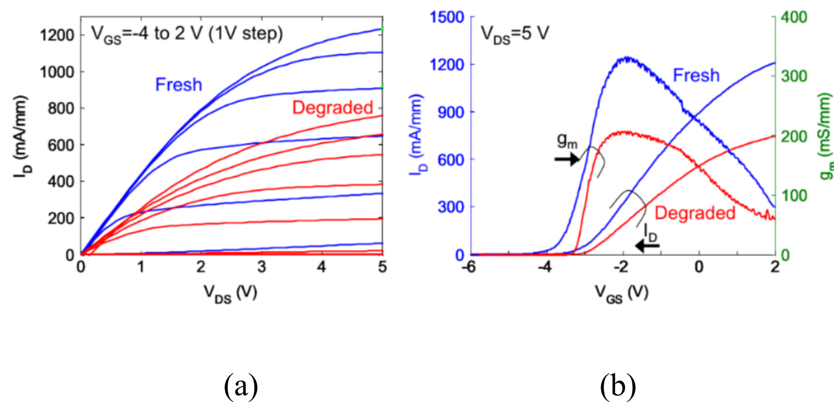


Figure 1.32: Cross section of a GaN HEMT including surface and buffer traps.

This effect consists of a dynamic worsening of the drain current (e.g., due to threshold voltage or R_{on} increase), after that a bias ("stress") is applied to the gate/drain, with respect to the "fresh" value before the applying of the stress: as an example, Figure 1.33 illustrates what happens to the drain current of a normally-on GaN HEMT after a V_{GS} step stress sequence from -10 V down to -50 V (1 V step every 1 min).



(a) (b)

Figure 1.33: Typical fresh and stress (a) output and (b) transfer characteristics of a GaN HEMT [40].

This is one of the strongest limitations of GaN-based devices and can significantly impact performance, making it difficult to reach the ideal ones. Moreover, it is also difficult to have a unique figure of merit for taking into account these dynamic effects, since they are highly dependent on the specific waveforms that are applied on the device. Nonetheless, many studies have been carried out in literature, and some key aspects are now very well clarified. For example, in the case of carbon doping of the buffer, the modelling of the dynamic current collapse is generally attributed to thermally activated hole emission process from C_N acceptor trap states at +0.9 eV above the valence band [41], as shown in Figure 1.34.

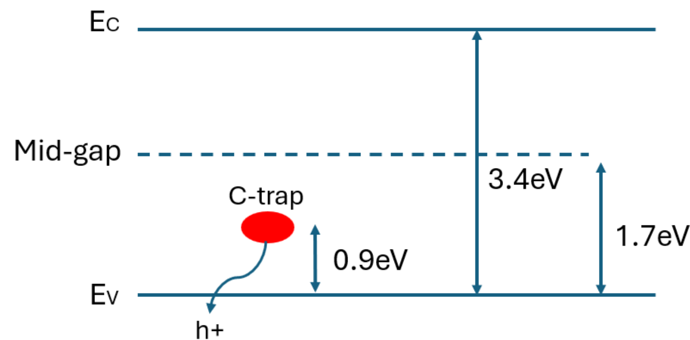


Figure 1.34: Band diagram of C-doped GaN buffer with hole emission from C-trap to valence band.

In particular, carbon doping is known to generate both deep acceptor traps (C_N substitutional) and shallow donor traps (C_{Ga} substitutional), in a ratio strongly dependent on growth conditions of the GaN. What is observed in GaN HEMTs with C-doped GaN buffers is that at large positive V_{DS} (or large negative V_{SUB}), current collapse phenomena slowly start to take place (stress phase). Then, when the bias is removed, the device slowly recovers to the initial state (recovery phase). Therefore, the application of the voltage must result in a negative charge build-up in the C-doped buffer (proportional to the applied voltage), as shown in Figure 1.35, that could be attributed either to electron capture or hole emission from the C-traps.

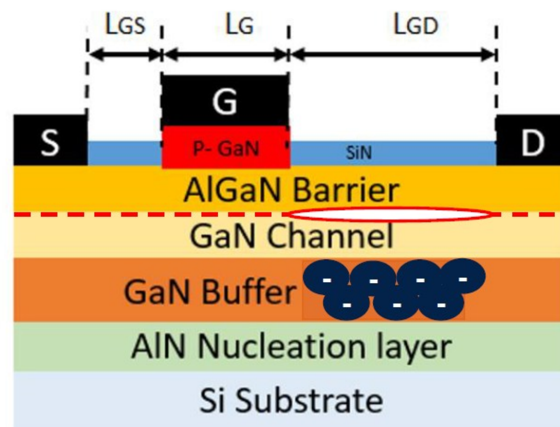
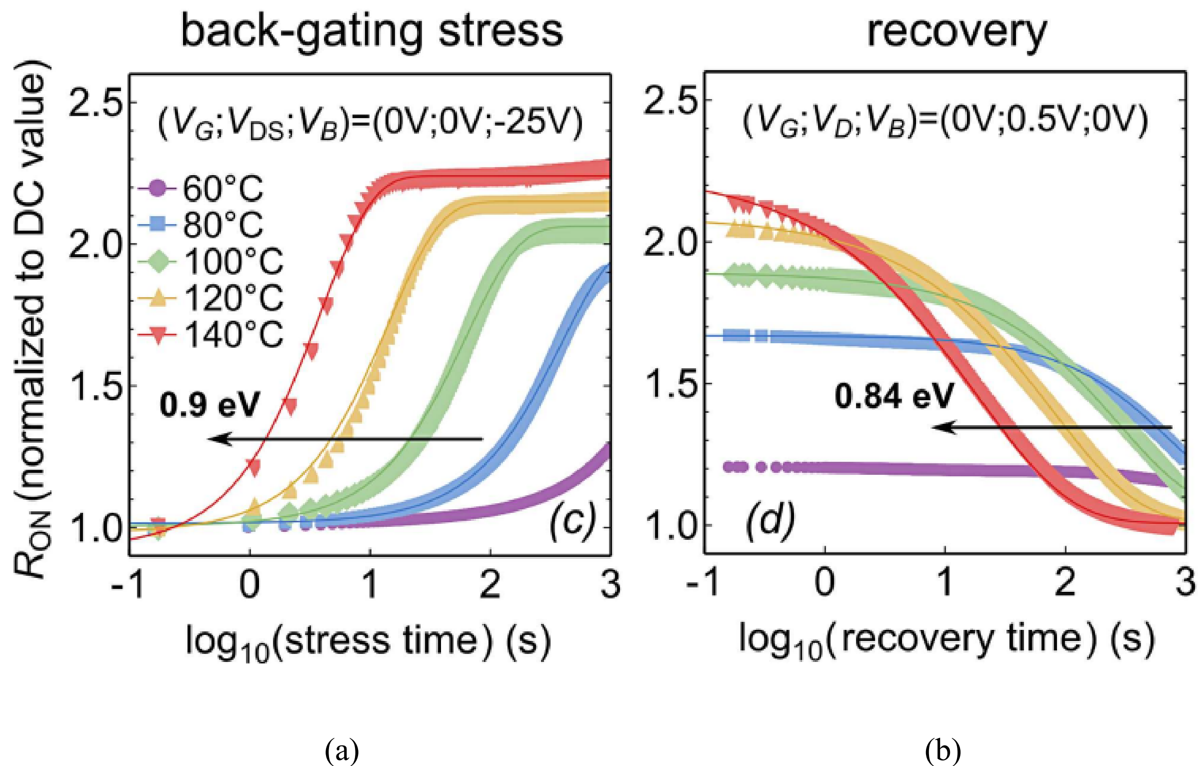


Figure 1.35: Schematic cross section of a GaN HEMT with C-induced 2DEG depletion.

However, since the dynamics of the stress phase at room temperature is rather slow (in the order of tens of seconds) and there is thermal activation, it can be concluded that hole emission is the right physical explanation. In fact, while electron capture would be an extremely fast and temperature-insensitive process, hole emission is governed by Arrhenius equation, which links the characteristic emission time from the trap to its energy level and to the temperature. This dependence can be used to extract the energy level and identify the trap:

$$\tau = \frac{1}{T^2} \cdot \exp\left(\frac{q \cdot E_A}{kT} + C\right) \tag{1.4}$$

When the stress is removed (switching to the on state), the current does not recover immediately because the negative charge built up in the buffer must be neutralized. To return to a neutral state, the negative C_N ions must re-capture a hole: this should be a fast phenomenon, but it is not what experimentally observed (an example is reported in Figure 1.36).



(a) (b)

Figure 1.36: R_{on} (a) degradation and (b) recovery phase of GaN HEMTs at different temperatures [42].

The reason behind this can be traced to the fact that in a standard GaN HEMT, there is no "hole source" (no p-type contact). The buffer must wait for holes to be thermally generated or for holes that were stored in the lower regions of the buffer to drift back and be re-captured. This lack of available holes makes the recovery phase exceptionally long, often lasting seconds or even minutes at room temperature. Of course, in GaN devices, there can be other trap states (e.g. due to Mg or Fe doping, surface states) and each of them require a dedicated analysis.

1.4.2 PIV (DCTs and OTF) and Dynamic Ron in p-GaN HEMTs

The most widely used technique for characterizing dynamic effects in GaN HEMTs is the use of pulsed IV characterizations. They are used both to measure the impact of dynamic stress on the main device parameters and to study the root cause of the dynamic effects, i.e. the nature of the traps. These measurements often involve two states for separately stressing and monitoring the device: first, a quiescent bias used to fill traps (longer than filling time constant); then a short pulse in the operative point (faster than de-trapping).

Depending on the quiescent bias applied, the effect of the applied stress from one or more terminals can be evaluated on the device. In order to monitor traps dynamics, two main pulsed characterizations can be exploited: Drain Current Transients (DCTs) and On-The-Fly (OTF) Characterizations. DCTs are used when the dynamic related to emission from traps happens in on state (e.g., Fe-doped GaN buffer) and they measure the so-called gate/drain lag. The gate/drain lag denotes the slow transient response of the drain current when the gate/drain voltage is pulsed, as shown in Figure 1.37. In particular, from what was discussed before, buffer traps are mainly responsible for drain lag while surface trap states mainly affect gate lag. Of course, both gate and drain lags can be detrimental for device performance since the device switches between on state and off state (both gate and drain are pulsed during application).

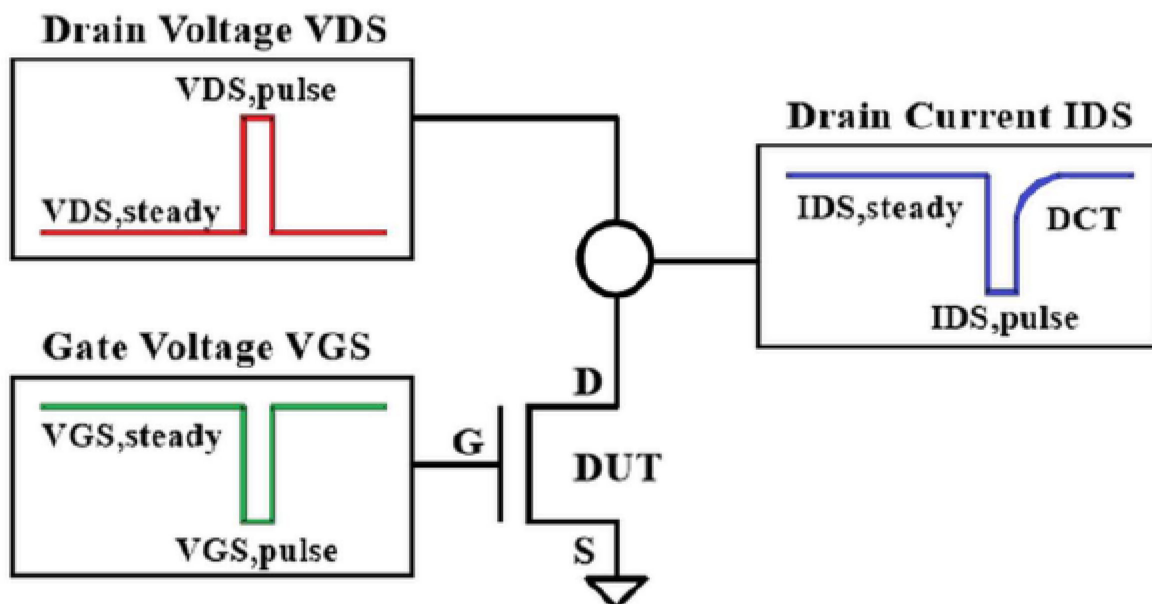


Figure 1.37: Schematic of the waveforms applied and measured for evaluating DCTs.

Gate/drain lag is a way of characterizing the traps responsible for the corresponding current transient. Of course, the typical pulse length must be larger than the trapping duration (which is quite fast) while the charge release from a trap is an emission process that requires more time (up to few seconds). Therefore, after performing DCTs at different temperatures, Arrhenius plots can be used to get the activation energy (E_A) and recognize trap's signature. An example of this procedure is reported in Figure 1.38.

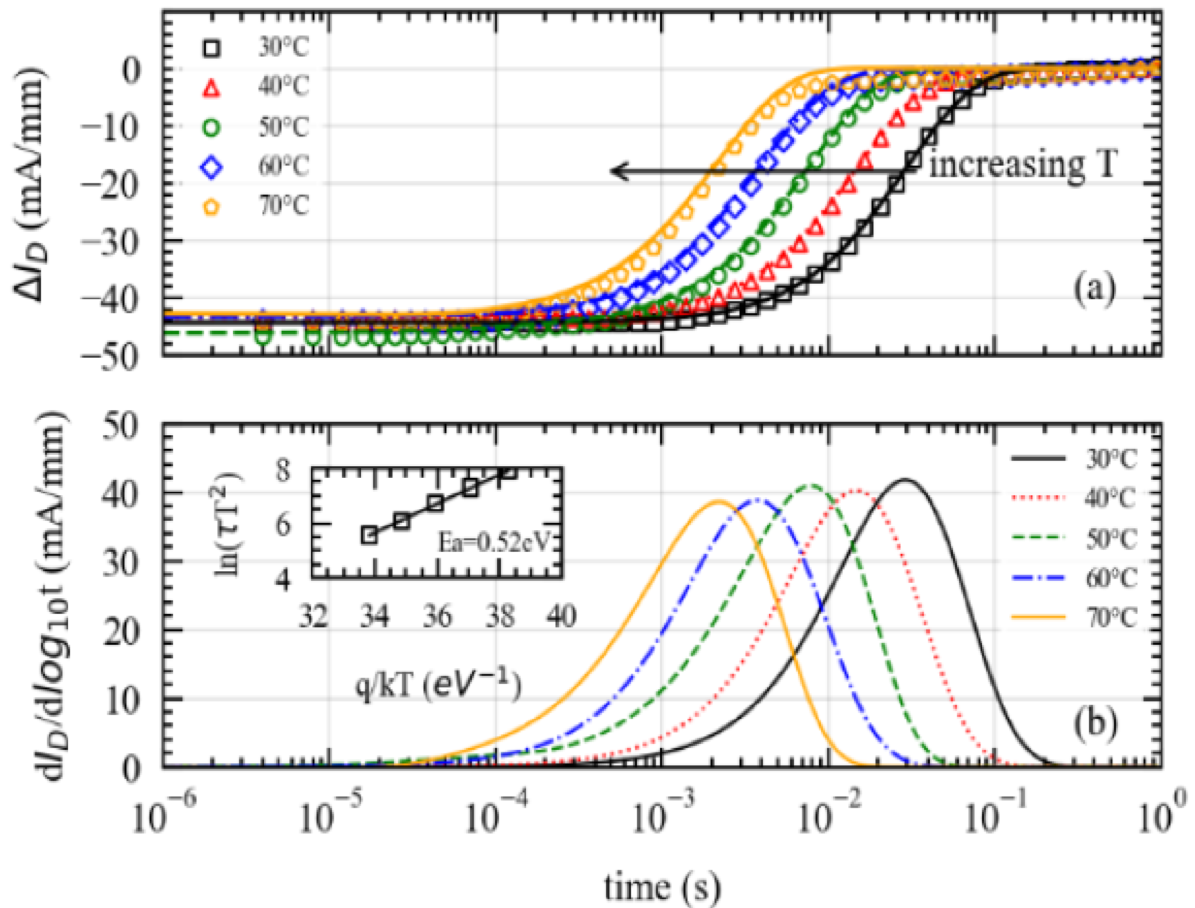


Figure 1.38: Temperature evaluation of DCTs with extraction of characteristic trap emission time and estimation of the activation energy [43].

OTF characterizations are instead used when the dynamic related to emission from traps happens during off state (e.g., C-doped GaN buffer). In this case, the idea is to continuously switch the DUT between the off state (stress) and the on state (measure) condition, as in Figure 1.39, with a switching period that allows to get e.g., R_{on} values over several time decades (similarly to what happens in a switching converter). This technique has also the advantage of providing information about the dynamic evolution of the parameter of interest during the stress period, by cumulating the effect of the stress.

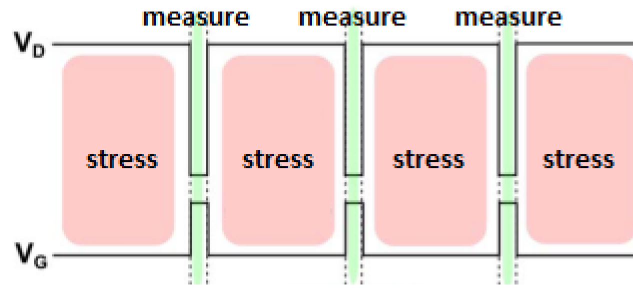


Figure 1.39: OTF sequence alternating off and on state.

This allows to gain physics insight in the mechanism responsibile for R_{on} degradation, since it allows to capture the dynamics of the trap states involved in the process. In fact, similarly to what discussed before about DCTs, also in this case, OTFs can be performed at different temperatures and by data fitting and calcutation, the activation energy of the trap can be identified (as shown in Figure 1.40).

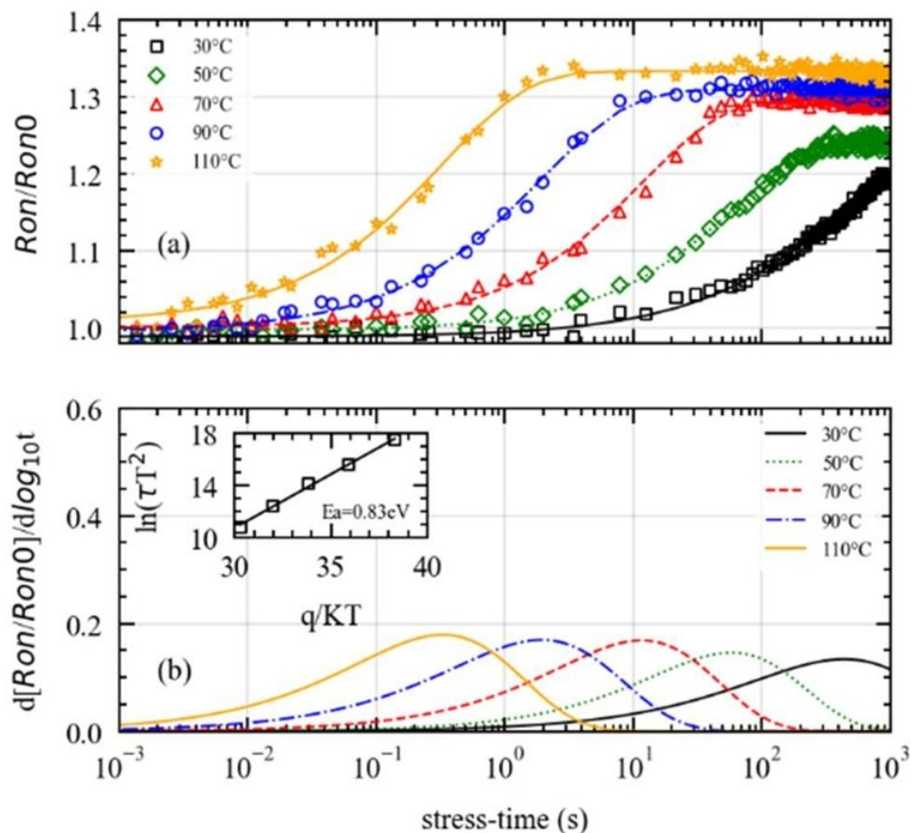


Figure 1.40: Temperature evaluation of OTF PIVs with extraction of characteristic trap emission time and estimation of the activation energy [44].

Therefore, OTF characterizations are a powerfool tool to investigate the dynamics of the most significant device parameters. In particular, R_{on} is the most important figure of merit for

switching power applications and it is interesting to study the most common trends of dynamic R_{on} in C-doped GaN HEMTs. In the case of high-voltage (e.g., 650 V) GaN HEMTs, dynamic R_{on} is generally characterized by a bell shape dependence on the V_{DS} stress (Figure 1.41). Ideally, the larger the stress, the higher the dynamic Ron, and in fact this is what happens up to a certain voltage. Then, at higher voltage, avalanche mechanisms start to become relevant: this favors the generation of free holes that can be used to compensate for the ionized C_N traps thus reducing the dynamic R_{on}.

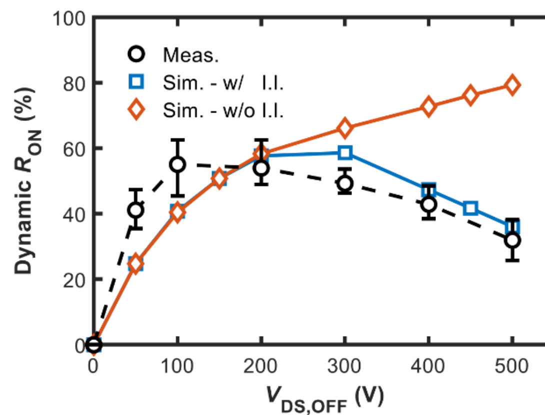


Figure 1.41: Typical dynamic R_{on} bell-behavior versus drain voltage, with partial recovery at high drain bias due to holes generation [45].

Given this phenomenon, a well-known method to improve the dynamic R_{on} even more is to include a hole supply in the structure, e.g. by connecting an additional p-GaN region to the drain [46], as shown in Figure 1.42.

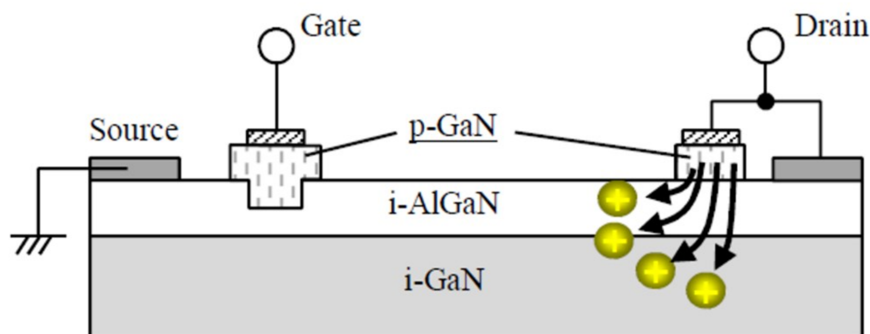


Figure 1.42: Schematic structure of a GaN HEMT with additional p-GaN connected to drain, for increase hole injection at high drain bias [47].

This solution allows a great improvement of the dynamic R_{on} at higher voltages (Figure 1.43) and in more stressful conditions like hard switching, where holes injection from the drain-connected p-GaN can compensate for additional hot electrons trapping phenomena.

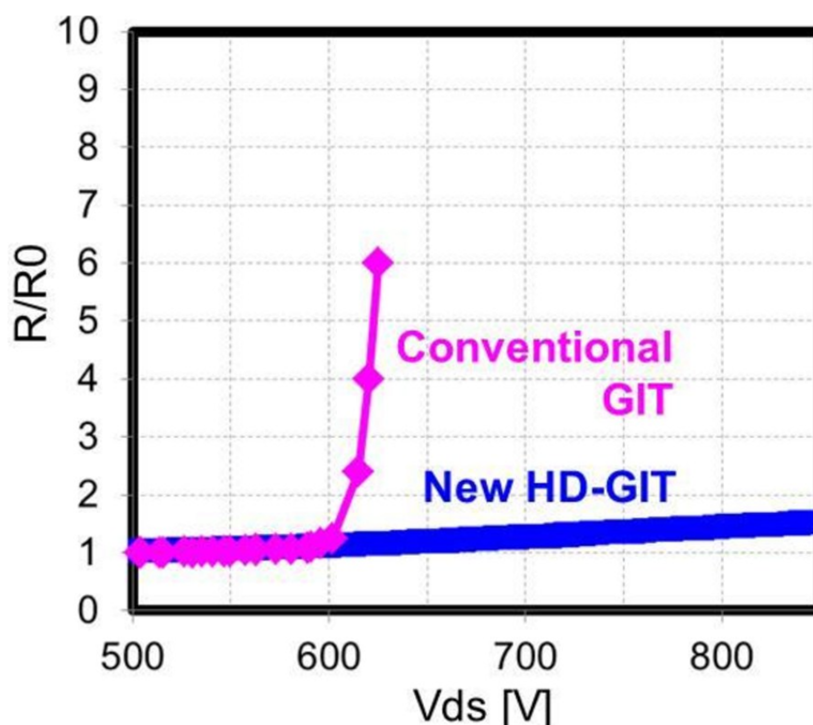


Figure 1.43: High voltage dynamic Ron comparison between a conventional GaN GIT HEMT and the solution with additional p-GaN connected to drain ("New HD-GIT") [47].

In all the previous cases, the most common dynamic R_{on} behavior was presented. Of course, other type of stresses can influence the current collapse in different ways, for example it could be worth to investigate the effects of substrate stress on the dynamic R_{on} and combine this with the drain stress, already shown: this is particularly useful to study and estimate the R_{on} degradation of monolithic high-side devices used in half-bridge configurations, where the DUT is subjected to high V_{DS} and high V_{SB} (lateral and vertical stress).

1.5 Outline

After the previous overview of GaN technology, the contents discussed in detail in the next chapters are briefly listed and summarized below:

Chapter 2 presents a study on the Mg role in the optimization of normally-off p-GaN HEMTs with the aid of TCAD simulations and experimental results.

Chapter 3 investigates the high-temperature performance degradation of p-GaN devices and some process improvements that can be made to limit the drift.

Chapter 4 discusses the drain and gate preliminary reliability by means of TCAD simulations aimed at the understanding of the observed phenomena and at the DUT robustness improvement.

Chapter 5 treats the DC/AC characterization of bidirectional p-GaN HEMTs in all their different operating modes, comparing the results with TCAD simulations and with unidirectional data.

Finally, Chapter 6 draws the conclusions of this work highlighting the main achievements, stressing the importance of an approach involving both simulations and experimental characterizations.

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2 Effect of Mg activation on pinch-off voltage

As mentioned in the introduction, the presence of the two-dimensional electron gas (2DEG) at the heterointerface between AlGaN and GaN makes these transistors intrinsically normally-on devices while, for power electronic applications, a normally-off operation is usually preferred for safety reasons and compatibility with CMOS circuitry (e.g., gate drivers). As previously discussed, one of the most-promising solutions for obtaining the enhancement operation is the introduction of a p-doped GaN layer. Even if many elements have been explored as alternatives for obtaining a p-doping, the preferred material (commercially-used) for GaN is still magnesium, given the fact that it is characterized by low activation energy [1]. Nonetheless, several solutions can be adopted for the electrical activation of magnesium in GaN both in terms of the temperature/pressure of the Rapid Thermal Annealing (RTP) process and the ambient gases (oxygen/nitrogen) ratio [1].

Regardless, the introduction of this p-GaN layer allows us to deplete the 2DEG below the p-GaN region when the gate voltage is at a zero bias and to restore the 2DEG channel when applying a sufficiently high overdrive voltage. Given the importance of this extra p-GaN layer, the correct and detailed understanding of its impact on the device behavior is crucial in the development and optimization of GaN HEMTs. In this chapter, Technology Computer-Aided Design (TCAD) simulations (run through the 2-D device simulator ATLAS (by Silvaco Group, Inc., Santa Clara, CA, USA [2]) and electrical measurements are presented, with the objective of interpreting the impact of magnesium-induced p-doping on the electrical behavior of the device.

2.1 Devices under test

The analysis reported in this chapter was carried out on wafers fabricated by STMicroelectronics. Figure 2.1 shows a schematic cross section of the p-GaN gate HEMTs investigated in this study (device under test, DUT, characterized by a gate width (W) of 0.4 mm).

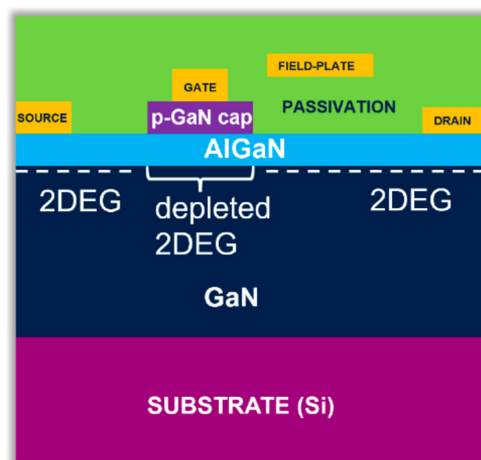


Figure 2.1: Schematic cross section of the p-GaN DUTs.

In particular, the devices analyzed in this chapter are p-GaN/AlGaN/GaN HEMTs grown on a Silicon(111) p-type substrate via metal–organic chemical vapor deposition (MOCVD).

The epitaxial stack consisted of a nucleation layer, an insulating GaN buffer suited to 100 V applications, followed by an AlGaN barrier layer (18 nm thick) with a 20% aluminum concentration. Both ohmic and gate contacts were formed via Ti/Al-based metallization defined by means of a liftoff process [3].

The main difference between depletion-mode (normally-on) and enhancement-mode (normally-off) HEMTs is represented by the threshold voltage (V_{TH}) of the device, since, in the former case, the V_{TH} is negative (therefore a negative voltage is required to turn off the device), while in the latter case, the threshold is positive (such that a positive gate voltage is necessary to switch on the transistor). Apart from V_{TH}, another parameter can be defined, considering the sub-threshold shape of the linear transfer characteristics, namely the pinch-off voltage (V_{PO}). The chosen definition of the pinch-off voltage is related to the voltage at which the detected drain current starts to rise with an exponential behavior with respect to V_{GS}, as reported in Figure 2.2.

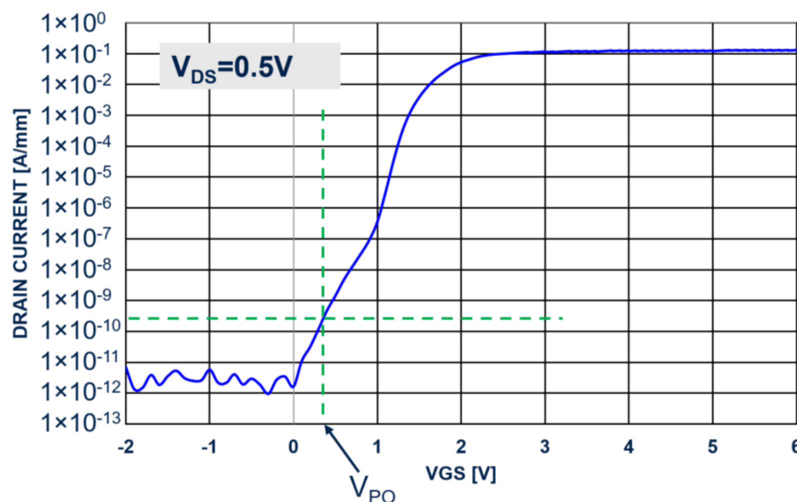


Figure 2.2: Typical linear transfer characteristic (semi-log scale) of a p-GaN HEMT highlighting the pinch-off voltage.

The introduction of this parameter can be very useful in order to better evaluate the effective interruption of the current when turning off the device. Indeed, higher V_{PO} values correspond to a reduced sub-threshold leakage at low gate bias, as shown in Figure 2.3:

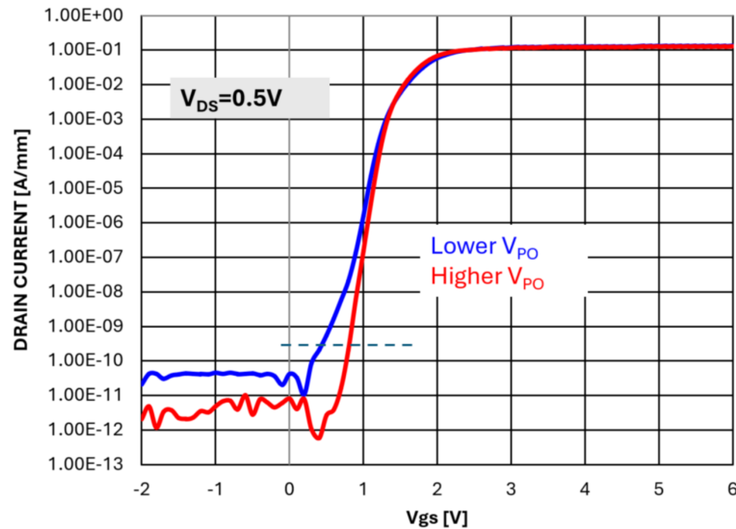


Figure 2.3: Comparison between linear transfer characteristic (semi-log scale) of p-GaN HEMTs characterized by different pinch-off voltages.

This feature can reflect also in reduced drain leakage at high drain voltages (e.g., at 100 V), given the increased margin to the drain-induced barrier lowering (DIBL) effect (leftward shift of the I_D-V_G due to high drain bias). Of course, V_{TH} will always be positively shifted with respect to V_{PO}, depending on the subthreshold slope (SS) of the device.

Therefore, to obtain a robust normally-off device and improve the overall performance, V_{PO} is an important parameter to be monitored. In p-GaN HEMTs, both V_{PO} and V_{TH} are mainly influenced by three actors [4]: (1) aluminum content (Al%) of the AlGaN barrier; (2) AlGaN barrier layer thickness; (3) magnesium doping. The first two parameters are very well known in the literature [5,6] and they have been described in the introduction. They show a very clear impact on the device: an increase in the Al% of the AlGaN barrier produces a more pronounced spontaneous and piezoelectric polarization effect, leading to a higher 2DEG density which in turn is reflected in a reduced V_{PO}; an increase in the AlGaN barrier thickness has essentially the same effect of a higher aluminum concentration, thus resulting in a decrease in V_{PO}. Mg doping acts instead on the device in a more complex way, and it has been investigated in detail via TCAD simulations and experimental Capacitance–Voltage (CV) measurements, which are reported in the following.

2.2 TCAD simulations of p-GaN effect

As a first step, the structure of a typical p-GaN HEMT has been reproduced via the ATHENA simulator (by Silvaco) [7]; then, the 2-D ATLAS device simulator has been used to implement the physical models for the device modelling. In particular, the Poisson's equation and continuity equations for electrons and holes were included, and a drift-diffusion model was used to solve the transport equations. The electron saturation velocity and mobility model according to Farahmand's theory [8] were implemented as well. The spontaneous and piezoelectric polarization were instead modelled as fixed sheet charges at the interface of AlGaN/GaN and p-

GaN/AlGaN. Then, properties of the p-GaN region were properly set for obtaining a correct modelling of the threshold, off-state and on-state parameters. In particular, a gate workfunction was set in order to get a Schottky barrier of about 1.0 eV (based on the analysis performed in chapter 5 of [9]). Moreover, surface recombination together with hole tunnelling was enabled at the gate contact in order to model thermionic field emission (TFE) conduction. TFE is an intermediate conduction model between pure thermionic emission (TE), where carriers must gain enough thermal energy to jump over the potential barrier and so there is a high temperature dependence, and pure field emission (TE), where carriers can tunnel through a thin barrier in the case of sufficiently high electric field [14,15]. The AlGaN barrier was instead modelled as a leaky dielectric by specifying a donor trap density and calibrating the capture cross section accounting for the trap-assisted tunneling induced by e.g. carbon impurities or oxygen vacancies.

After setting all the main device parameters, two Design of Experiments (DoEs) regarding the Mg concentration have been evaluated. Simulations were run by defining the substitutional portion of the nominal Mg concentration (i.e., the one accounting for p-type conductivity), as an acceptor dopant in GaN with an activation energy of about 170 meV [9,10]. Therefore, incomplete ionization model was also included in the simulation.

Then, for each DoE, a simulation of the linear I_D-V_G of the device has been carried out in order to understand the results in terms of V_{PO}. Both V_{PO} (pinch-off voltage) and V_{TH} (threshold voltage) have been extracted from simulations and experimental measurements. In particular, the V_{PO} has been extracted with constant current method (i.e. as the voltage at which the drain current reaches 2.5×10^{-10} A/mm), while the V_{TH} has been defined by the extrapolation in the linear region (ELR) method [11]. In the following, the two TCAD DoEs are detailed showing the main findings:

a) In the first DoE, the HEMT structure has been simulated with different levels of Mg concentration. All the Mg profiles were ideal and confined only along the p-GaN thickness (no Mg out-diffusion in the AlGaN barrier), as shown in Figure 2.4.

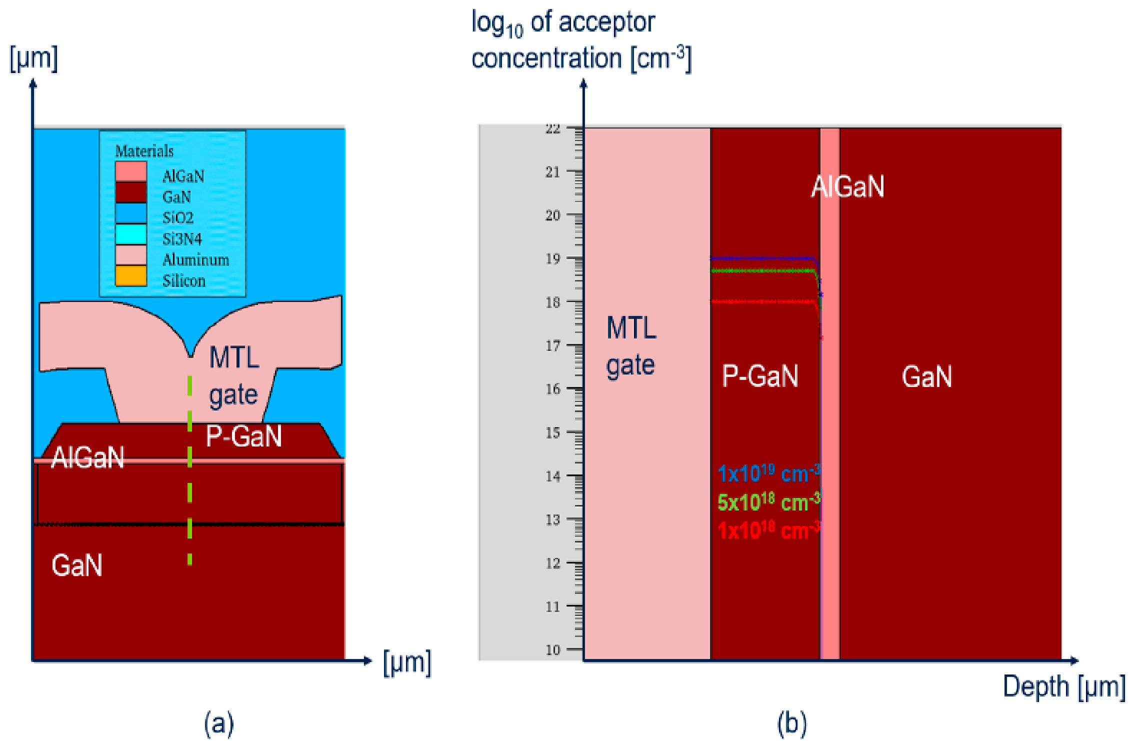


Figure 2.4: (a) TCAD simulated p-GaN module (b) Cutline of the different acceptor doping profiles implemented in the simulation.

The simulation results are summarized and shown in Figure 2.5, where it can be observed that no differences in terms of V_{PO} have been obtained with the levels of Mg equal or above 10^{18} cm−3, while the pinch-off voltage becomes lower in the case of no acceptor concentration in the GaN cap. The explanation of this trend can be found in the band diagrams of the gate stack (reported in Figure 2.4): as long as the acceptor concentration in p-GaN is high enough to induce a depletion region whose width is shorter than the whole p-GaN thickness (about 100 nm), no variations are produced at the conduction band (CB) edge close to the AlGaN/GaN heterointerface (meaning that the potential well, and so the 2DEG density, is not altered). Then, when the acceptor concentration is very low (or absent at all), the extension of the depletion width reaches the total p-GaN thickness, thus inducing a pull-down of the conduction band edge, reaching the quasi-Fermi level (EF). As a consequence, 2DEG density is increased and an early turn-on of the device (in terms of a reduced V_{PO}) is induced.

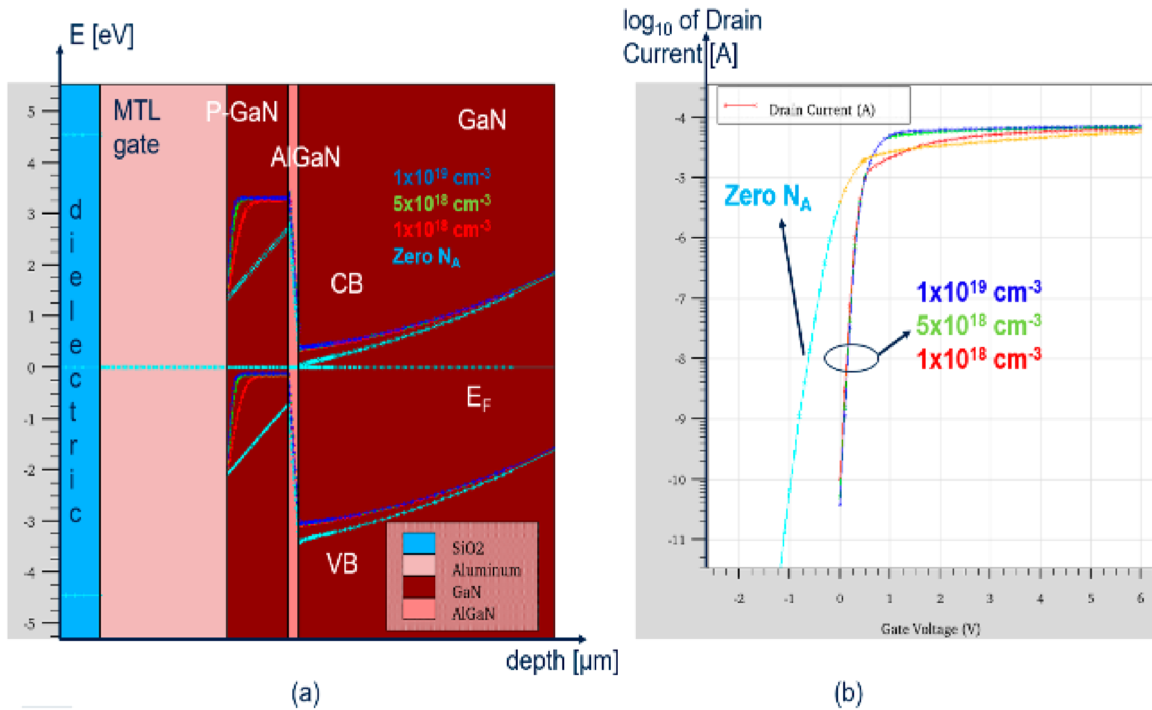


Figure 2.5: (a) TCAD simulated energy band diagrams (b) simulation of the linear transfer curves (VDS = 0.5 V) for the different doping levels.

b) A second DoE has been performed by fixing the value of the acceptor concentration level in p-GaN and varying the out-diffusion profiles in the AlGaN/GaN region: the different profiles have been simulated starting from an experimental out-diffusion shape (Figure 2.6 (a), red line) and then simply shifting the profile "tail" deeper into the AlGaN/GaN region. The Mg out-diffusion is something expected from real Mg profiles in p-GaN and it can be influenced by growth conditions and activation processes.

The results of the simulations are shown in Figure 2.6, where it is clearly visible how the out-diffusion influences both the pinch-off and threshold voltage. This is because the out-diffused acceptor concentration further depletes the 2DEG, making it more difficult to restore it with V_{GS}, thus increasing V_{PO} (this effect has been also reported in the literature [5,12]).

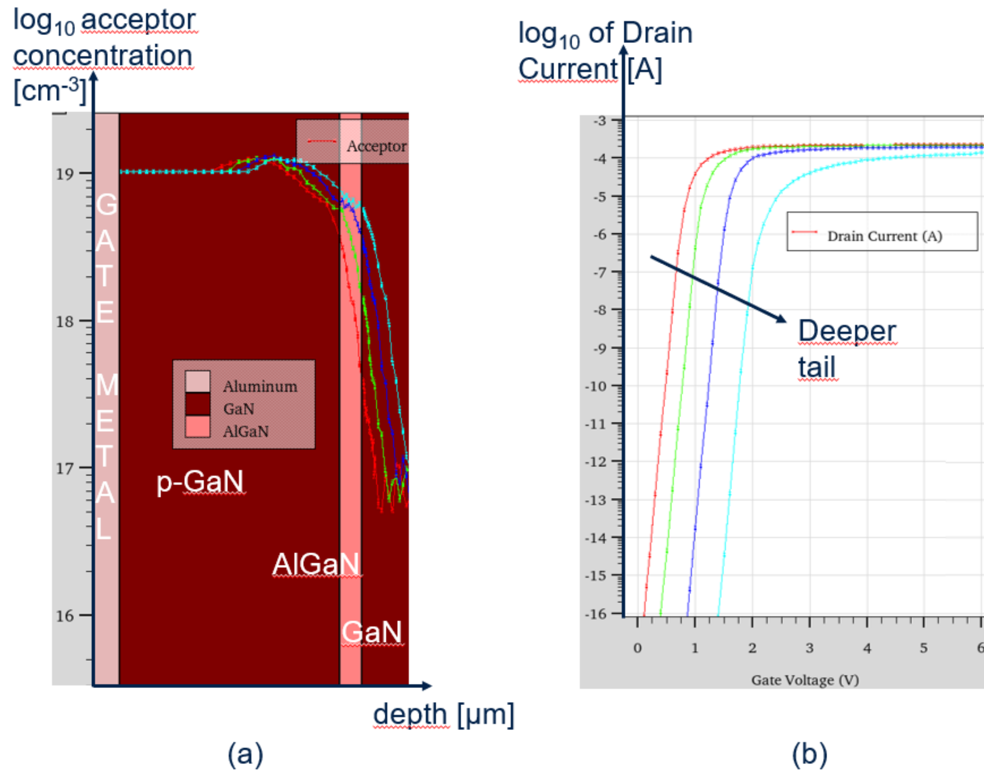


Figure 2.6: (a) Different acceptor out-diffusion profiles along the p-GaN region implemented in the TCAD (b) simulation of the corrisponding transfer curves (VDS = 0.5 V).

2.3 Gate capacitance measurements and interpretation

The experimental measurement of gate capacitance can be very useful for the analysis of the device behavior since it easily allows us to extract some information regarding the net acceptor concentration in p-GaN layers [13]. Another possible method consists of analyzing the gate leakage current but, in this latter case, it is harder to estimate the acceptor concentration. In fact, if the overall gate leakage current is not dominated by a bulk conduction in p-GaN and if the gate current model has not been clearly identified as, e.g., a thermionic (or a thermionic-field) emission [14,15], there is more margin for poor estimation. Instead, the measured gate capacitance curve can be effectively analyzed using the same model, regardless of the gate current conduction mechanism (of course, the only assumption is to have reduced gate leakage, which is the case for good Schottky interfaces). Therefore, it is not only easier but also more reliable to obtain information on the p-GaN acceptor concentration from CV rather than from the gate current measurements. The metal/p-GaN/AlGaN/GaN stack can be modelled as two diodes connected in anti-series: a first Schottky junction for the metal/pGaN region and a p-i-n diode for the p-GaN/AlGaN/2DEG region (Figure 2.7).

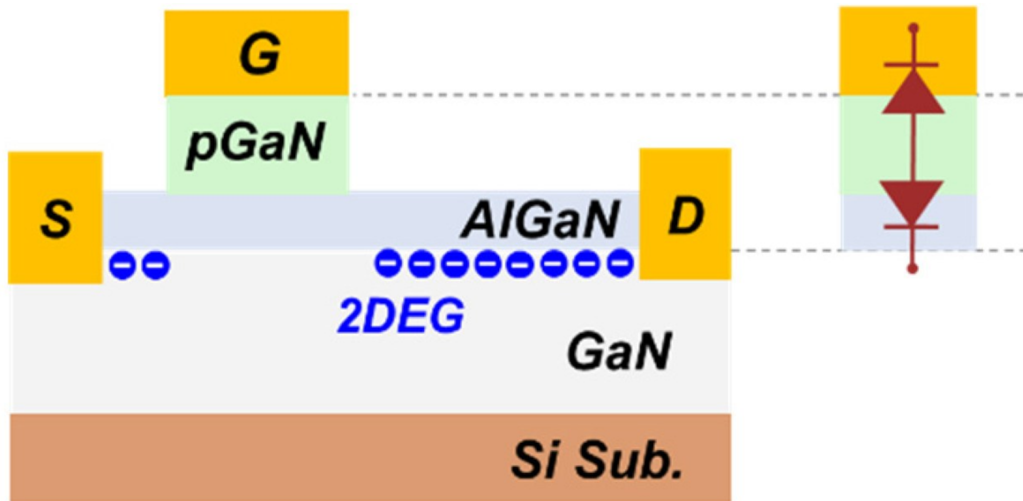


Figure 2.7: GaN HEMT gate stack (metal/p-GaN/AlGaN/GaN) circuit model in the case of Schottky contact between gate metal and p-GaN [16].

Each diode is characterized by a specific capacitance, contributing to the total capacitance of the overall gate stack [17]. In particular, when the 2DEG channel under the p-GaN is restored (i.e., in the super-threshold region), the total gate capacitance ($C_{G,tot}$) consists of the series of the AlGaN p-i-n diode capacitance (C_{AlGaN}), which can be assumed constant with V_{GS}, and the Schottky junction capacitance (C_{junc} or C_j), which is decreasing with V_{GS} (because of the increase of the depletion region). Figure 2.8 shows the gate stack modelling based on these two capacitances, highlighting the typical experimental gate CV curves.

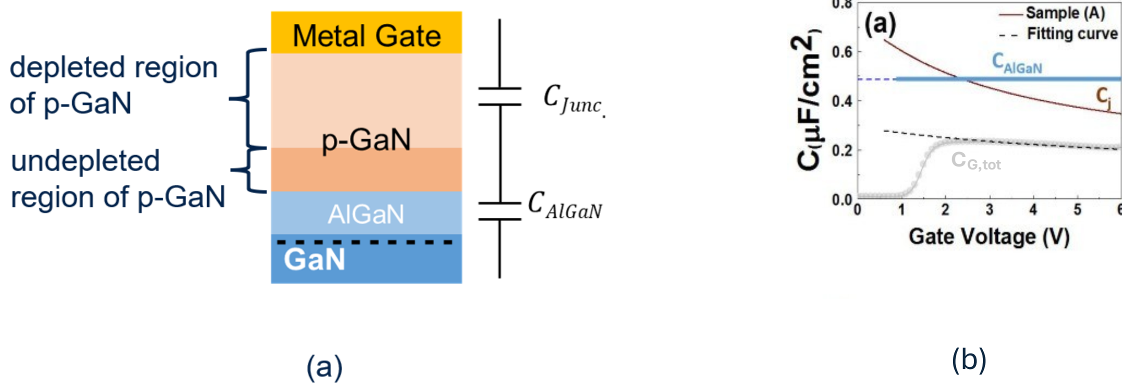


Figure 2.8: (a) Capacitance model of the p-GaN gate stack (b) typical gate capacitive contributions and overall gate capacitance [20].

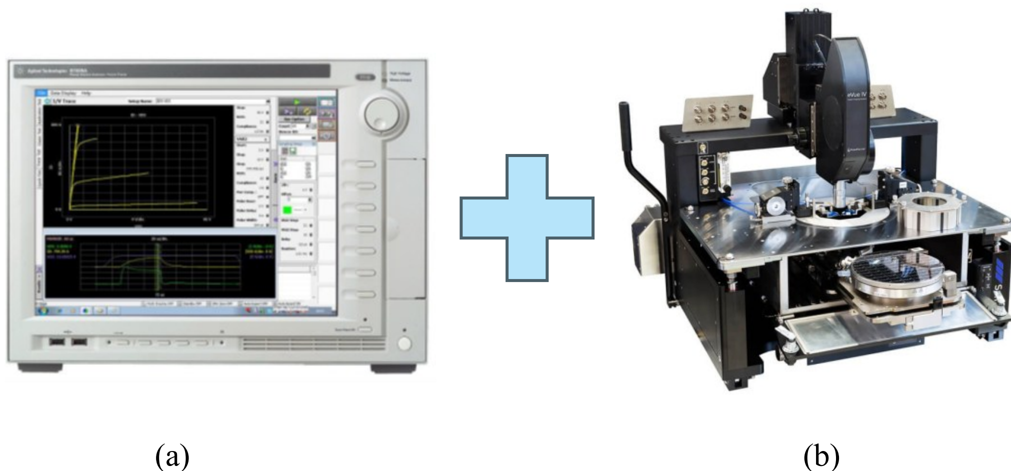
Focusing on the Schottky junction capacitance, the expanded expression reveals the dependence on the net acceptor concentration (the larger the N_A, the larger the C_j):

$$C_j = \sqrt{\frac{q \cdot \epsilon_{GaN} \cdot N_A}{2(V_{bi} + V_j)}} \tag{2.1}$$

Moreover, by rearranging the equation, it can be found that the net acceptor concentration is linked to the gate capacitance measurements by the following relationship, which is rather useful for estimation N_A from experimental gate capacitance measurements:

$$N_A \approx \frac{2}{q \cdot \epsilon_{GaN} \frac{\partial}{\partial V_{GS}} \left(\frac{1}{C_j}\right)^2} \tag{2.2}$$

Therefore, it can be concluded the acceptor concentration is the main technological parameter modulating the gate capacitance and, if it is lowered, the gate capacitance decreases as well. In particular, under the hypothesis of very low (or absent) active Mg in p-GaN (meaning very low or zero acceptor concentrations), the measured capacitance value would be low and constant with the gate voltage, thus showing to a dielectric-like behavior. In this chapter, all the shown CV measurements have been performed at wafer level through a B1505A interface with a probe system (Figure 2.9). The measurement frequency was 1 MHz with an AC signal of about 50 mV.



(a) (b)

Figure 2.9: (a) B1505A parameter analyzer and (b) 200 mm Cascade Summit probe system.

2.4 Experimental results

2.4.1 GaN cap process splits

Three different processes with different p-GaN cap have been implemented and compared for

better understanding the role of Mg doping and its activation as an acceptor:

a. undoped GaN cap process (reference), where no intentional magnesium doping has been introduced in the GaN cap.

b. single-RTP process, characterized by an intentional Mg doping (of about 1×10^{19} cm^{-3}) during the epitaxial growth of the GaN cap and a standard Rapid Thermal Processing (RTP) for Mg activation (temperature in the range of 700–850 °C for a time duration of 1–10 min), performed after the p-GaN growth.

c. multiple-RTP process, featuring intentional Mg doping (of about 1×10^{19} cm^{-3}) during the epitaxial growth of the GaN cap and an improved RTP steps for Mg activation (same conditions as in the single-RTP process, but the activation process is performed several times during the device process flow).

Differences in terms of device behavior between the undoped GaN cap and the p-doped ones have been detailed in the next section. Combining the TCAD simulations results already presented and some chemical analyses on the samples, a deeper understanding of the observed data is provided. Then, the effects of the improved activation process for the p-GaN (namely, the multiple-RTP process) are presented and thoroughly analyzed.

2.4.2 Comparison between unintentionally-doped and p-doped GaN Cap Layer

Reference process and single-RTP process devices have been characterized through DC and AC measurements. In particular, linear transfer characteristics and gate capacitance measurements showed that devices with an undoped GaN cap are characterized by negative V_{PO}/V_{TH} (normally-on behavior) and flat C/V curves, as reported in Figure 2.10. On the other hand, single-RTP process devices behave as normally-off HEMTs, showing a higher V_{PO} (positive but close to zero) and V_{TH} (Figure 2.9). However, the measured CV curve of the single-RTP process exhibits the same behavior already observed in the reference process, meaning that also in this case the gate capacitance is constant versus V_{GS} (Figure 2.9).

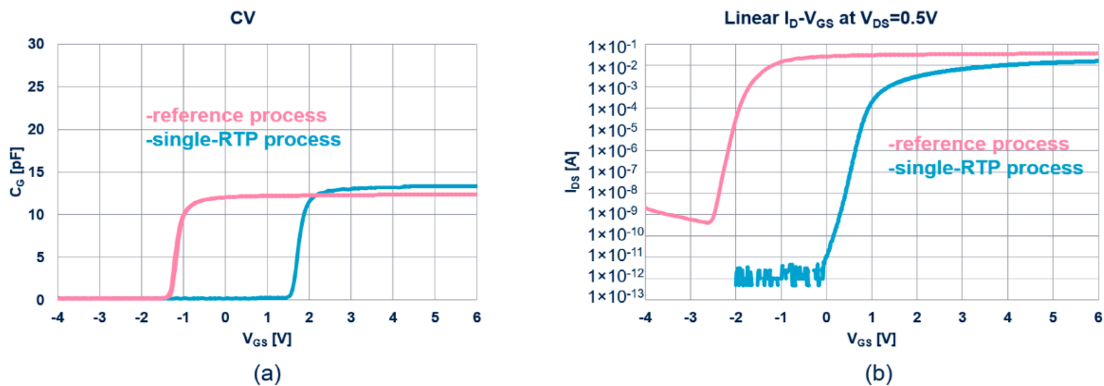


Figure 2.10: (a) Gate capacitance and (b) linear IV comparison between reference and single-RTP process.

Moreover, the gate leakage measurements have shown very similar values between the reference process and the single-RTP process, as shown in Figure 2.11.

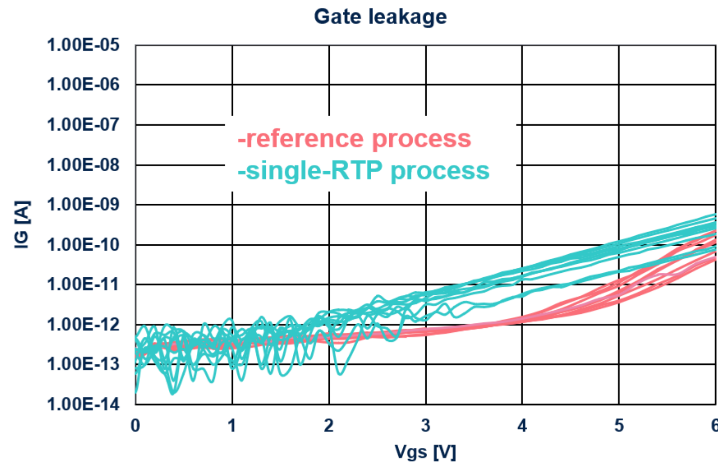


Figure 2.11: Gate leakage comparison between reference and single-RTP process.

As discussed in the previous section, a flat gate capacitance (dielectric-like behavior) can be an indication of a fully depleted GaN cap layer. This condition can be present in the case of zero or very low active Mg concentration in p-GaN ($<5 \times 10^{17}$ cm^{-3}). Therefore, it is not strange to obtain a flat CV curve for the undoped GaN process (where there is no intentional Mg doping) but this behavior is less expected in the case of single-RTP process. Moreover, it must be highlighted that even if the gate capacitance is flat on both processes, pinch-off values are quite different. In order to investigate these unclear results observed in single-RTP process devices, Secondary-Ion Mass Spectrometry (SIMS) analyses have been performed on dedicated structures with large-size p-GaN. In fact, through SIMS inspection, it is possible to obtain information about the position and the concentration of the chemical species inside the probed structure. Figure 2.12 displays the results of the SIMS analysis performed on single-RTP process devices with specific focus on the profiling of Mg, H, Ga, Al concentrations along the p-GaN layer and the AlGaN/GaN region. Hydrogen species are expected to be present (and in fact they were detected), due to some contamination coming from the precursors used in the reaction chamber for the p-GaN growth.

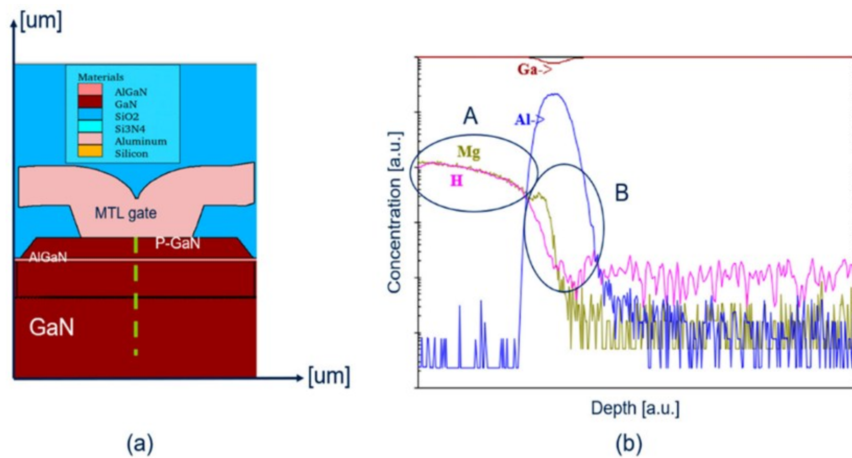


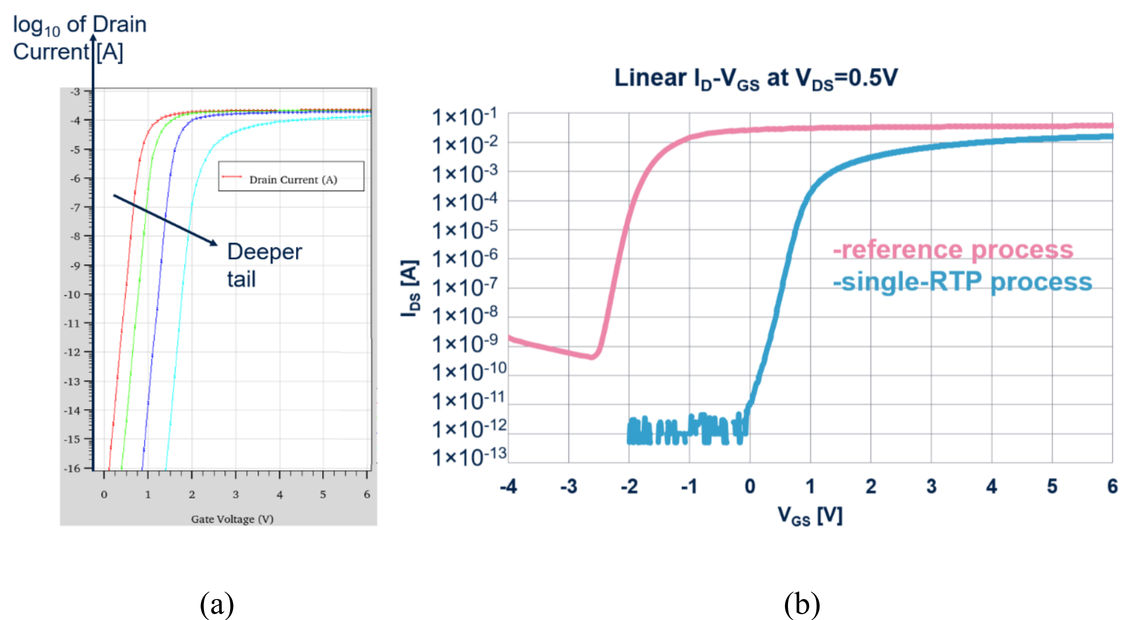
Figure 2.12: (a) p-GaN gate stack and (b) SIMS results from p-GaN region of single-RTP process.

Referring to Figure 2.12, two different regions can be identified based on the SIMS levels of both hydrogen and magnesium:

A. in this first region, which corresponds approximately to the dimension of p-GaN layer, the Mg concentration is at the same level of the hydrogen (H) concentration. As reported in the literature, Hydrogen can produce a passivation effect on Magnesium (preventing Mg to act as an acceptor for GaN), because Mg and H can form chemical bonds, resulting in Mg–H complexes [18]. Therefore, the flatness of the CV measurement previously reported can be well explained by the very low active Mg (low acceptor concentration) induced by high H levels in p-GaN.

B. The second region, corresponding to the AlGaN barrier region, shows a difference between Mg and H concentrations, where Mg is consistently higher than H. This suggests a non-zero Mg concentration that can act as acceptor close to the AlGaN barrier, given the fact the hydrogen levels are not enough to passivate all Mg. This finding, as studied in the previous section, can justify a positive shift of V_{PO}/V_{th} with respect to a fully undoped GaN cap, as observed in both the CV and IV measurements.

Therefore, experimental results are qualitatively in agreement with TCAD simulation trends (Figure 2.13) and the effect of Mg out-diffusion in AlGaN on V_{PO} has been experimentally confirmed also in the case of non-optimized p-GaN activation, which is the case of the single-RTP process.



(a) (b)

Figure 2.13: (a) TCAD simulations of the transfer curves (VDS = 0.5 V) for different acceptor out-diffusion profiles along the p-GaN/AlGaN region and (b) experimental transfer curves of devices with different Mg-H out-diffusion in AlGaN

2.4.3 Comparison between Single- and Multiple-RTP process

Multiple-RTP process devices have been analyzed in this subsection and compared to the results of the single-RTP process devices. As previously described, multiple-RTP devices share the same nominal Mg doping as the single-RTP process but have been fabricated with an optimized thermal treatment (RTP), applied for improving the activation in p-GaN. SIMS analyses have been performed also in this case and the results are shown in Figure 2.14: as can be seen, this time the measured H concentration is clearly lower than Mg even along the p-GaN thickness (and not only in the AlGaN region), suggesting that a significant portion of the Mg could contribute to the net acceptor concentration of the p-GaN.

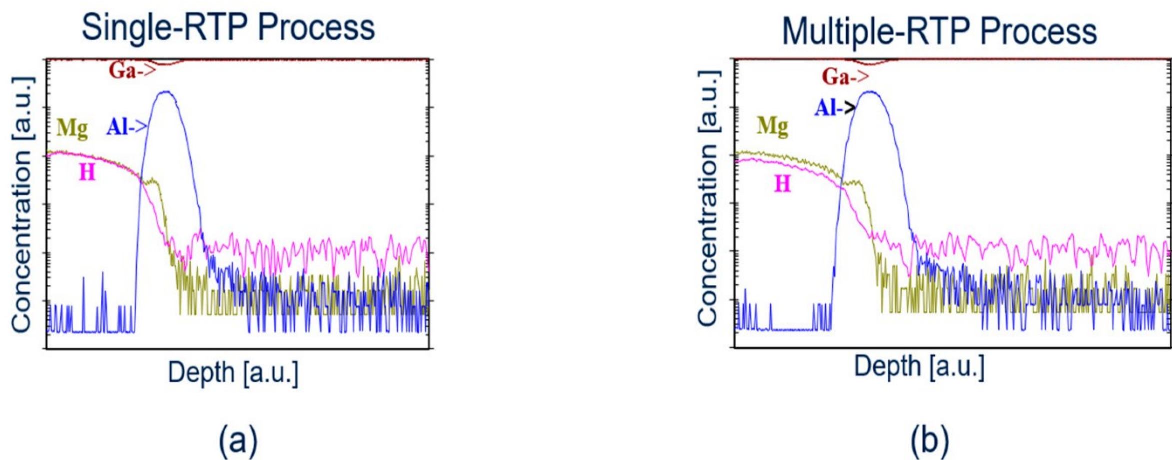


Figure 2.14: Comparison between SIMS results coming from the p-GaN region of (a) single-RTP process and (b) multiple-RTP process.

Gate capacitance measurements have been carried out on multiple-RTP devices, and they show the expected non-flat behavior (typical of a Schottky junction) after the threshold, confirming the improved activation of Mg. Moreover, IV measurements performed on the same devices have shown an increased value of V_{PO}/V_{TH} with respect to what obtained for the single-RTP process HEMTs (Figure 2.15). This is consistent with a pulling-up of the band diagram (described with TCAD simulations in the previous section), which, in this case, is induced by the improved Mg activation in p-GaN. By making use of equation 2.2, the net acceptor concentration in p-GaN could be extracted, resulting in about 2×10^{18} cm^{-3}. This value is highly dependent on the annealing process (it can be found that in this specific case the activation efficiency is 20% with respect to nominal Mg doping of about 1×10^{19} cm^{-3}) and it is in line with other literature findings regarding p-GaN HEMTs where values in the 1×10^{17} cm^{-3} - 1×10^{20} cm^{-3} range are usually reported with ionization levels of few % at room temperature corresponding to activation energies around 160-200 meV [12,17,19].

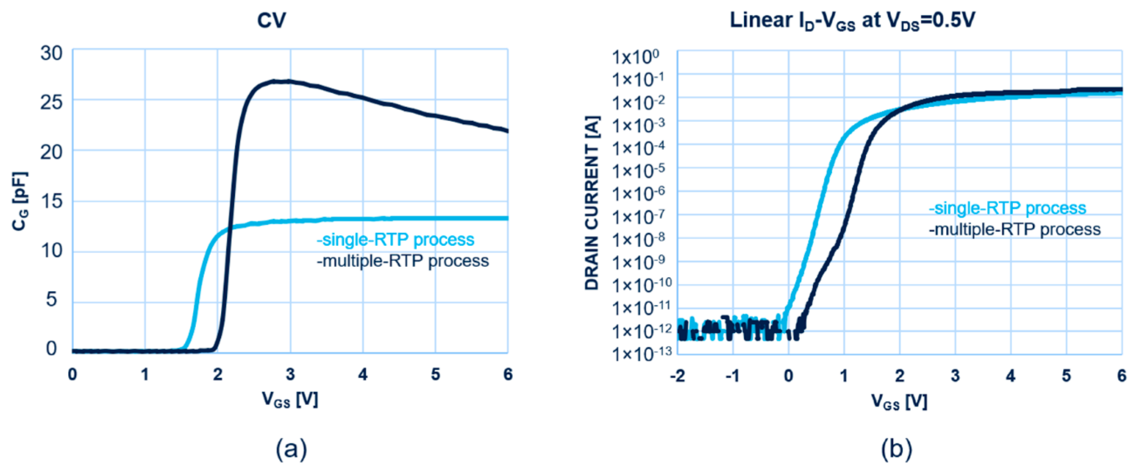


Figure 2.15: (a) Gate capacitance and (b) linear transfer characteristic comparison between single- and multiple-RTP process.

One of the advantages of the higher pinch-off voltage is related to the link between V_{PO} and I_{DSS}. In fact, as mentioned before, a higher V_{PO} means improved pinch-off of the channel at zero gate bias, which can result in a lower and more stable drain leakage current up to high drain voltages, as shown in Figure 2.16. In particular, given the fact that the main leakage contribution to the overall DUT drain leakage consists of the source leakage (while gate and substrate components are negligible), the drain leakage reduction observed in the case of multiple-RTP process is linked to a reduction of the leakage between drain and source.

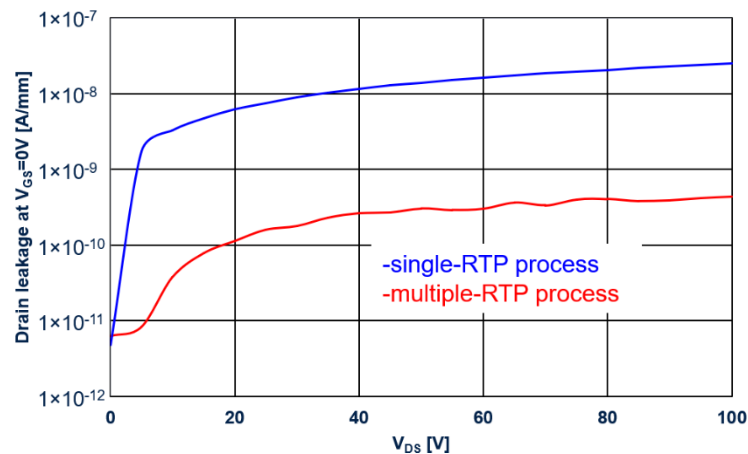
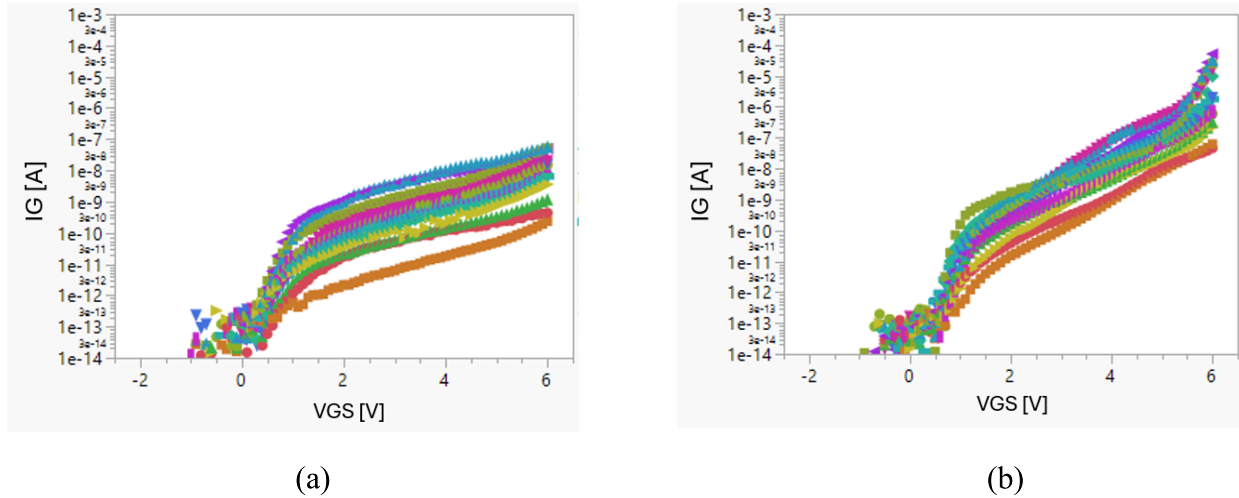


Figure 2.16: Comparison between drain leakage (at zero gate bias) of single- and multiple-RTP processes.

In terms of gate leakage, instead, the improved p-GaN activation has another effect, since it leads to an increase of hole injection. Igss measurements were performed, and they confirmed the expectations, i.e. higher I_{GSS} was measured for multiple-RTP process devices, as reported in Figure 2.17.



(a) (b)

Figure 2.17: Comparison between gate leakage of (a) single- and (b) multiple-RTP process (measurements performed on several devices).

Apart from the improved off-state behavior, an improved p-GaN activation (like the multiple-RTP process) can produce also other advantages for the on-state operation of the device in terms of the transconductance (g_m), on-resistance (R_{ON}), and saturation current (I_{SAT}). In particular, the improved gm value is a result of the increased gate capacitance value, given the fact the transconductance is not only dependent on the electron mobility but also on the gate capacitance [20]. Moreover, statistical measurements performed on single-RTP and multiple-RTP devices showed a reduced R_{ON} intra-wafer spread in the latter case, as shown in Figure 2.18.

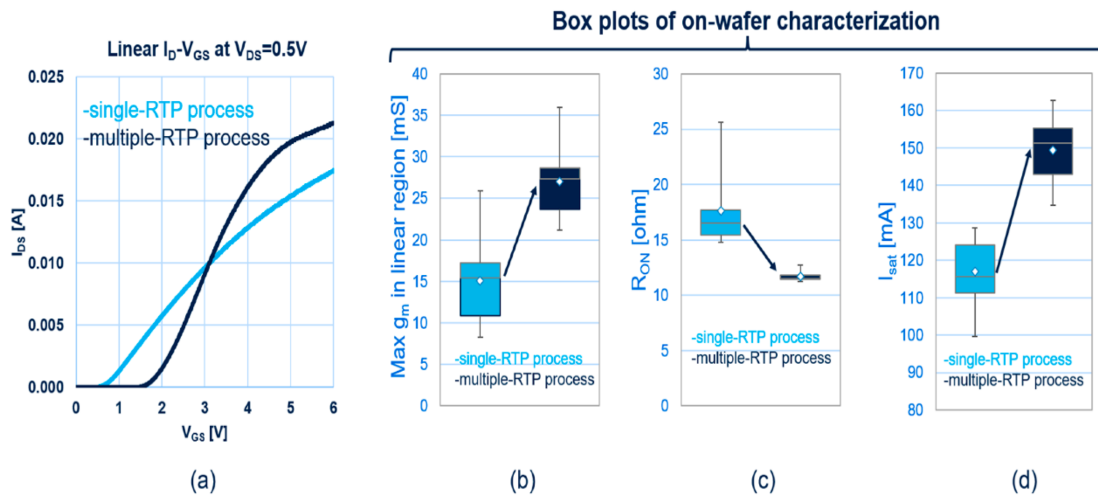
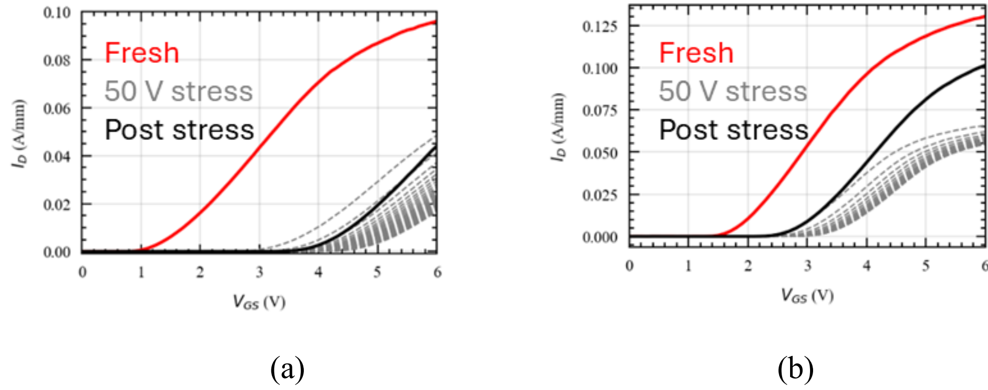


Figure 2.18: Comparison between single- and multiple-RPT process in terms of (a) linear IV characteristic, (b) maximum transconductance, (c) on-resistance and (d) saturation current.

Another advantage of the improved p-GaN activation has been observed in terms of dynamic performance: a reduced dynamic threshold voltage shift has been measured in the case of multiple-RTP process, as shown in Fig. 2.19. This effect could be linked to the better channel potential control that is achieved in the improved RTP case.



(a) (b)

Figure 2.19: Dynamic monitoring with OTFs (1000 s) of the linear IV (V_{DS} = 0.5 V) characteristic of (a) single-RTP process and (b) multiple-RTP process.

Finally, on the improved devices (multiple-RTP process), a complete temperature characterization of the main on-state parameters has been performed. The results of this characterization have been summarized in the plots reported in Figure 2.20, where all the parameters have been normalized with respect to their room temperature value: of course, at high temperatures, a reduction of the current levels is observed due to mobility degradation.

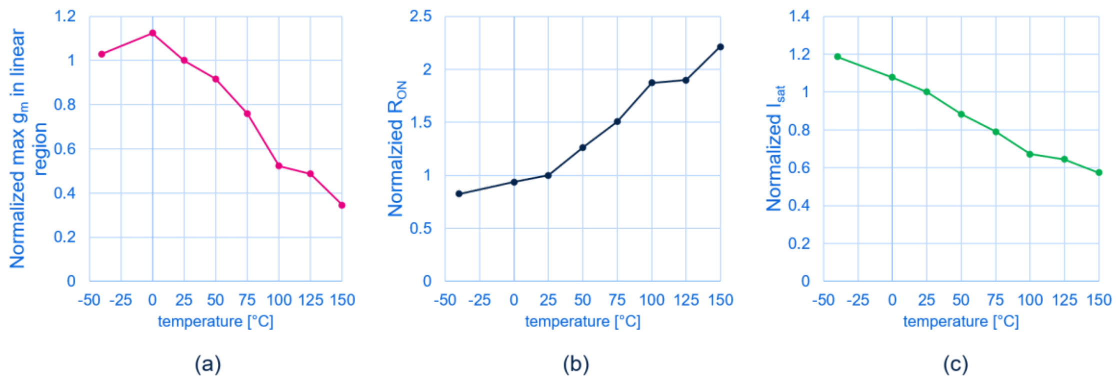


Figure 2.20: Experimental temperature normalized trends measured on multiple-RTP process DUTs: (a) transconductance, (b) on-resistance and (c) saturation current.

2.5 Conclusion

A comparison between AlGaN/GaN HEMTs with undoped and p-doped GaN gate modules has been investigated in this chapter. TCAD simulations have been carried out to study the effect of the net acceptor concentration of the gate stack on the band diagram of the structure. This preliminary study has been useful to interpret the following characterizations, especially in terms of the pinch-off voltage of the transistor. Indeed, experimental results on three different p-GaN cap processes have been compared. In particular, at first, the effect of a poorly activated p-GaN process has been compared to an undoped p-GaN process, underlying the different impact of the Mg close to the Schottky interface and the one close to the AlGaN region (Mg out-diffusion). Then, the results obtained on multiple-RTP process devices (improved p-GaN activation with

respect to the other case) have been analyzed in detail, showing increased V_{PO} values, more stable off-state performances (at a zero-gate voltage) in terms of a reduced drain leakage, and better static and dynamic on-state behavior (consisting of reduced on-resistances and enhanced saturation currents).

As a result of the previously commented theoretical study and experimental results, some general considerations can be drawn to summarize the effect of the different Mg activation levels on the VPO:

- Whether the active Mg concentration in p-GaN is high or low, there can be an indirect influence of the Mg doping level on the VPO via its out-diffusion in the AlGaN barrier.
- If the active Mg concentration inside the p-GaN is rather low, the depletion width of the Schottky junction can cover the whole p-GaN layer, reaching the AlGaN barrier, thus pulling down the entire band diagram (→increased 2DEG →V_{PO} lowering).
- If the active Mg concentration in p-GaN is high enough to induce a depletion width shorter than the full p-GaN thickness, there will be no direct dependence of V_{PO} on the specific Mg doping level nor on the gate metal workfunction.

Of course, it is worth highlighting that a stronger magnesium activation can produce, in some cases, one or more of the following drawbacks:

- Higher gate leakage [14].
- Higher hysteresis and VTH instability [21].
- Increased current collapse in dynamic conditions [12].

These issues should be addressed as well while optimizing the activation process, e.g., limiting their impact on the device behavior by implementing additional solutions (improved passivation, pre-passivation cleaning treatments, etc.), e.g. to limit the gate leakage. Another important aspect to be considered is the refinement of the p-GaN growth conditions, e.g., in terms of pressure and temperature, which play an important role in the improvement of the gate stack, since it can modify the Mg incorporation and activation as well. To conclude, this study has underlined the relevance of improved annealing processes for p-GaN HEMTs, by providing a detailed understanding of the important effect of Mg activation. This comprehension was also assisted by a novel DC/AC comparison between undoped and p-doped GaN cap layers. These results can be used as one of the many steps in the optimization of p-GaN HEMTs, both in off-condition as well as in on state.

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3 High-temperature behaviors

Another key aspect of transistors in general and for GaN HEMTs specifically is the high temperature de-rating of the device parameters. In fact, during the operation of actual applications, e.g., in power converters, GaN devices are switching at high power levels and high frequency for many cycles, thus inducing power dissipation (conduction and switching losses) [1]. Therefore, heat production generates an increase of the device temperature, drifting GaN HEMT characteristics from the ones expected at room temperature [2]. It is thus important to study the temperature behavior of the main HEMT parameters to evaluate their degradation and to find proper tailoring of the device to better its performance at high temperature. The main parameter considered for power devices is the on-resistance (R_{ON}), which is the most important figure-of-merit (FOM) of the device when it is used as a power switch. In fact, R_{ON} directly affects the conduction losses of GaN power devices, significantly impacting on the efficiency of switching converters.

Comparing typical temperature R_{on} performance of p-GaN HEMTs versus other technologies is useful to understand advantages and drawbacks of each approach. A typical comparison is reported in Figure 3.1.

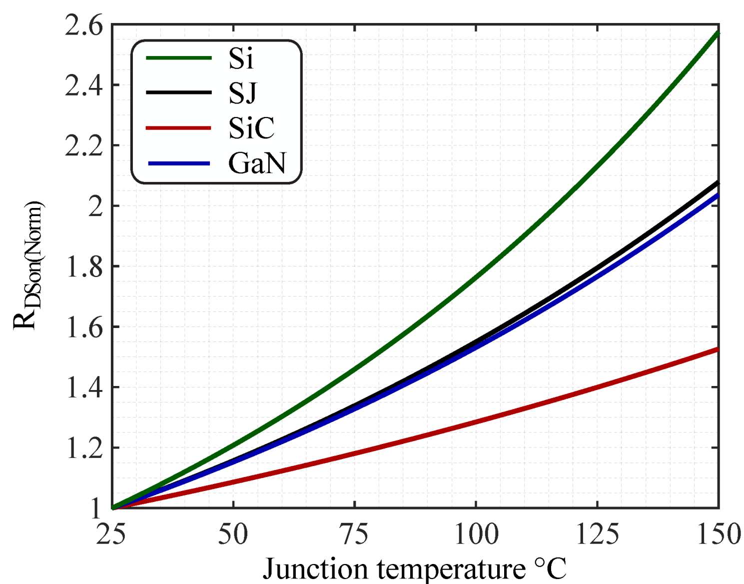

Figure 3.1: Comparison between typical normalized temperature trends for on-resistance of conventional silicon, silicon Superjunction, SiC and GaN devices [3].

In SiC MOSFETs, the total on-resistance is the sum of the channel resistance and the drift layer resistance. These components react differently to heat, creating a partial cancellation effect and this is why SiC is characterized by the least severe temperature derating. Superjunction silicon MOSFETs exhibit instead similar temperature performance with respect to GaN HEMTs and lower than conventional silicon MOSFETs. In fact, since the Superjunction structure blocks the voltage more efficiently, the drift layer can be significantly thinner than the one of a

conventional MOSFET of the same voltage rating. A thinner conducting path means that the drift layer (subject to temperature-induced mobility loss) relative weight on the total on-resistance is small, resulting in a more stable R_{on} across the operating range. In GaN HEMTs, the main conductive path is instead related to the Two-Dimensional Electron Gas (2DEG), whose density (n_s) is linked to sheet resistance through this formula (where R_s represents the sheet resistance and μ_s is the electron mobility):

$$R_S(T) = \frac{1}{e \cdot n_s(T) \cdot \mu_s(T)} \approx \frac{1}{e \cdot n_{s0} \cdot \mu_s(T)} \tag{3.1}$$

However, 2DEG density only experiences a slight decrease with increasing temperature (Figure 3.2), therefore the only relevant temperature effect comes from mobility degradation.

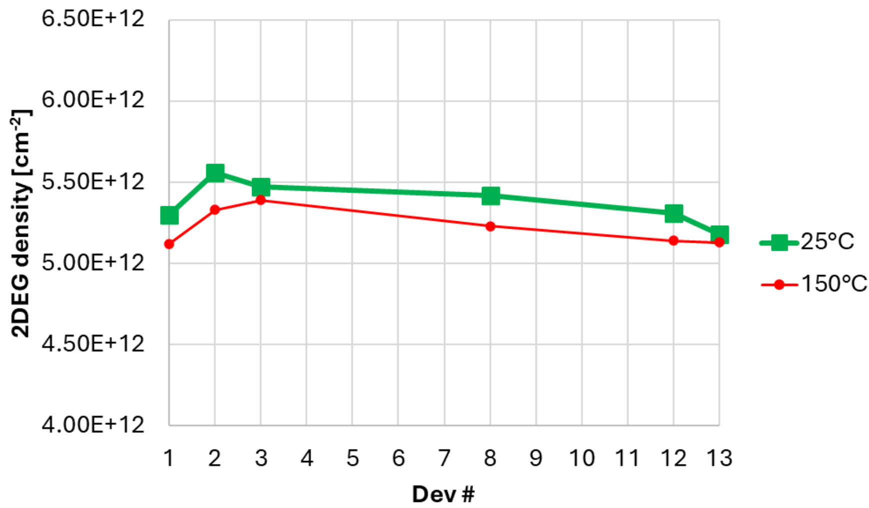

Figure 3.2: Experimental 2DEG density evaluation for different devices at room and 150 °C temperature.

The overall 2DEG mobility is the contribution of different scattering mechanisms (Matthiessen's rule):

$$\frac{1}{\mu_S} = \frac{1}{\mu_C} + \frac{1}{\mu_{SR}} + \frac{1}{\mu_{ap}} + \frac{1}{\mu_{op}} \tag{3.2}$$

At low temperature, Coulomb and Surface Roughness scattering are predominant, but they are constant with temperature while Acoustic and Optical Phonon are temperature dependent: that is what the decrease of 2DEG sheet mobility is generally attributed to optical phonon scattering.

However, polarization-induced 2DEG reduces "impurity scattering" (no doping needed for GaN HEMTs).

In the case of GaN devices, temperature may also have a significant effect on dynamic R_{ON} [4], since it could impact the trapping/de-trapping dynamics [5] and the amount of degradation induced by off-state drain voltage stress [6]. To ensure the correct modelling and optimization of GaN HEMTs, it is crucial to gain insights into the dynamic R_{ON} under conditions that are close to the device operating temperature [7]. This requires careful characterization of the device thermal behavior to be aware of the performances that the device will reach in its final operative scenario. Therefore, in the following sections of this chapter, temperature characterization performed on p-GaN HEMTs both in DC and dynamic conditions are presented and some key results are extracted from this evaluation.

3.1 Devices under test and experimental setup

The analysis reported in this chapter was carried out on wafers fabricated by STMicroelectronics. Figure 3.3 shows a schematic cross section of the p-GaN gate HEMTs investigated in this study (device under test, DUT).

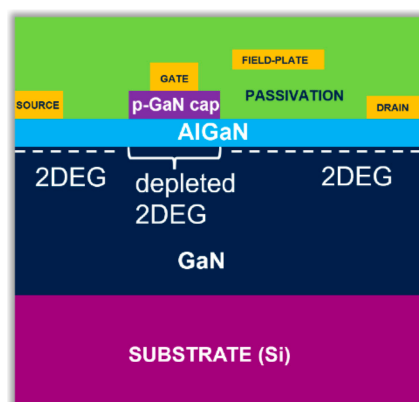

Figure 3.3: Schematic cross-section of the p-GaN DUTs.

In particular, the devices analyzed in this chapter are p-GaN/AlGaN/GaN HEMTs grown on a Silicon(111) p-type substrate via metal–organic chemical vapor deposition (MOCVD). The epitaxial stack consisted of a nucleation layer, an insulating GaN buffer suited to 100 V applications, followed by an AlGaN barrier layer (18 nm thick) with a 20% aluminum concentration. Both ohmic and gate contacts were formed via Ti/Al-based metallization defined by means of a liftoff process.

On-Wafer devices have been interfaced to the instrumentation by means of Form Factor 200 mm Cascade Summit probe system equipped with a chiller for the wafer temperature tuning. The maximum temperature at which devices have been characterized is 150 °C, which is usually considered an upper temperature bound for industrial applications. All the DC/AC characterizations have been performed through a B1505A parameter analyzer (Figure 3.4) while an AM200 PIV system (Figure 3.5) was used to perform the evaluation of the dynamic R_{on}.

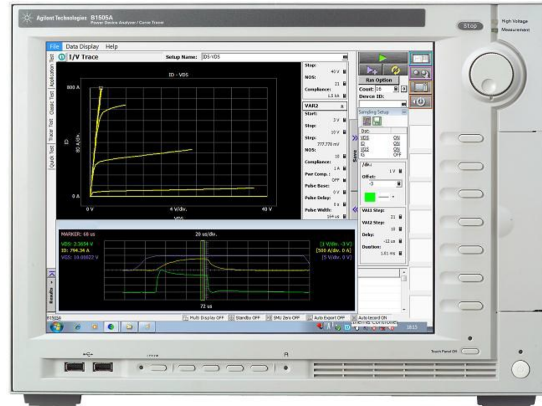

Figure 3.4: B1505A parameter analyzer

Figure 3.5: AM200 system for evaluation OTF PIVs.

3.2 High Temperature Behavior of Static Ron

In this first section, the temperature behavior of the static R_{ON} of a reference process is analyzed.

For the on-resistance extraction, a linear transfer characteristic is performed from zero gate bias up to $V_{GS} = 6$ V and then R_{ON} is evaluated as $R_{ON} = \frac{V_{DS}}{I_D@V_{GS}=6V}$. Then, stemming from this study, two different process variations are evaluated, showing the improvements at high temperature and explaining the possible reason for these improvements. First, it is important to define the R_{ON} Temperature Ratio (RTR) as a FOM for the high temperature behavior. This ratio can be defined as R_{ON} at 150 °C divided by R_{ON} at 25 °C. However, as shown in Figure 3.6, another equivalent way to evaluate this parameter is simply by taking the ratio of the drain current in linear region at 25 °C divided by the value at 150 °C.

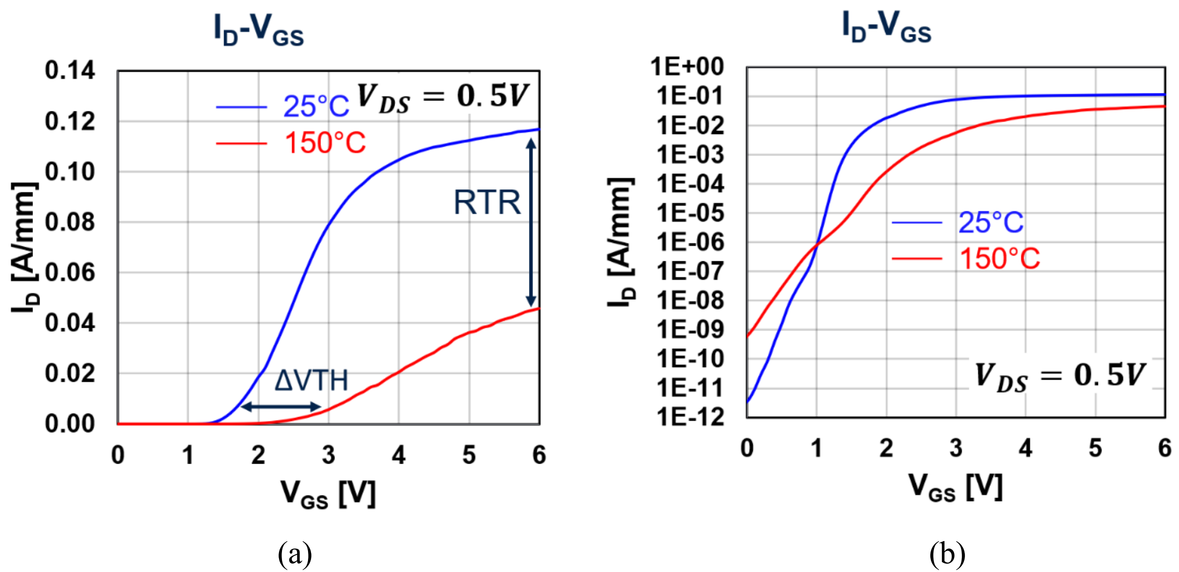

Figure 3.6: Typical linear IV characteristic at 25 °C and 150 °C measured on reference DUTs: (a) linear scale and (b) semi-log scale.

This temperature ratio, i.e., R_{ON}(150 °C)/R_{ON}(25 °C), has been analyzed by taking into account how each different resistive contribution of the structure impacts on the overall on-resistance of the device (see Figure 3.7).

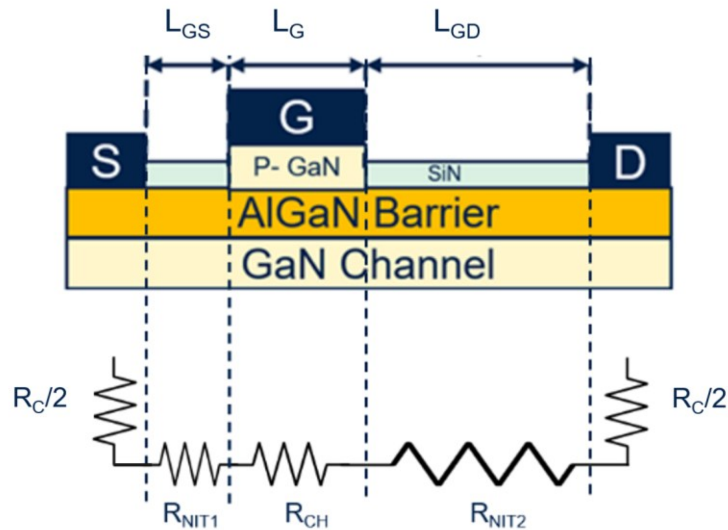

Figure 3.7: Schematic cross-section of the DUT detailing all the different resistive contributions to the overall on-resistance.

Specific contact resistance slightly increases (since it is characterized by metal-like behavior) while sheet resistance variations depend on mobility variations. Differently from high-voltage devices like 650 V p-GaN HEMTs ($L_{GD} \leq 20$ µm, $L_G \leq 2$ µm), where the resistance in the access regions represents the main contribution on the overall on-resistance [8,9], 100 V rated devices ($L_{GD} \leq 2$ µm, $L_G \leq 1$ µm) are characterized by a relevant weight of the resistance under the p-GaN gate, namely the channel resistance (R_{CH}). In particular, the analysis of the temperature behavior of each resistive portion of the HEMT (realized through ungated and gated TLM structures) has revealed that, for the technology under evaluation in this chapter, R_{CH} has the largest impact on R_{ON} at 150 °C, as reported in Figure 3.8.

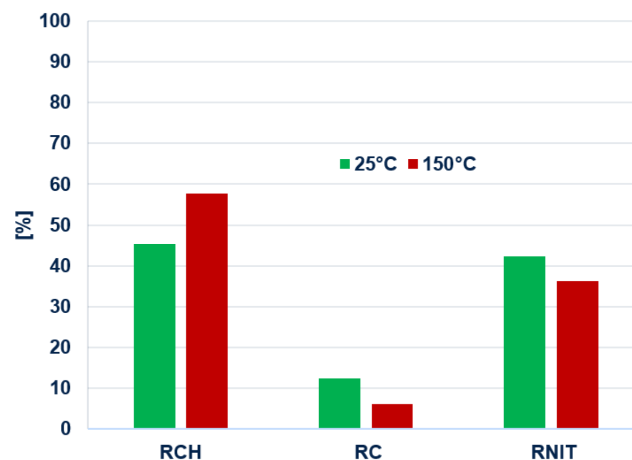

Figure 3.8: Weight of resistive contributions with respect to the total on-resistance (R_{NIT}=R_{NIT1}+R_{NIT2}).

Therefore, R_{CH} has been further investigated through IV measurements performed on a dedicated HEMT structure (Figure 3.9 and 3.10) with increased gate length ($L_G >> L_{GD}+L_{GS}$).

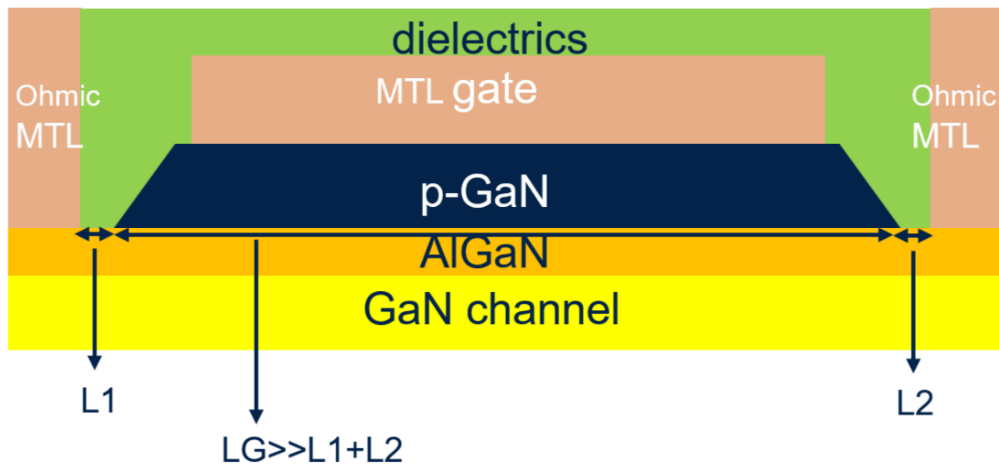

Figure 3.9: Schematic cross-section of the dedicated HEMT structure for channel resistance study.

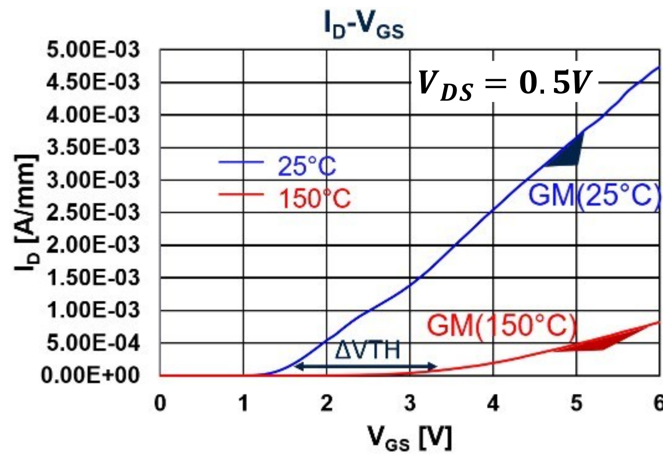

Figure 3.10: Typical linear IV characteristics measured on dedicated HEMT structures for channel resistance evaluation.

As can be observed, the overall temperature variation of R_{CH} is dependent on both the threshold voltage (V_{TH}) increase and the transconductance (gm) reduction: these two effects are propagated also to the 100 V DUT.

One relevant remark is that the IV temperature behavior of D-Mode HEMTs (without p-GaN) does not show the V_{TH} shift observed in the case of p-GaN HEMTs. In particular, D-mode devices, sharing the same epitaxial structure up to the AlGaN barrier layer as in the DUTs, have

been characterized at room and high temperature, showing quite stable V_{TH}, as reported in Figure 3.11, consistently to literature results [10]. On the other hand, the sub-threshold leakage increases at high temperatures for D-Mode HEMTs (Figure 3.11) as well as it does for E-mode HEMTs (Figure 3.6), as also observed in literature [11,12].

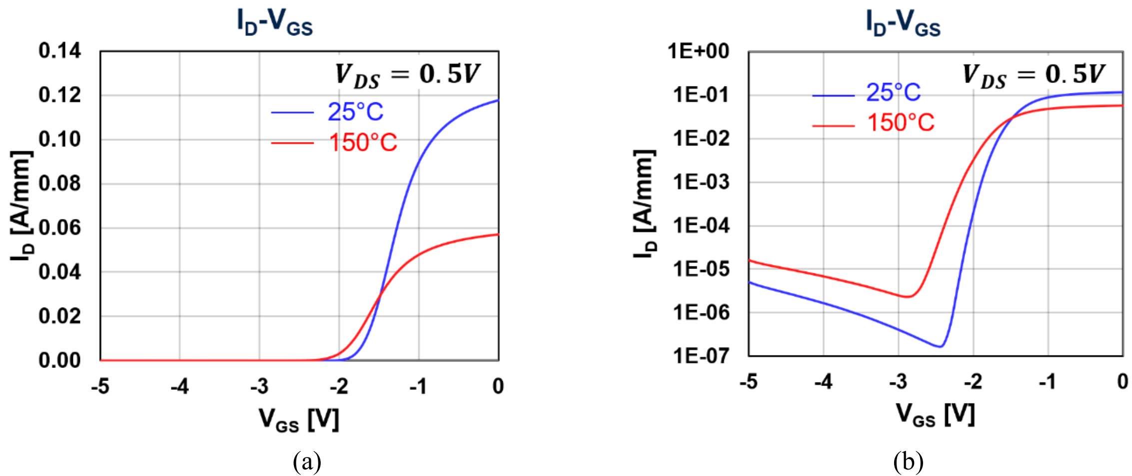

Figure 3.11: Typical linear IV characteristic at 25 °C and 150 °C measured on D-mode GaN HEMTs in (a) linear scale and (b) semilog scale.

The high temperature positive V_{TH} shift in the case of Schottky p-GaN gates like the STD process ones can be explained by two main factors: the first is that, at higher temperature, gate leakage is increased already at low positive gate bias and this implies a larger voltage drop across the Schottky junction and a reduced voltage drop across the p-i-n diode, meaning that a larger V_{GS} is required to turn on the channel [10]; the second is that temperature enhances electron emission and trapping from 2DEG to bottom p-GaN, leading to a negative charge accumulation on top of the AlGaN barrier, which further hinders 2DEG channel formation [13,14]. In terms of transconductance, instead, the expected temperature degradation mechanism should come from electron mobility [15-17]. Actually, this is not the only effect observed in the case of DUTs. In fact, it must be remembered that in a field-effect transistor g_m is proportional to both mobility and gate capacitance. CV measurements performed on DUTs proved that gm decrease at high temperature is linked not only to the mobility degradation but also to the decrease of the gate capacitance (Figure 3.12). It is worth noticing that for high positive V_{GS} the slope of the C_G does not significantly change with temperature: in fact, while acceptor ionization is increased at high temperature, the slope of the capacitance is only dependent on the net acceptor concentration, which is not modified at 150 °C. However, at high temperature, small changes on the slope can still be observed because of the parasitic effect of the series resistance [18].

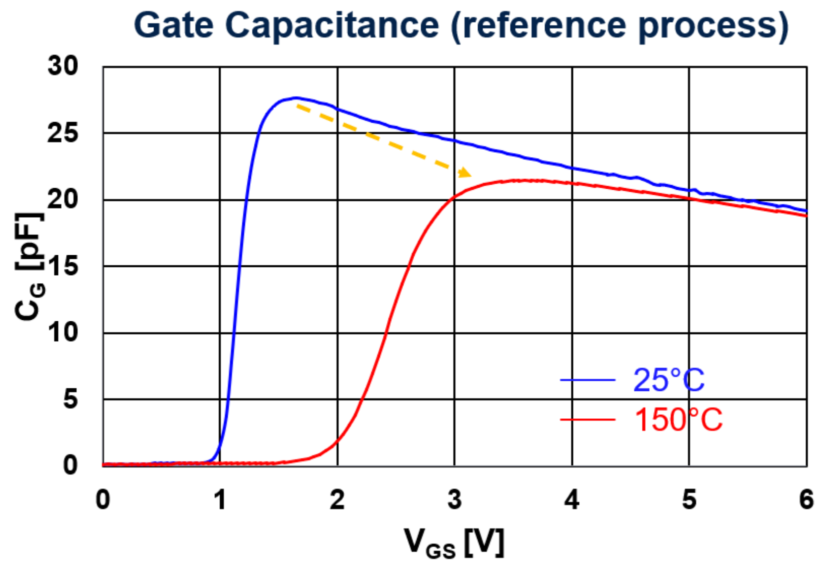

Figure 3.12: Typical gate capacitance at 25 °C and 150 °C measured on DUTs fabricated with STD process.

Based on these considerations, two process variations have been then proposed to improve device performances at high temperature, while ensuring the correct normally-off behavior: 1) process A consisting in an improved thermal annealing for the magnesium activation in the p-GaN gate; 2) process B related to an increase of the nominal magnesium concentration of the p-GaN. Both processes have been characterized by IV measurements at room and high temperatures, and the results are shown in Figure 3.13.

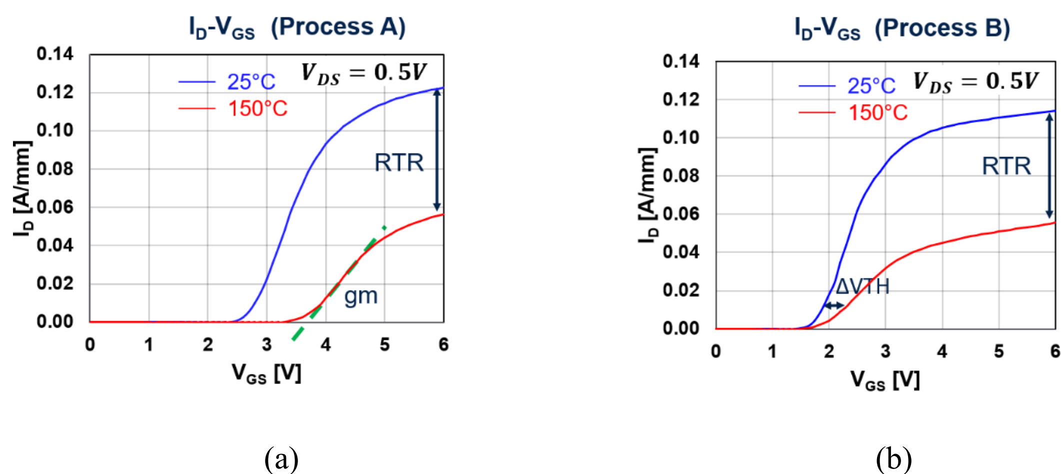

Figure 3.13: Typical linear IV characteristics at 25 °C and 150 °C measured on DUTs fabricated with (a) process A (b) and process B.

Stemming from these measurements, RTR, transconductance and V_{TH} temperature variations have been evaluated on both processes, and the results have been reported in Figure 3.14.

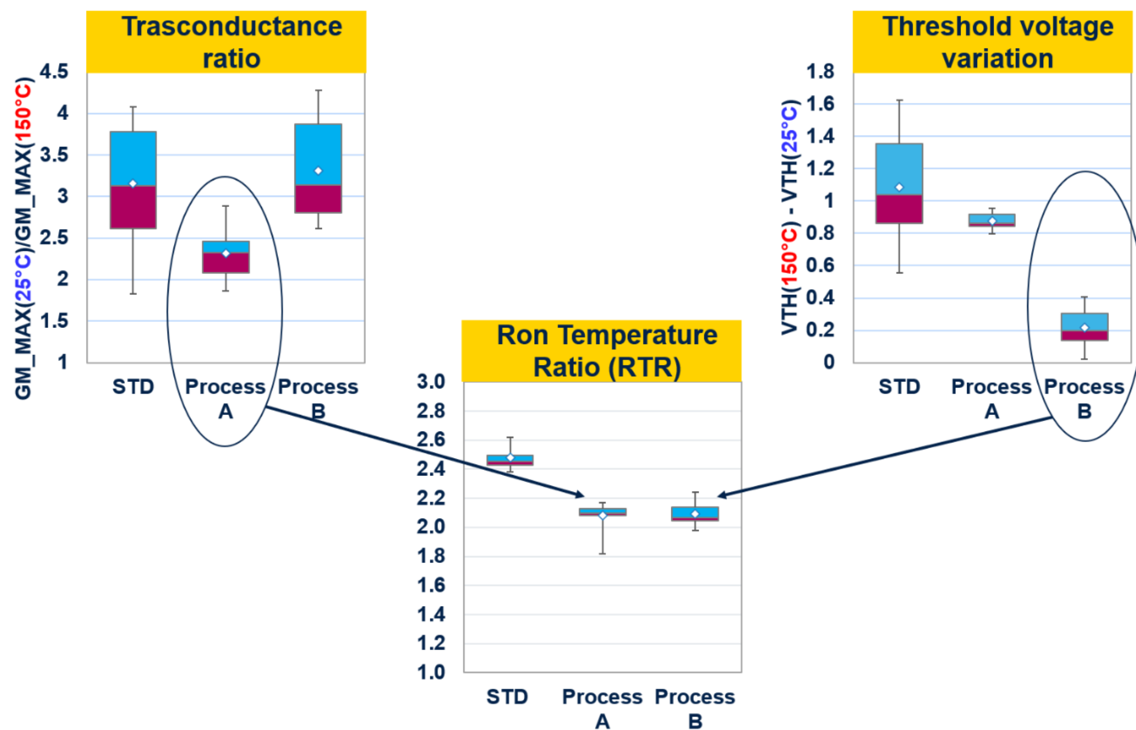

Figure 3.14: Summary of temperature transconductance ratio, threshold voltage shift and RTR for STD process and improved process A and B.

As shown in Figure 3.13 and 3.14, both process A and B allow to reach a reduced R_{ON} temperature ratio: however, this is achieved in different ways since process A is effective in obtaining a reduced V_{TH} shift at high temperature while process B helps in improving the maximum transconductance at 150 °C. The explanation of these phenomena can be found through the analysis of the measurements reported in Figure 3.15 and 3.16. In fact, in the case of process A, the stronger p-GaN activations leads to higher gate capacitance (increased acceptor concentration): in this way, the CV curve become more insensitive to V_{GS} increase (reduced depletion width of the Schottky junction) and even if at 150 °C there is still V_{TH} shift, the gate capacitance value remains quite high. Therefore, in this case, the only practical contribution to the transconductance decrease is due to the mobility degradation.

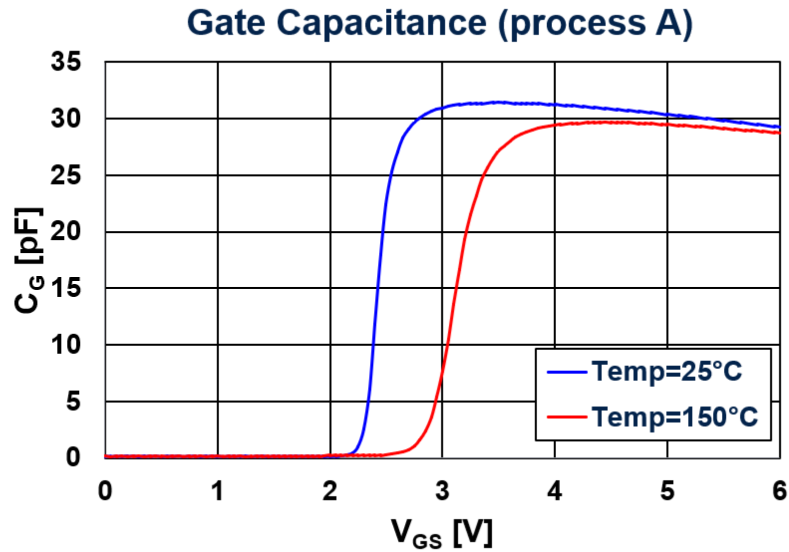

Figure 3.15: Typical gate capacitance at 25 °C and 150 °C measured on DUTs fabricated with process A.

For what concernes process B, instead, a significant gate leakage increase has been measured, also at low V_{GS}: this implies that hole injection mechanism from gate metal has been increased very much already at room temperature and then, no significant charge balance variation are induced when increasing the DUT temperature.

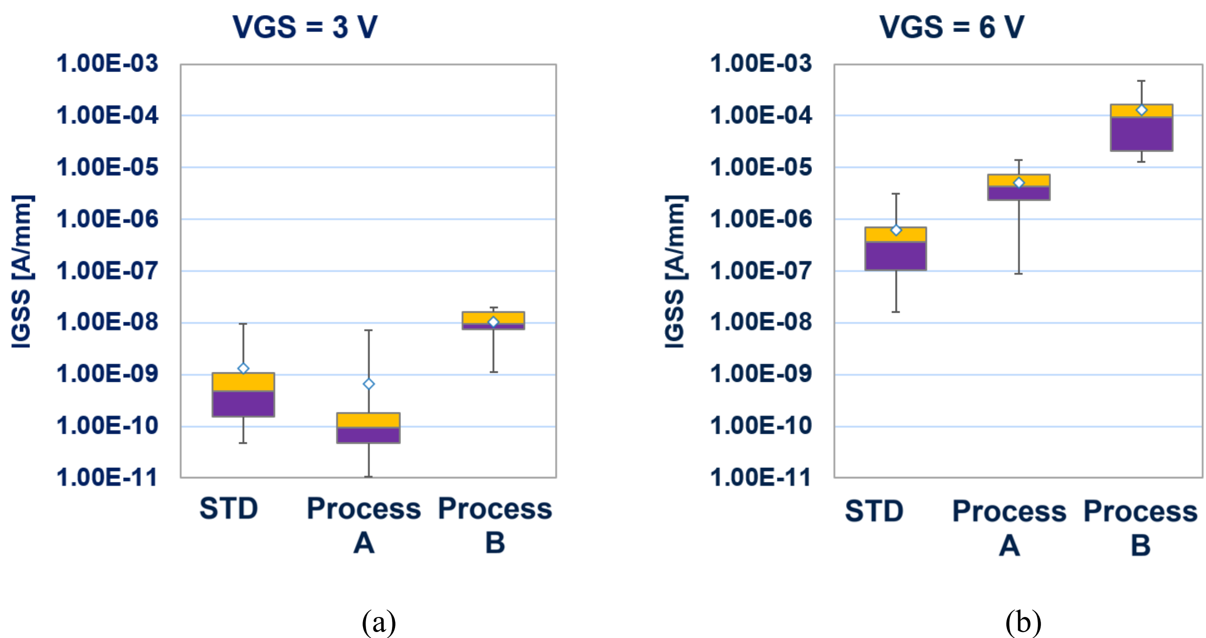

Figure 3.16: Gate leakage measurements at (a) $V_{GS} = 3$ V and (b) $V_{GS} = 6$ V performed at room temperature on several DUTs fabricated with all three processes.

Another advantage of the proposed processes is that they are also characterized by higher saturation currents at room temperature and also lower relative degradation at 150 °C. This has been evaluated through the I_{SAT} Temperature Coefficient ("ITC"), defined as

$\left(\frac{1}{125}\cdot\left(\frac{I_{sat,150C}}{I_{sat,25C}}-1\right)\right)$, as shown in Figure 3.17.

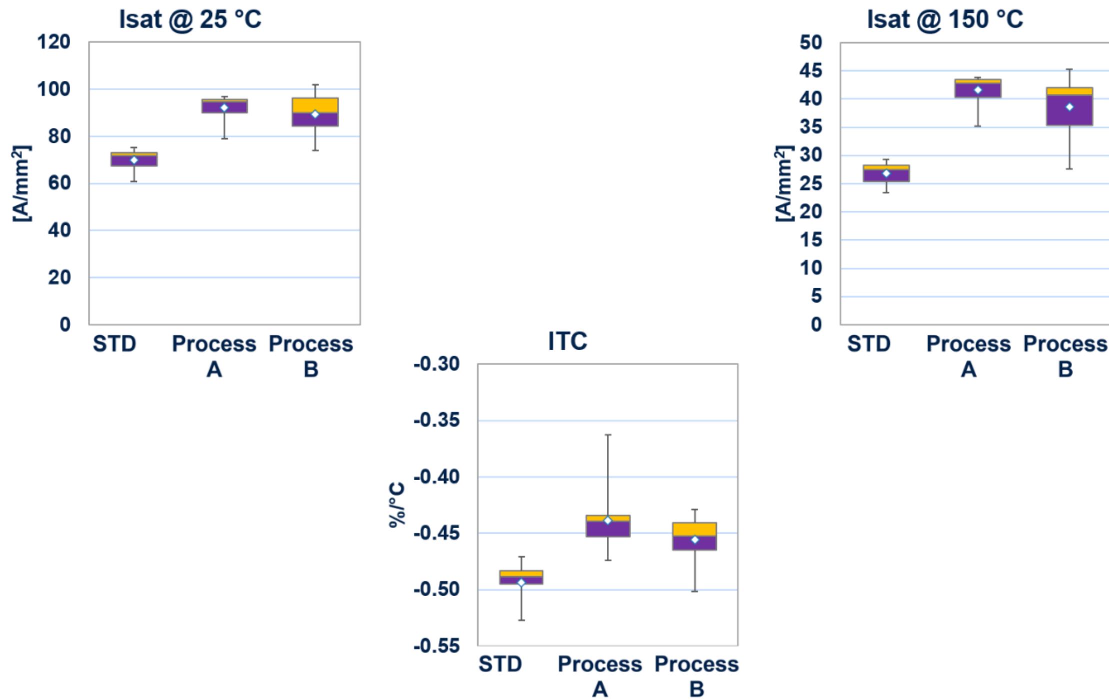

Figure 3.17: Boxplots of 25 °C, 150 °C and temperature coefficient data for saturation current of DUTs, compared among the three different processes.

As observed in Figure 3.16, the main side effect of process A and B is instead related to an increase in the gate leakage, which must be optimized with other process variations.

3.3 Temperature Effect on dynamic RON-degradation

In this section, the high temperature evaluation has been focused on the dynamic R_{on} of p-GaN HEMTs. The experimental procedure for dynamic-R_{ON} evaluation under off-state drain voltage stress is schematically depicted in Figure 3.18.

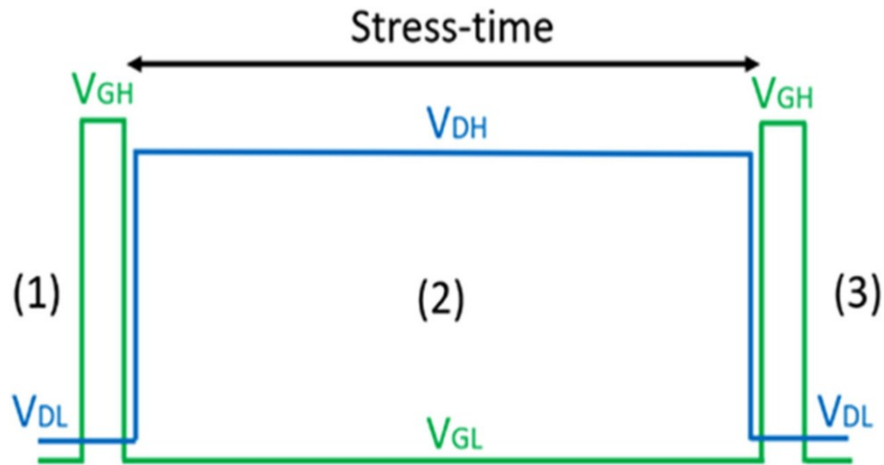

Figure 3.18: Gate and drain voltage waveforms applied on DUTs for evaluating dynamic Ron after static drain stress.

The fresh R_{ON} (1) is measured by pulsing V_{GS} (2 μs) to V_{GH} = 6 V, while V_{DS} is kept at V_{DL} = 0.5 V to bias the DUT in its linear region. Then (2) an off-state stress is performed by biasing the DUT at V_{GL} = 0 V and $V_{D\,H}$= 50 V for a predefined time interval (stress-time). At the end of the stress (3) VGS is pulsed again to V_{GH} to acquire the R_{ON} value after stress.

Also in this case, Devices Under Test (DUTs) are 100 V p-GaN gate AlGaN/GaN HEMTs grown on Silicon substrate fabricated with process B-like improvements (described in the previous section). The fresh I_D-V_{GS} characteristics have been measured for the DUTs devices at different temperatures (T), from 25 °C to 150 °C, with 25 °C step, and the results are reported in Figure 3.19.

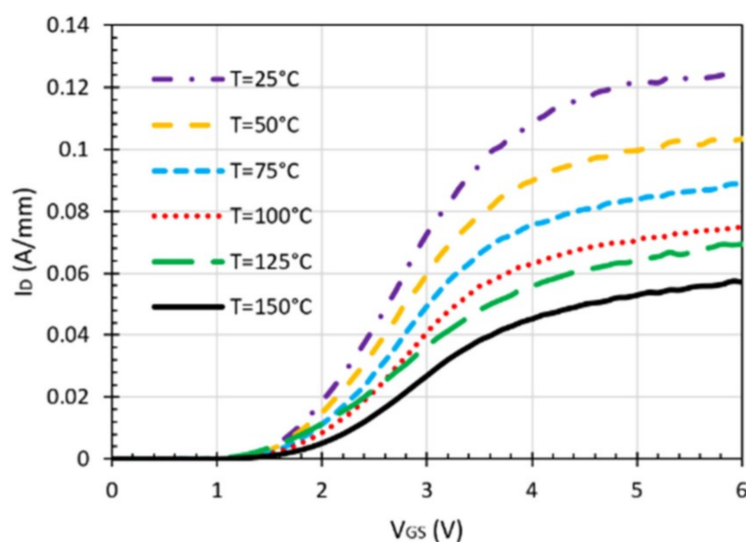

Figure 3.19: Typical linear IV (V_{DS} = 0.5 V) characteristics measured on DUTs at different temperatures.

As commented also in the previous section, an increase in temperature yields to a lower current level in linear region, due to a reduced electron mobility [19]. It has been observed that the increase of the fresh on-state resistance (R_{ON0}) with increasing temperature is almost linear in the considered temperature range (Figure 3.20), in agreement to what observed in literature [12,20,21].

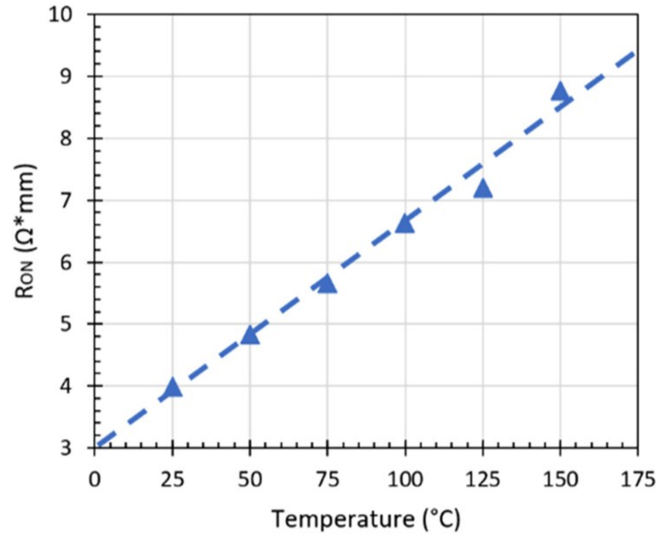

Figure 3.20: Typical on-resistance measured on DUTs at different temperatures.

Moreover, it must be underlined that, in the case of negligible V_{TH} shift with temperature (as observed on process B devices analyzed in section 1), the RTR can be well correlated with another parameter, i.e., the Mobility Temperature Ratio ("MTR"), defined as $\mu_n(25°C)/\mu_n(150°C)$. This correlation is shown on Figure 3.21. MTR data were extracted by combining the results of TLM and CV measurements performed on wafer, given that $\mu_{2DEG} \approx \frac{1}{q \cdot n_{2DEG} \cdot R_{S,2DEG}}$.

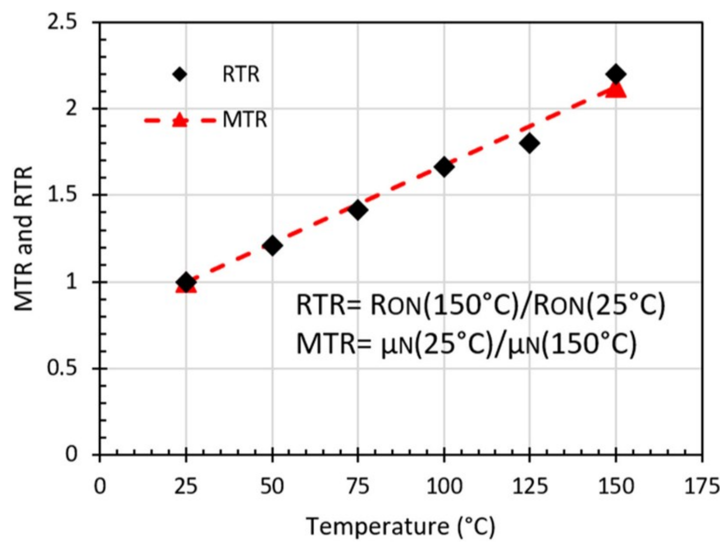

Figure 3.21: Comparison between R_{on} Temperature Ratio (RTR) and Mobility Temperature Ratio (MTR) evaluated for different temperatures.

At this point, the experimental procedure for the dynamic R_{on} evaluation was applied on DUTs, by varying the stress-time between 15 s and 1000 s to see the impact of this parameter as well of the temperature on the amount of R_{ON} degradation.

In Figure 3.22, R_{ON}-degradation (R_{ON}/R_{ON0}) results obtained for different stress times and different temperatures in the 25 °C to 150 °C range have been reported.

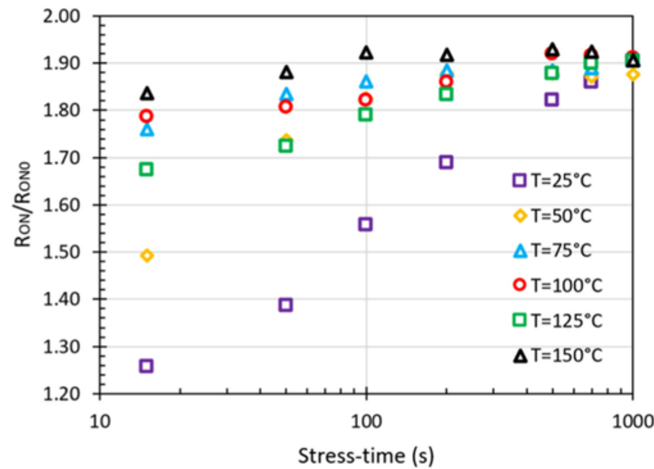

Figure 3.22: Dynamic R_{on} evaluation for different static stress time at different temperatures (typical values).

Looking at Figure 3.22, two important effects can be observed: (i) At 25 °C the R_{ON}-degradation increases with the applied stress-time and requires about 1000 s to reach a steady state condition. In fact, this time duration is consistent with the hole emission model of C-doped buffers described in the introduction; (ii) At higher T values, the time required for reaching the R_{ON}/R_{ON0} plateau reduces. Moreover, after 1000 s, the degradation level seems weakly affected by the specific DUT temperature.

This observation has been confirmed also by additional measurements of the steady-state dynamic R_{ON}/R_{ON0} behavior at different temperatures, obtained for a stress-time of 1000 s (Figure 3.23).

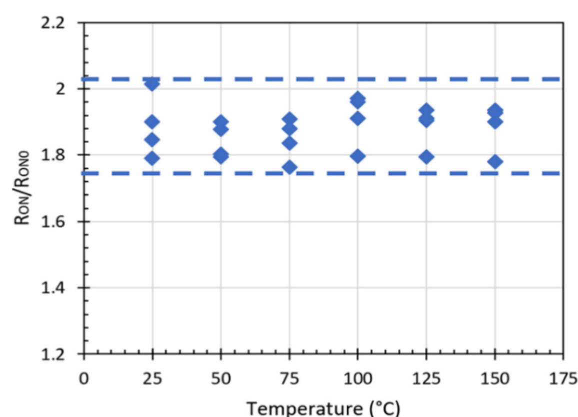

Figure 3.23: Dynamic R_{on} measurements after 1000 s static stress at different temperatures.

Therefore, it can be concluded that relative the amount of degradation impacting R_{ON} is insensitive to temperature. Actually, this is valid if and only if two important conditions are satisfied: (i) the stress time is long enough to appreciate the complete degradation induced at steady-state and (ii) no additional trapping/de-trapping mechanisms are generated at higher temperatures. This finding is totally in line with the theoretical expectations. In fact, the ratio R_{ON}/R_{ON0} is directly proportional to the ratio between the electron density available in the two-dimensional electron gas (2DEG) in the pre- and post-stress conditions (n_0/n). Assuming that the trapping/de-trapping mechanism occurring in the considered temperature range is always the same, the charge variation ($\Delta n = n_0 - n$) induced by the applied stress will be weakly affected by temperature. In fact, since temperature is expected to have approximately no impact on the 2DEG charge density (as mentioned in the previous section), the ratio n0/n is expected to be constant at different T (within the range under exam), resulting in the same R_{ON}/R_{ON0} degradation.

Consequently, this suggests the possibility to test the dynamic R_{ON} degradation at one single temperature and then extrapolate the R_{ON} after stress in the whole temperature range by simply measuring its fresh value (R_{ON0}) at each considered temperature. This could significantly speed up the time required for a complete dynamic-R_{ON} temperature evaluation, always under the assumptions that (i) the degradation is evaluated at equilibrium and (ii) no additional trapping/de-trapping mechanisms are introduced by operations at higher temperatures.

3.4 Conclusion

A study of the high temperature behavior of the on-resistance in reference 100 V p-GaN transistors has been carried out by analyzing each different resistive portion along the pitch of the transistor. As a result, the relevance of the resistive component under the p-GaN gate module in the 100 V technology under exam has been proved, showing that its increase with temperature is caused both by the positive V_{TH} shift and by the g_m degradation. In particular, a new finding was that the transconductance degradation can be linked not only to mobility reduction but also to the gate capacitance reduction. To improve the high temperature behavior of the DUTs, while preserving normally-off operation, two process variations have been proposed, consisting of A) an improved thermal annealing for Mg activation; B) an increase in the nominal Mg concentration. It has been shown how both processes are effective in reducing the R_{ON} Temperature Ratio, acting respectively on the g_m degradation and on the V_{TH} shift and these findings have been explained through additional CV and gate leakage measurements. This work has further confirmed the dominance of the R_{CH} component on the total on-resistance of low voltage (e.g.,100 V) p-GaN HEMTs and traces the road for further improving its thermal stability. Moreover, the temperature effect on R_{ON} degradation induced by off-state drain voltage stress has been studied in 100 V p-GaN HEMTs. The invariance of the relative R_{ON} degradation at different temperatures has been observed on several samples, suggesting the generality of the observed behavior. This effect has been also theoretically justified, in the case of one single trapping mechanism for all the considered temperature range, thus providing a novel interpretation to a very important experimental observation. This result allows to reduce the number of characterizations required for evaluating the R_{ON} degradation under different thermal

conditions.

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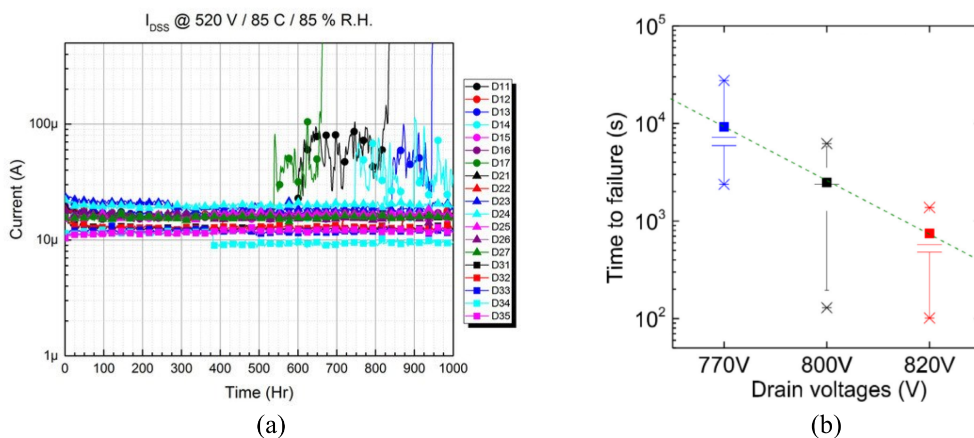
4 Drain and gate static reliability

In addition to the high temperature behavior, the continuous switching over time required by the usual power applications implementing p-GaN HEMTs suggests another key feature that must be carefully investigated, namely reliability. Reliability is generally defined as the probability that a device (the transistor in this case) will perform a required function under defined conditions (of voltage/temperature/pressure/humidity, etc. [1]) for a specified period of time. The reliability assessment is usually performed through different sets of time-limited characterizations that focus on a specific part of the device or a specific electrical condition and then, starting from these results, a more general long-term behavior is predicted. This is quite useful in order to estimate the degradation of the performance under specific conditions and to ensure that the large majority of fabricated devices are not going to fail during their functioning. More specifically, devices can be evaluated both in terms of dynamic and static reliability: the first one concerns how the device behaves during switching thus involving high-frequency operation and coupling the interaction of gate and drain; the latter, instead, focuses on constant, non-changing stress applied to the gate or drain terminal. In this chapter, the focus will be on the static reliability of gate and drain of p-GaN switches, investigated through TCAD simulations and experimental results performed on 650V p-GaN HEMTs.

4.1 TCAD simulation study of HTRB-induced current collapse

Given the fact that power HEMTs are switching between an on state and an off state, both conditions can induce some kind of failure or degradation and must be studied separately for a better understanding of the phenomena involved. Static drain reliability involves stressing of the drain terminal only, while having all the others shorted to ground. Stress characterizations can be aimed either at the lifetime prediction at maximum voltage rating (Time-Dependent Drain Breakdown, TDDB), generally performed up to DUT failure (as shown in Figure 4.1), or at the robustness evaluation at maximum voltage rating (or fractions of it), in terms of performance degradation (High Temperature Reverse Bias, HTRB), generally performed up to 500 or 1000 hours (Figure 4.1).



(a) (b)

Figure 4.1: (a) Typical drain leakage monitoring during HTRB stress from [2]. (b) Typical lifetime prediction plot with TDDB time-to-failure data from [3].

In this work, a study on packaged p-GaN 650 V HEMTs under HTRB stress was carried out. DUTs are MOCVD-grown p-GaN HEMTs (Figure 4.2) characterized by nominal gate driving at V_{GS} = 6 V. HTRB tests are usually performed as time-efficient accelerated aging tests by stressing DUTs at high voltage and high temperature. In particular, after the stress, devices showed a non-recoverable degradation of the on-resistance. The aim of the study is to understand the physical mechanism behind this electrical behavior, with the support of TCAD simulations.

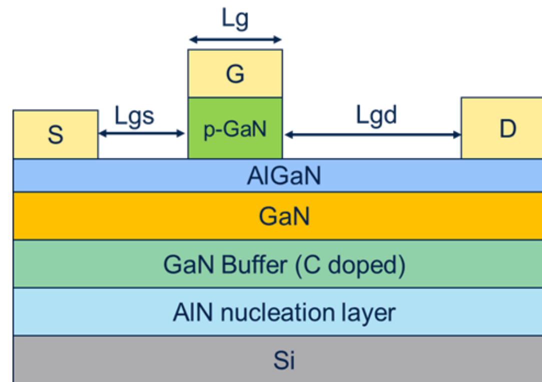


Figure 4.2: Schematic cross-section of the 650 V DUTs.

4.1.1 Experimental results and physical interpretation

Before starting the HTRB trial, all DUTs have been characterized in terms of linear transfer characteristics. Then, stress conditions for the DUTs are set-up with a temperature of 150 °C, drain-source bias voltage at 650 V and V_{GS} = 0V (Figure 4.3) and the drain leakage was monitored for 168 hours, as reported in Figure 4.4.

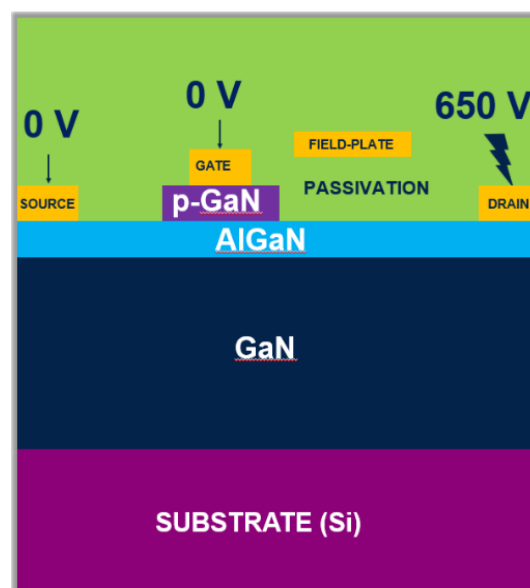


Figure 4.3: Schematic cross-section of the DUT with bias conditions for HTRB stress test.

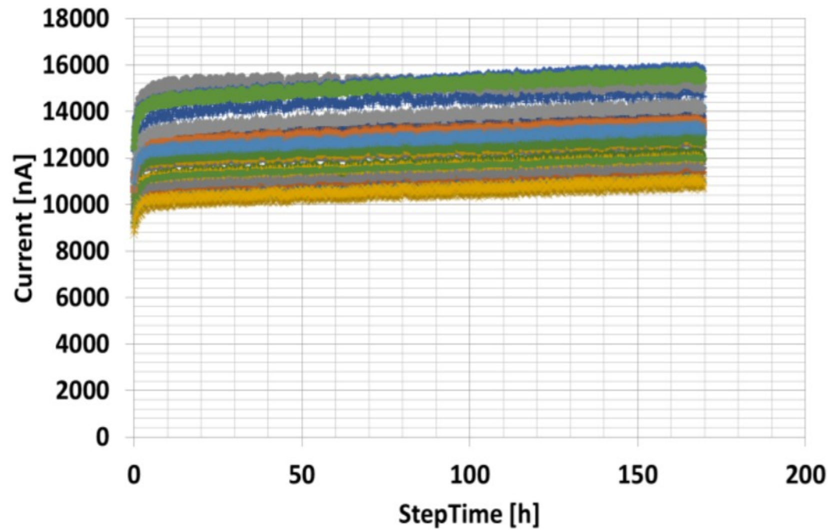
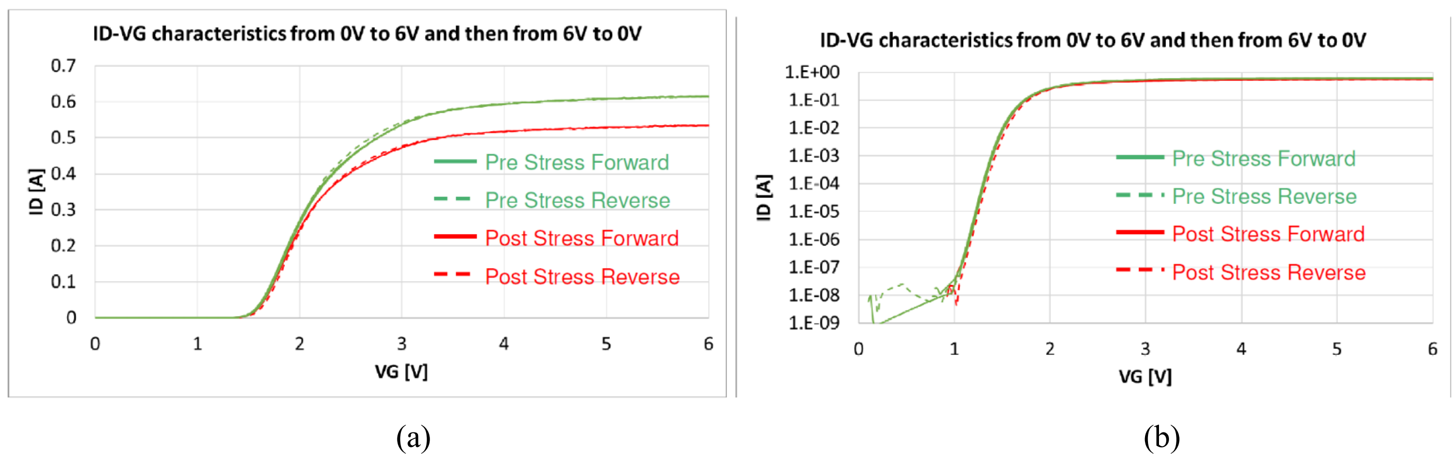


Figure 4.4: Drain leakage monitoring on DUTs during 168 hours of HTRB stress.

After the end of stress test, all the samples have been characterized again in terms of linear transfer characteristics, with the objective of performing a drift analysis on V_{TH} and R_{ON}. The analysis has shown that all samples shared the same degradation: in fact, a drain current decrease has been observed (corresponding to R_{on} increase of about 15%) with no threshold voltage (V_{TH}) shift and no recorded hysteresis variation (between forward curve and reverse curve, see Figure 4.5).



(a) (b)

Figure 4.5: Example of linear IV (V_{DS} = 0.5 V) characteristics evaluated before and after HTRB stress on DUTs in (a) linear scale and (b) semi-log scale.

4.1.2 TCAD simulations and results

To find out a possible physical explanation of this electrical behavior, TCAD simulations have been performed. In particular, Silvaco tools have been used (ATHENA and ATLAS). As first step, the physical HEMT structure has been reproduced in simulation through ATHENA. Then, a calibration of the ATLAS models and parameters was performed in order to match the experimental DUT characteristics. As in previous chapters, material parameters were set from

the default values of the simulator library and the transport equations for the carriers were solved using the drift-diffusion model. Shockley–Read–Hall model, the high-field mobility model, and the Farahmand mobility model were also employed in the simulations. The spontaneous and piezoelectric polarization were instead modelled as fixed sheet charges at the interface of AlGaN/GaN and p-GaN/AlGaN, calibrated to match the experimental sheet resistance and threshold voltage. The Schottky gate contact was properly set by fixing the gate workfunction in order to obtain the matching with the experimental Schottky barrier of about 1 eV. Then, acceptor doping of the p-GaN region (magnesium-related) and of the GaN buffer (carbon-related) were properly calibrated for obtaining a correct modelling of the threshold, off-state and on-state parameters. As an example, Figure 4.6 reports the alignment between the simulated I_D-V_G curve and the experimental one (pre-stress characteristics).

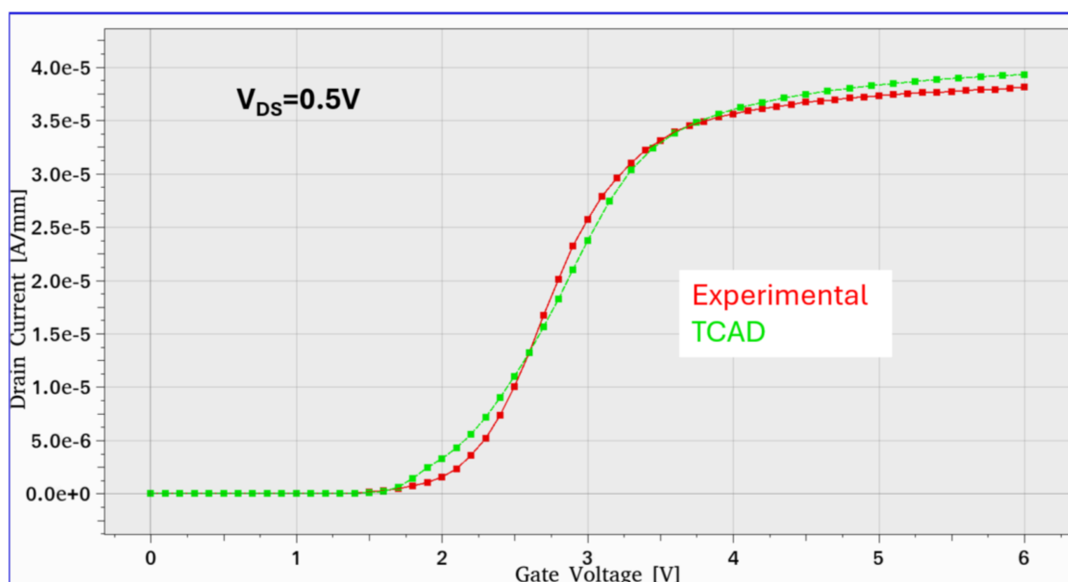


Figure 4.6: TCAD simulations results of linear IV characteristics compared to typical experimental data measured on DUTs.

Next, the electric field distribution has been investigated at V_{DS} = 650 V in off state condition, and four critical regions have been localized on the structure (Figure 4.7): one region corresponding to the gate edge, two regions corresponding to the source field plates and one last region close to the drain edge. These high-field regions could be linked to weak spots where charges (e.g., injected by field-plates during the stress) remain trapped, thus depleting the 2DEG by electrostatic repulsion.

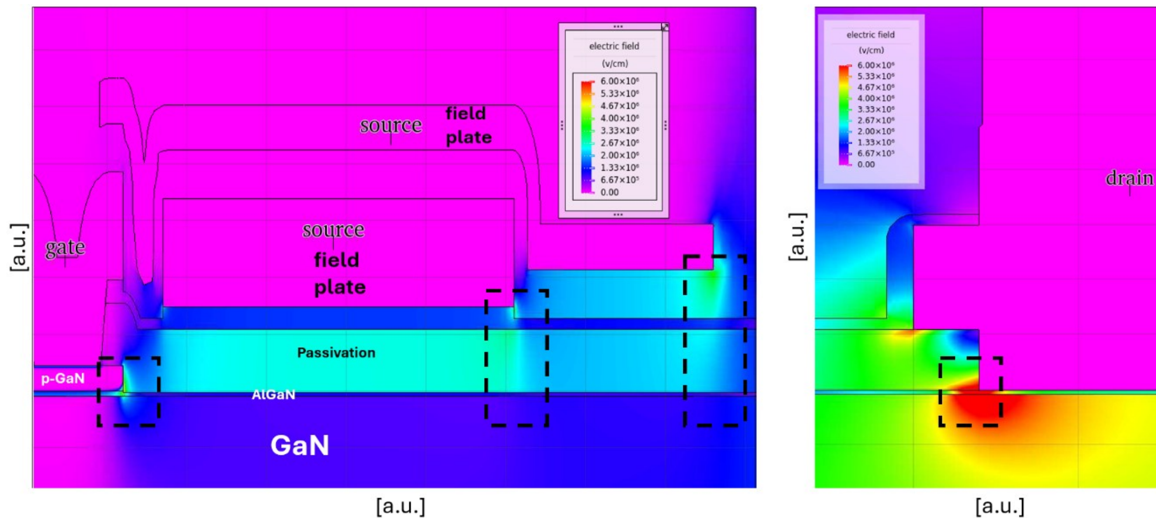


Figure 4.7: TCAD simulations of electric field along the gate-drain distance of the DUT, highlighting the high field regions at V_{DS} = 650 V.

In order to validate this hypothesis, further simulations have been run, each including additional negative fixed negative charges ($\approx -8 \cdot 10^{12} cm^{-2}$) at the passivation/AlGaN interface in each of the four different positions (regions 1, 2, 3 and 4) along the gate-drain region (Figure 4.8), where the electric field is higher. In this way, the effect of electron trapping in the four different regions could be easily simulated.

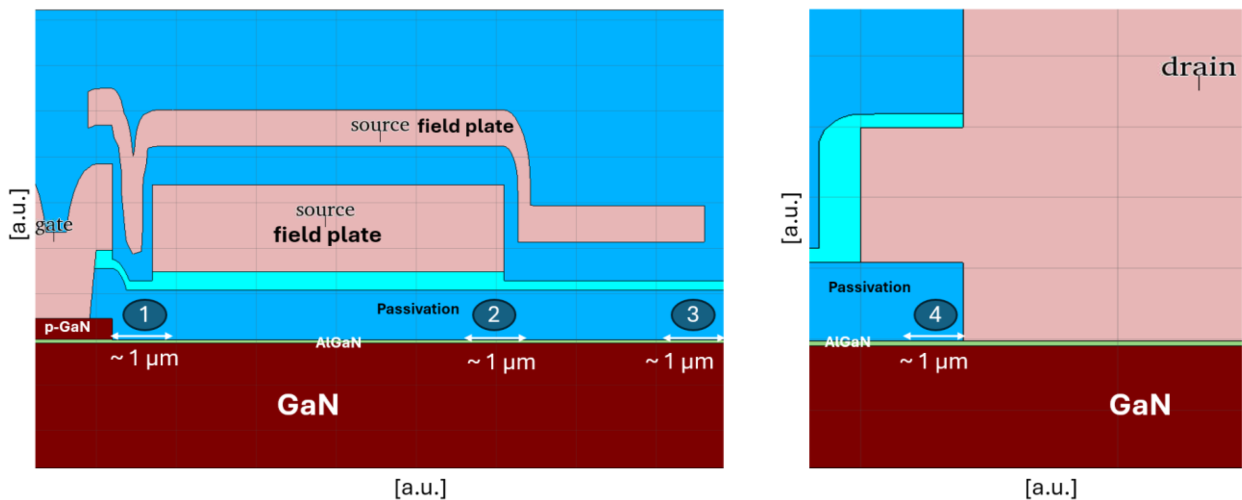


Figure 4.8: Cross-section of the DUT highlighting the four different regions where negative charges have been inserted for the TCAD DoE.

The results of the simulations, in terms of I_D-V_G curves, are reported in Figure 4.9, where it is shown that there is no V_{TH} shift nor significant I_D degradation with charges close to p-GaN (region 1) while in the other three cases (region 2, 3 and 4), there is non-negligible I_D degradation (about 12%) without V_{TH} shift.

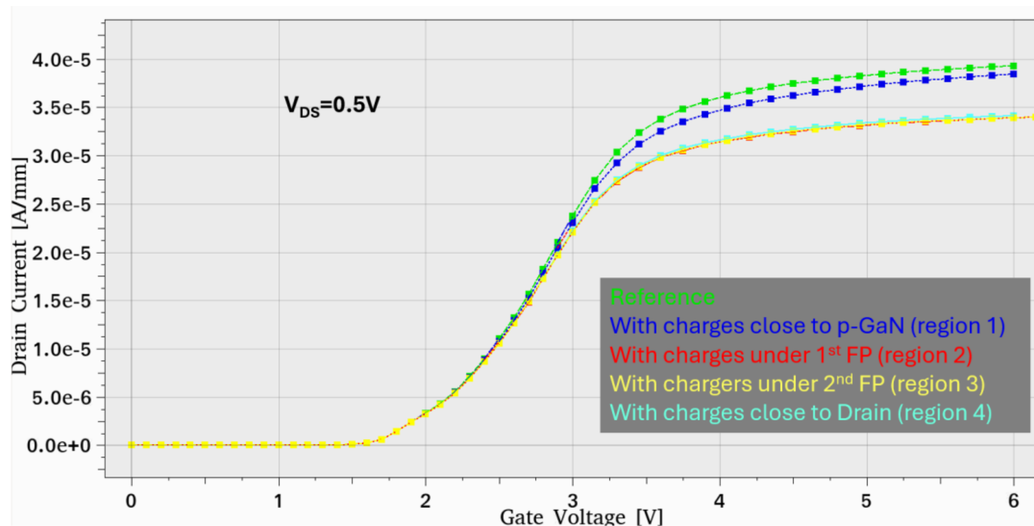


Figure 4.9: TCAD simulation results of linear IV characteristics comparing the reference case with the experiments where additional negative fixed charges were introduced at the passivation/AlGaN interface.

Stemming from these results, the following conclusion can be drawn: a degradation of Ron cannot be achieved if charges are trapped near the p-GaN gate, therefore the experimental behavior after HTRB stress can only be linked to negative charges trapped either under the field plates or close to the drain edge. However, since the highest electric field at 650 V is focused on the drain edge, it is most likely that the trapping happens in this region, assisted by non-idealities in the structure. In order to prove this, DUTs fabricated with a process variation related to a different chemistry for the ohmic cleaning have been tested through the same HTRB stress procedure presented before. In this case, the modification has resulted in a very good improvement in the performance (residual R_{on} drift below 5%, Figure 4.10), confirming the output of the TCAD simulations. However, it is worth noting that, in this case, a small degradation of the transconductance has been observed after HTRB (lower slope in the range between 2 V and 3 V of V_{GS}), suggesting residual trapping effects in the channel region (below the p-GaN).

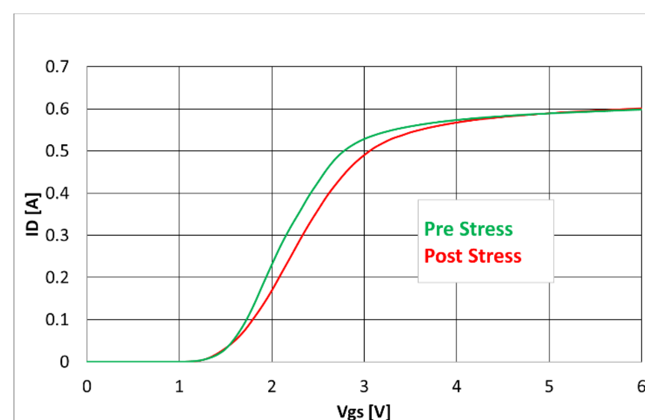
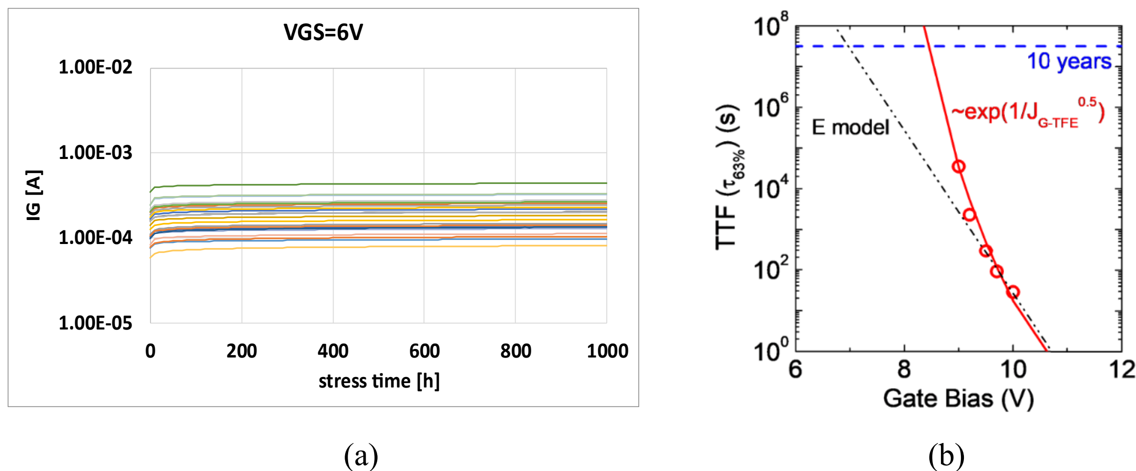


Figure 4.10: Typical linear IV (V_{DS} = 0.5 V) characteristics evaluated before and after HTRB stress on DUTs fabricated with improved ohmic cleaning.

4.2 Screening method for preliminary gate robustness assessment

Gate reliability is another very important aspect given the fact that gate of Schottky p-GaN HEMTs is typically driven at around +6 V with respect to the source terminal in order to obtain the optimal on-resistance and saturation current with limited gate leakage. In particular, when the transistor is continuously switched on, the forward gate bias applied to the device (i.e., +6 V) may induce gate leakage degradation and eventually failure. As for the drain terminal, also in this case, there are two main families of stress characterizations: Time-Dependent Gate Breakdown, TDGB, for lifetime prediction at maximum gate voltage rating (where the devices are stressed at very high gate bias up to failure, as shown in Figure 4.11) and High Temperature Gate Bias, HTGB, for endurance and drift analysis, again performed up to 500 or 1000 hours (where devices are stressed at their maximum gate voltage rating, verifying if any failures or significant degradations occur during or after the stress), as in the examples of Figure 4.11.



(a) (b)

Figure 4.11: (a) Typical gate leakage monitoring during HTGB stress performed on DUTs and (b) Typical lifetime prediction plot with TDGB time-to-failure data from [4].

Under moderately high positive gate bias, TCAD simulations show that the main stressed region, in terms of high electric field, is the gate metal corner interface with the p-GaN [5,6] but other sources of degradation, involving electron injection from the AlGaN barrier, may also play a role [7,8]. However, the time-to-failure dependence on the applied gate bias is not easy to determine since the acceleration factor can be modified by the specific physical gate leakage conduction mechanism involved at each different bias range (e.g., low V_{GS}, medium V_{GS}, high V_{GS}). This can lead to complex modeling through modified E-models or power laws [4,9], requiring many trials and a lot of time and effort with the final goal of achieving at least, e.g., 10 years of expected lifetime (which is a usual customer requirement). Following the indications of the international standards (AEC Q101 [10], JESD47 [11], JEP180 [12], etc.), it is found that the most common gate stress test is represented by the HTGB (high-temperature gate bias) characterization. This test is typically performed at nominal gate voltage (e.g., V_{GS} = 6 V) and a temperature of 150 °C for 500 h or 1000 h. Since all these stress tests are quite time-

consuming, they are usually performed in parallel on many packaged devices through dedicated equipment. Therefore, it could be useful to have an alternative method for an easier and faster on-wafer early screening of p-GaN HEMTs fabricated with different process flows.

With this objective, a novel accelerated gate stress procedure, able to give a first idea of gate robustness, was developed and it was then applied to evaluate different p-GaN devices.

4.2.1 DUTs and stress test description

Devices Under Test (DUTs) are 650 V-rated p-GaN HEMTs for power applications, with Mg-doping in p-GaN approximately 1×10^{19} cm^{-3} and p-GaN thickness in the range of 60–120 nm, grown on a p-type low-resistive Si substrate using a metal organic–chemical vapor deposition (MOCVD) system. The schematic cross-section of a typical DUT is depicted in Figure 4.12, with an indication of the main lateral dimensions. Devices analyzed in the following are characterized by a large active area (a few mm^2), which makes it easier to spot possible failures within a reduced stress time window [13,14].

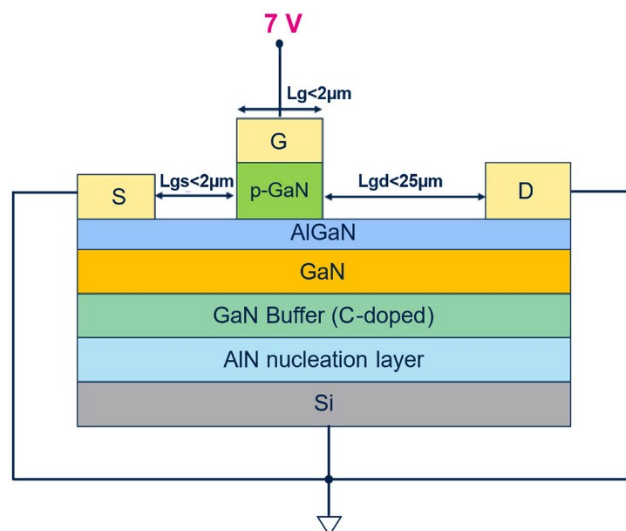


Figure 4.12: Schematic structure of tested AlGaN/GaN HEMTs with bias conditions for accelerated gate stress.

The bias conditions for the proposed stress test are reported directly in Figure 4.12, where it is shown that all the terminals of the device are grounded except for the gate, which is biased at a constant voltage, similarly to what happens in the case of HTGB. However, in this case, the idea is to apply +7 V on the gate terminal for a total stress time of 10,000 s at room temperature (25 °C). This 10,000 s stress duration has been chosen as an acceptable trade-off between a minimum reasonable observability time for potential stress-induced gate failures and the repeatability of the stress procedure for a considerable number of devices. In fact, in order to acquire meaningful statistical data, 24 devices per wafer have been stressed in the above-described conditions.

The bias conditions have been experimentally applied on several devices directly on the wafer, through a B1505A parameter analyzer [15] and a probe system [16], illustrated in Figure 4.13.

(**a**) (**b**)

Figure 4.13: (a) B1505A parameter analyzer; (b) Probe system for on-wafer measurements.

During the proposed room-temperature gate bias ("RTGB") stress test, the gate leakage is probed every 10 s in order to monitor the device behavior during the stress sequence. Moreover, transfer characteristics, leakage measurements before and after gate stress have been performed in order to monitor possible drifts on the main relevant parameters (e.g., threshold voltage, gate and drain leakage). The test sequence applied to each DUT is listed below (the entire sequence is performed at a temperature of 25 °C):

- Pre-stress transfer characteristic
- Pre-stress gate leakage
- Pre-stress drain leakage
- RTGB ($V_{GS} = V_{GD} = 7$ V, duration = 10^4 s)
- Post-stress transfer characteristic
- Post-stress gate leakage
- Post-stress drain leakage.

It is important to underline that these stress conditions have been chosen such that an accelerated p-GaN degradation can be induced on the DUTs. In particular (i) +7 V is a more challenging condition than the nominal operating voltage (+6 V) but at the same time it is not too far, hence a similar gate conduction mechanism can be assumed, and (ii) 25 °C is usually a more stressful temperature than 150 °C, given the negative temperature acceleration factor (AF) of p-GaN failures under positive gate bias stress [17], which is generally linked to the fact that, for example, avalanche breakdown phenomena (such as impact ionization) are penalized at higher temperature. While there can be other stress phenomena becoming increasingly significant at higher temperatures (like ion migration/diffusion, Frenkel defect formation, defect generation, or material degradation, etc.), the negative temperature AF has been confirmed for the DUTs through stress measurements at different temperatures (best results obtained at high temperature). Therefore, the chosen stress conditions can accelerate the degradation while also staying fairly close to the actual operating bias conditions. This condition reduces the risk of encountering additional physical degradation mechanisms occurring, e.g., at higher gate voltages and induced by strong hole injection [18,19], which can modify the lifetime and lead to results not easy to be

interpreted.

4.2.2 Experimental results and discussion

Then, the proposed accelerated gate stress test has been applied to three different families of DUTs, characterized by different processing of the p-GaN region. Starting with a reference process, two improved solutions have been then analyzed in terms of gate pre-reliability and DC performance.

a) Reference Process

DUTs fabricated with a reference process have been characterized in DC (Figure 4.14) and then stressed with the RTGB stress to evaluate their endurance.

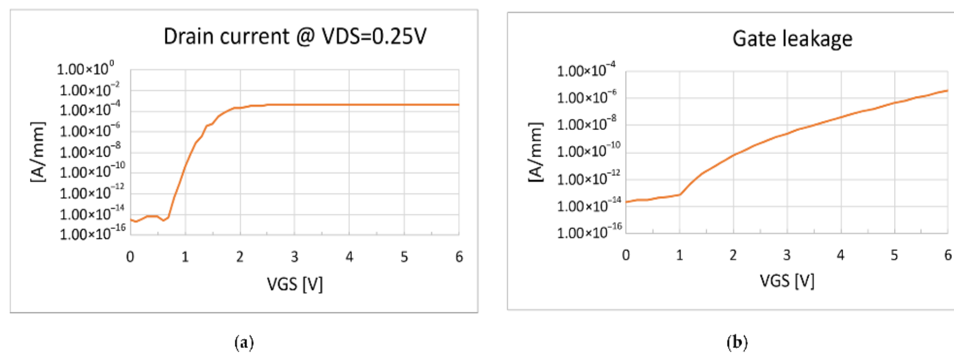


Figure 4.14: (**a**) Typical linear IV characteristic and (**b**) typical gate leakage measured on reference DUTs.

A relevant gate leakage degradation was observed during the monitoring (Figure 4.15), with some devices showing a gradual worsening with stress time, (as observed, e.g., for percolation-driven phenomena [20,21]).

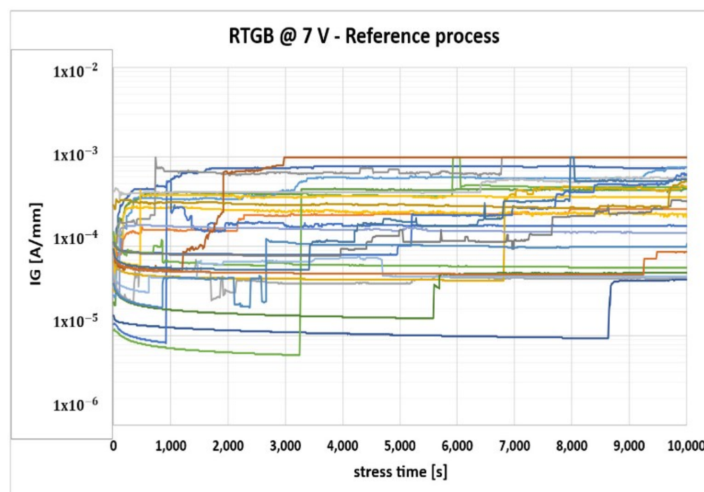


Figure 4.15: Gate leakage monitoring during RTGB stress test on reference DUTs.

The observed behavior during RTGB already suggests poor gate robustness in the case of a moderately large positive voltage; thus, there is no need to perform additional gate reliability tests, like HTGB, on packaged samples, because it is certain that devices would not pass those stress tests. Therefore, this technique can strongly reduce the time required for the evaluation of a process change (at least when results are as bad as shown in Figure 4.15).

b) Interdielectric Process

In order to mitigate the gate leakage degradation, a variation in the process flow, consisting of ex situ Atomic Layer Deposition (ALD) of a dielectric interlayer (namely Al_2O_3) of about 0.5–5 nm between p-GaN and gate metal, was proposed and implemented, as shown in Figure 4.16. Indeed, the introduction of this interdielectric layer can improve the insulation of the gate and have a passivation effect on the p-GaN surface, obtaining an MIS (metal–insulator–semiconductor) stack instead of the Schottky interface.

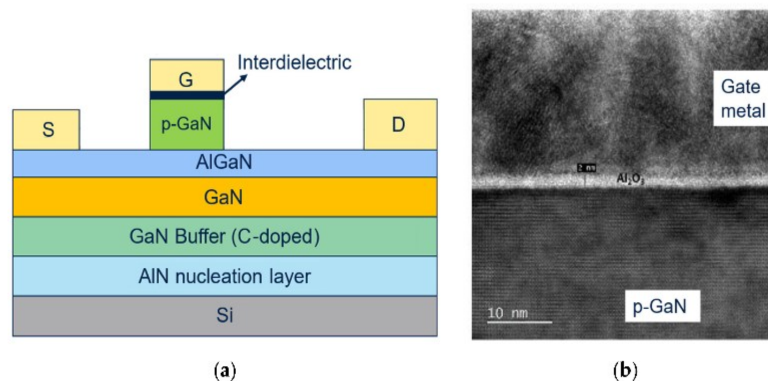


Figure 4.16: (a) Schematic cross-section and (b) TEM image of the interdielectric process.

DC characterizations of devices with such modification have been performed and the results are shown in Figure 4.17, where the reference devices are compared to devices processed with the interdielectric approach.

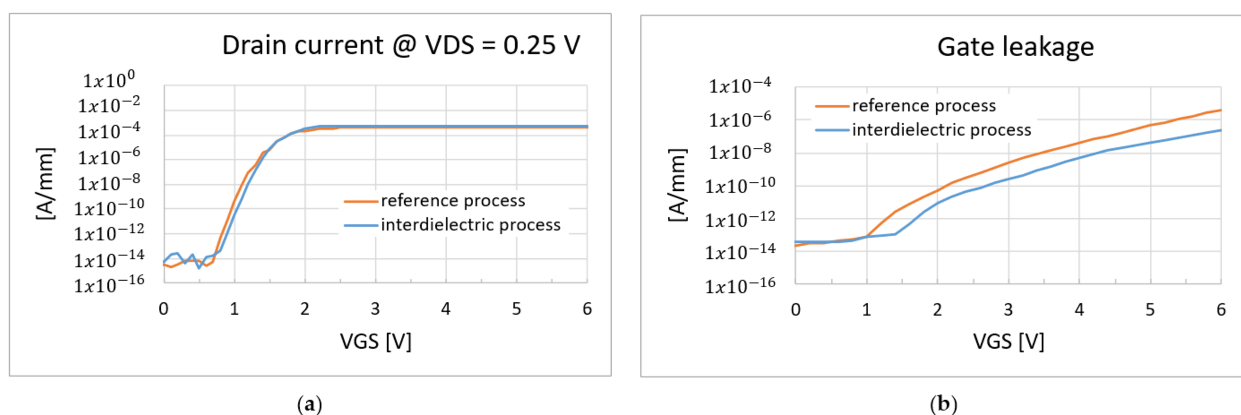


Figure 4.17: (a) Typical linear IV characteristic and (b) typical gate leakage measured on DUTs fabricated with interdielectric process compared to reference DUTs.

The comparison of the DC characteristics reported above shows no significant variations between the two different gate implementations, apart from a small reduction of the gate leakage in the case of the interdielectric approach. More importantly, the introduction of the interdielectric layer led to a stronger gate region, as shown from the gate leakage monitoring of all the tested devices under RTGB stress (Figure 4.18): no failures were observed during the time window of the measurements.

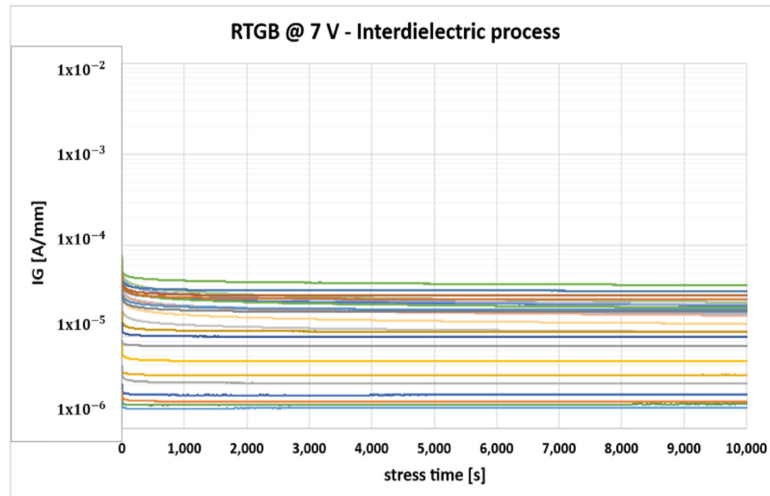


Figure 4.18: Gate leakage monitoring during RTGB stress test on DUTs fabricated with interdielectric process.

Nevertheless, even if the threshold voltage showed no significant variation, it was observed that the introduction of the interdielectric layer led to an increase in the drain leakage current, as shown in Figure 4.19, due to a worse control of the electrostatic potential under the p-GaN region ("channel potential"). This phenomenon was better analyzed through TCAD simulations, detailed in the following.

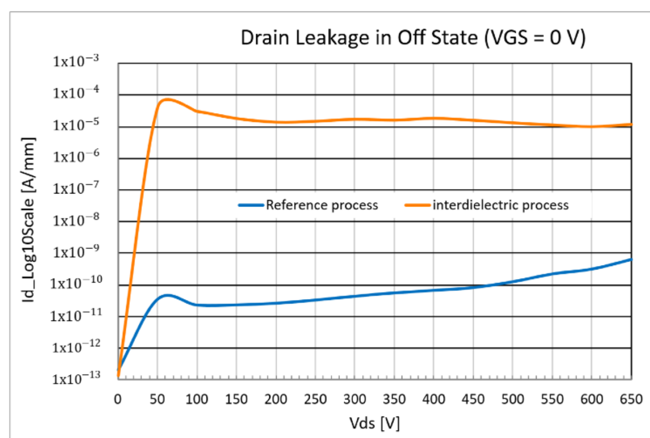


Figure 4.19: Drain leakage measurement comparison between reference process and interdielectric process.

TCAD simulations using Synopsys tools were carried out to investigate the physical behavior near the p-GaN gate region. The p-GaN HEMT structure was reproduced through Sentaurus Process, while the device simulation was performed thanks to Sentaurus Device [22], including physical models for GaN-based devices. Also in this case, material parameters were set to the default values of the simulator and drift-diffusion model was used for solving transport equations. All the other parameters and models were calibrated as in the previous section but in this case critical attention was given to the gate module definition. In particular, in order to simulate the interdielectric process, an Al_2O_3 layer (either 0.5 nm or 5 nnm thick) with 8.8 eV energy bandgap was introduced between the p-GaN and the gate metal. Moreover, Fermi-level pinning and additional gate tunnelling models (nonlocal path and direct tunnelling) were considered. Then, DUT was simulated in off state for matching the behavior of the simulated drain leakage with the experimental one and the results are shown in Figure 4.20.

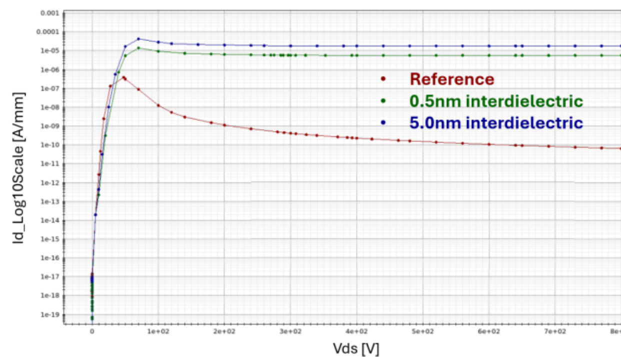
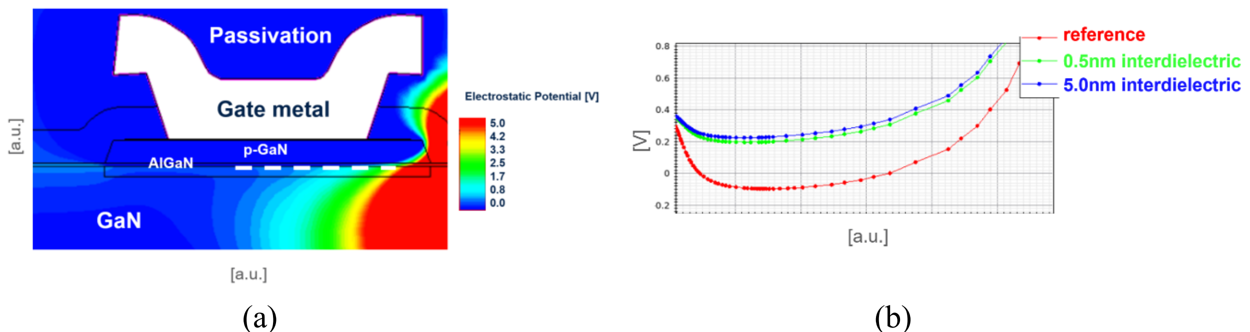


Figure 4.20: TCAD simulated drain leakage of the reference process compared to the interdielectric process.

As following step, the 2D potential distribution was evaluated at V_{GS} = 0 V and V_{DS} = 650 V. As reported in Figure 4.21, the potential under the p-GaN region, at the drain-side (on the right of the gate), was found to be higher in the case of an interdielectric between p-GaN and gate metal: this results in a lower energy barrier (between source and drain) for the electrons.



(a) (b)

Figure 4.21: (a) TCAD simulation of the 2D potential distribution close to the p-GaN region at zero gate bias and V_{DS} = 650 V for the 5 nm interdielectric case and (b) horizontal cutline along AlGaN (white dotted line) of the TCAD simulated potential for reference and interdielectric cases.

This phenomenon can be explained by the fact that the dielectric layer introduces an insulating barrier between the gate metal and p-GaN, thus producing a redistribution of the electric field, given the new boundary conditions. However, at low drain-source bias, the electric field is limited and, therefore, the dielectric layer presence does not significantly perturb the electrostatic potential yet. Instead, at higher bias, the electric field at the drain edge of the p-GaN/AlGaN interface becomes high, and the local distortion of the potential distribution is enough to facilitate an unwanted leakage path. Therefore, this modification of the electrostatic potential is the root cause of the parasitic electron current path formed between the source and drain, even with zero gate bias (Figure 4.22). Moreover, this condition cannot be easily mitigated by the addition of field plates, as shown in Figure 4.23. This novel result gives further understanding of the p-GaN gate module and of the metal/p-GaN interface, specifically, highlighting the importance of avoiding any dielectric residuals at this critical interface.

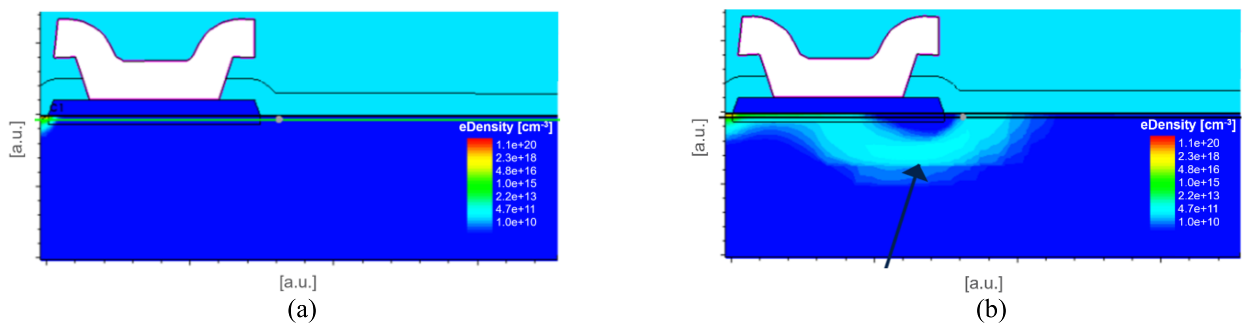


Figure 4.22: TCAD simulations of 2D electron concentration at zero gate bias and V_{DS} = 650 V in the case of (a) reference process and (b) interdielectric process.

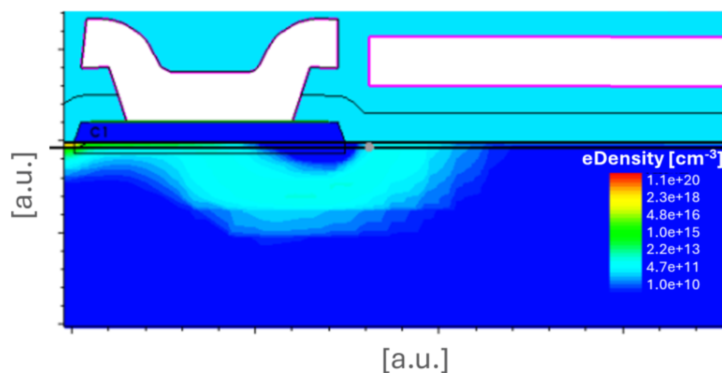


Figure 4.23: TCAD simulations of 2D electron concentration at zero gate bias and V_{DS} = 650 V in the case of interdielectric process with field plate addition.

c) Surface Treatment

The third option was proposed with the objective of improving gate robustness without the limitations observed in the interdielectric process. In this case, starting from the reference process, a different process modification was applied. In particular, an extra step of p-GaN surface

treatment was performed during the process flow (Figure 4.24). In particular, this process consists of a dry treatment performed at room temperature where the p-GaN surface is exposed to ozone (O_3), in order to obtain a cleaner and passivated surface and improve the interface quality, which is critical for enhancing long-term reliability.

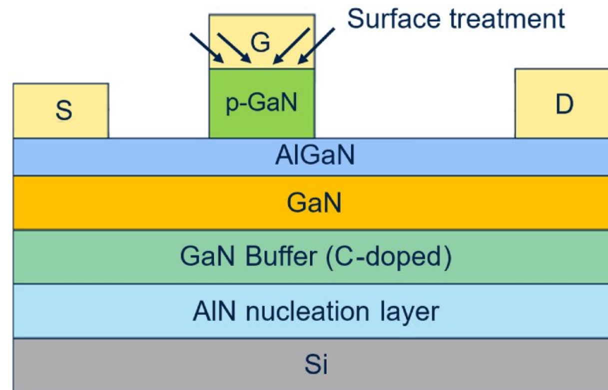


Figure 4.24: Cross-section of the DUTs fabricated with improved surface treatment on p-GaN.

As in the previous cases, a small DC characterization was performed on the devices, and the results (compared to the reference process) are reported in Figure 4.25.

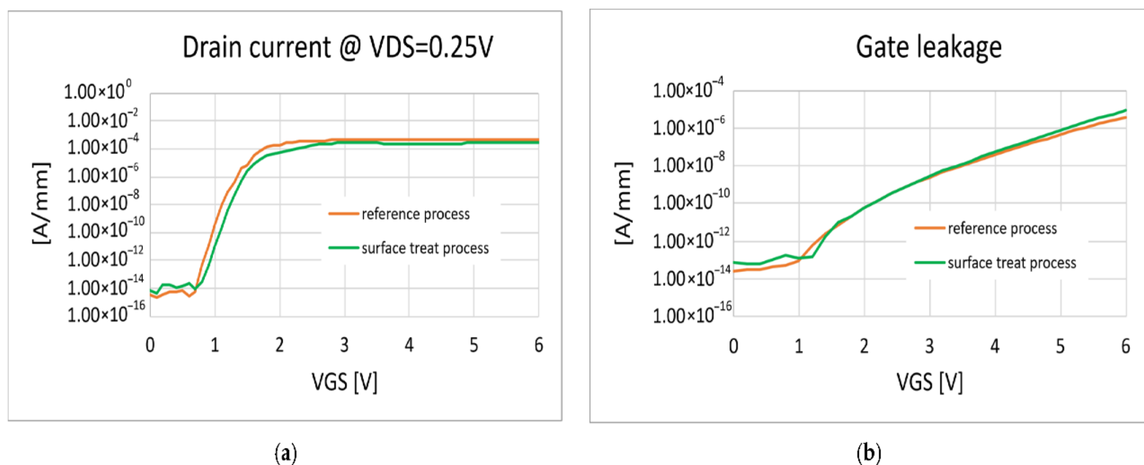


Figure 4.25: (a) Typical linear IV characteristic and (b) typical gate leakage measured on DUTs fabricated with surface treatment process compared to reference DUTs.

Then, the RTGB stress test was performed on the DUTs fabricated with said process, and the results are shown in Figure 4.26.

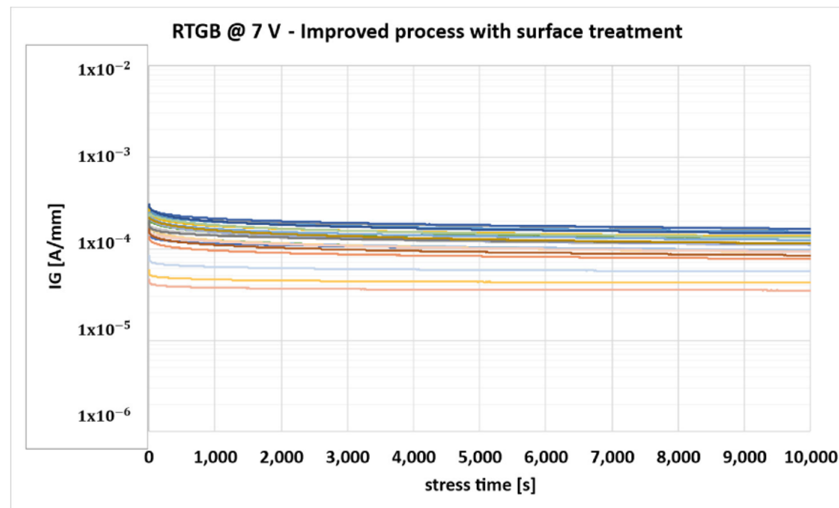


Figure 4.26: Gate leakage monitoring during RTGB stress test on DUTs fabricated with surface treatment process.

As in the previous case, all the tested devices showed no degradation of the gate leakage during the stress phase. However, for this improved process, low drain leakage was maintained up to high V_{DS}, with no increase or worsening with respect to the reference process (Figure 4.27), given the fact that the electric field in the gate stack was not modified by the surface treatment.

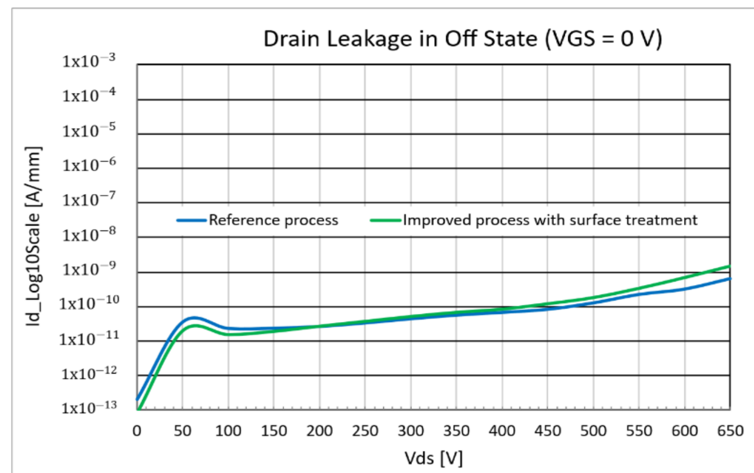


Figure 4.27: Drain leakage measurement comparison between reference process and surface treatment process.

In this case, given the good gate reliability and drain leakage results, a drift analysis on the main DC parameters was performed to further check the stability after the gate stress (Figure 4.28). As can be seen, no significant degradation was observed both for on-state (on-resistance, gate leakage) and off-state (drain leakage) parameters, while the threshold voltage, V_{TH} (semi-on state parameter), was only slightly affected (small increase).

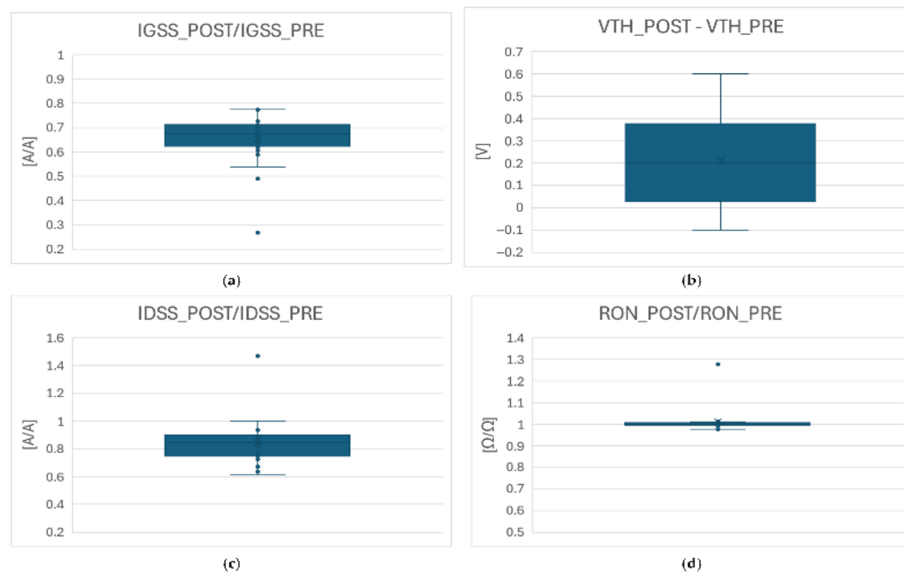


Figure 4.28: Boxplots with measured drift data evaluated after RTGB on DUTs fabricated with surface treatment process: (a) gate leakage drift at V_{GS} = 6 V; (b) threshold voltage shift; (c) drain leakage drift and (d) on-resistance degradation.

In conclusion, the proposed RTGB test was demonstrated to be very useful as gate screening technique and therefore could be used as a quick and useful tool for benchmarking different devices already at wafer level.

Moreover, it can be concluded that p-GaN surface treatment can be of paramount importance for the reliability improvement of the gate and must be carefully engineered to obtain the best results. Instead, the introduction of a dielectric layer between p-GaN and gate metal is a risky option, since it degrades the channel control at zero gate bias in the case of high drain-source voltage. However, since both solutions were able to improve preliminary gate reliability under positive gate bias stress conditions, it can be assumed that, in the reference process, the failure region was located mainly at the metal/p-GaN Schottky interface. This could be probably related to impurities or other contaminants present on the p-GaN surface (dedicated failure analyses would be needed to further investigate the root cause but they are out of the scope of this work).

4.3 Conclusions

In this Chapter, the static reliability of p-GaN HEMTs has been studied in detail both for the drain and the gate region. In the first part, the results from an HTRB test have been analyzed, highlighting an R_{ON} drift of the sample after the stress. With the help of TCAD simulations, this phenomenon has been deeply investigated, by inspecting all the possible regions leading to a 2DEG depletion. Simulations results have shown that only trapping under the field-plates or close to the drain can lead to the experimentally observed degradation. In particular, TCAD simulations have suggested that the most probable region where trapping happens is the one close to the drain, given the highest electric field. This hypothesis has been validated by HTRB

and drift analysis results on samples fabricated with an improved ohmic cleaning (acting directly on the drain region), which showed reduced R_{ON} degradation with respect to the reference process. Then, gate preliminary reliability of p-GaN HEMTs under positive gate bias has been studied through a room-temperature on-wafer accelerated stress test (RTGB), proposed to speed up the comparison of different gate module trials. Different gate processes have been presented and compared, highlighting the drawbacks and advantages of each approach. First, DUTs fabricated with a reference process have been tested, and the experimental characterizations have shown poor gate reliability behavior. Then, a first process variation including a dielectric layer between p-GaN and gate metal has been proposed for improved gate robustness. Devices with this process have been stressed, and the results have shown improved gate reliability performance, at the cost of a significantly increased drain leakage. This effect has also been examined through the help of TCAD simulations, which have shown how the potential distribution under the p-GaN region is negatively impacted by the introduction of a dielectric layer sandwiched between p-GaN and gate metal. Consequently, the drain leakage increases in this condition. An additional solution, consisting of an extra surface treatment step on the p-GaN, has been finally shown and described, underlying its good reliability performance under the considered stress conditions. This approach also allows good control of the channel region under the p-GaN, in terms of low drain leakage, up to elevated drain-source bias.

References - Chapter 4

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5 Bidirectional p-GaN HEMTs

In all the previous chapters, the focus was always on p-GaN HEMTs with a well-defined distinction between source and drain terminals. In fact, for a conventional planar p-GaN HEMT, drain contact must be physically more distant to the gate with respect to the source. This geometrical constraint is mandatory for high-voltage applications, where the gate-drain distance, together with the field-plates, is designed to sustain a specific maximum voltage rating, depending on the required application. On the other hand, it is useful to minimize the gate-source distance in order to obtain better driving of the transistor and a reduced on-resistance. This asymmetry between drain and source with respect to the gate can be referred to as “unidirectionality”: in other words, since power applications usually involves the switching between high and low voltage (off and on state), in all the previously analyzed power devices, the high voltage can be sustained only in one direction, i.e., at the drain side. However, some power applications (for example advanced converter topologies like T-type and matrix converters, OBCs, SSCBs, etc.), need bidirectional power switches, with high voltage / high current capability in both directions with respect to the gate (“bidirectional”). For example, in the case of matrix converters, the AC-AC power conversion is typically obtained with two different stages, AC-DC and DC-AC, usually involving bulky DC-link capacitors in the middle. Of course, the AC-DC-AC process involves efficiency reduction through each power conversion stage therefore, a direct AC-AC conversion would be the best solution. Figure 5.1 reports a typical sinusoidal AC signal: in order to obtain a conversion of this signal, an AC switch with bidirectional voltage capability is required in order to sustain high voltages from the positive peak sine value down to the negative peak sine value (the switch must alternate between on and off states, following the sine wave signal, which acts as the envelope of the voltage across the switch).

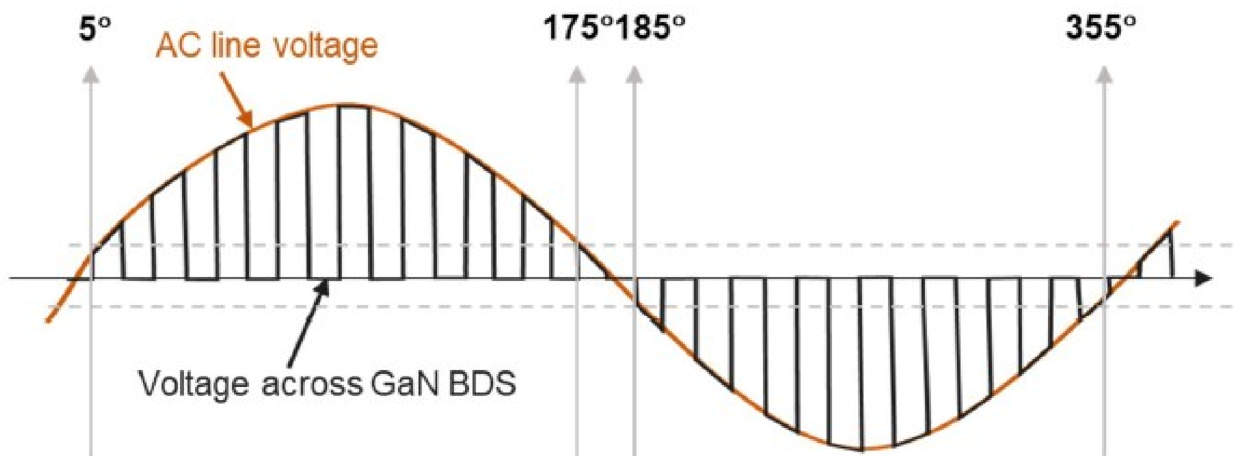


Figure 5.1: Example of a bipolar sinusoidal AC waveform to be handled by an AC switch [1].

This feature could be easily obtained, for instance, by an anti-series connection of two discrete p-GaN HEMTs with a common drain node (Figure 5.2): in this case, the source terminals of the two devices will alternatively act as an effective drain of the overall switch and

will sustain the high AC voltage.

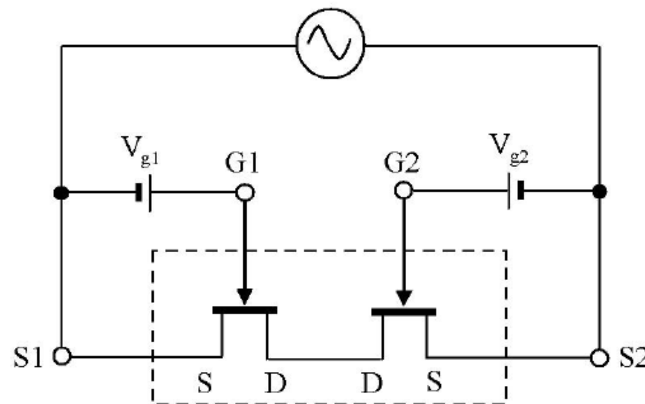
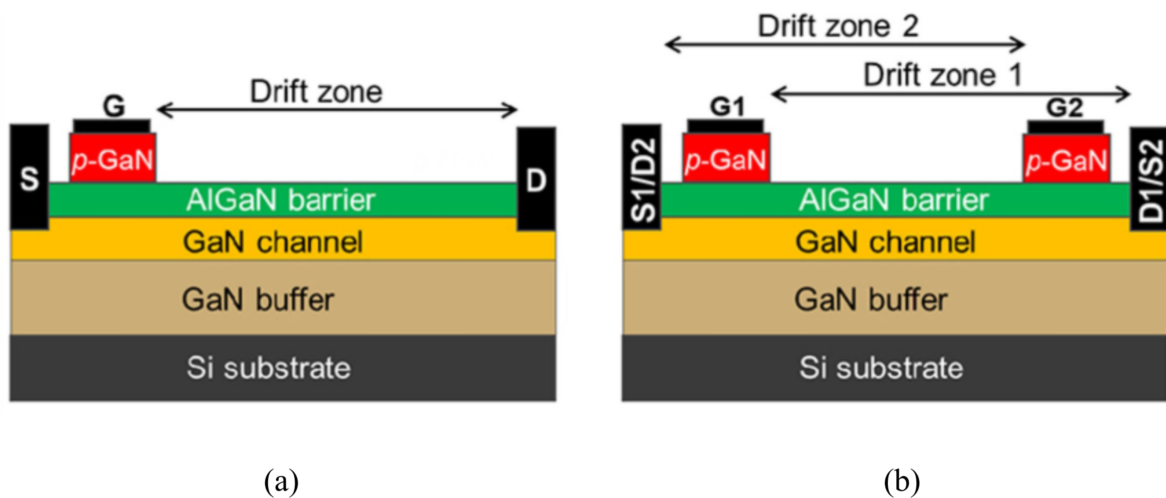


Figure 5.2: Bidirectional AC switch obtained through anti-series connection of two discrete unidirectional GaN HEMTs [2].

However, this implementation of a bidirectional switch including two discrete unidirectional GaN transistors connected in anti-series has the disadvantage of increasing the number of components (with increased parasitic inductances) and of worsening the conduction losses (equivalent on-resistance is doubled). Therefore, to reduce the on-resistance, the idea is to add two additional back-to-back transistors in parallel, but in that case, the area waste would be even higher. Thanks to the planar processing of GaN HEMTs, a monolithically integrated implementation of a bidirectional GaN HEMT, able to overcome all limitations of the discrete approach, can be realized. In particular, the most interesting solution is the dual-gate approach, where a second gate electrode is added close to the drain terminal, obtaining a symmetrical structure including two gates and two sources and a shared drift region in the middle. In particular, this chip structure (Figure 5.3) is obtained by a merging of two unidirectional p-GaN HEMTs sharing the same drift region, that can be used for bidirectional blocking high voltage during off-states.



(a) (b)

Figure 5.3: Schematic cross-section of (a) conventional unidirectional p-GaN HEMT and (b) monolithically-integrated bidirectional p-GaN HEMT [3].

Thus, the length of the shared drift region of the monolithic bidirectional device can be similar to the one of a single unidirectional GaN transistor with equivalent blocking voltage capability (Figure 5.3). Consequently, the on-state resistance of the monolithically integrated bidirectional GaN HEMT is significantly reduced in comparison to the solution where two or more discrete unidirectional GaN transistors are connected in anti-series. In fact, with this monolithic solution, the on-resistance of the bidirectional p-GaN HEMT can be approximately similar to the one of a single unidirectional GaN HEMT, with just limited increase. This is an important advantage with respect to what can be realized in other technologies, like Silicon or SiC, where the vertical approach to power MOSFET limits the bidirectional capability: in that case, a bidirectional switch can only be obtained by a back-to-back connection of two SiC devices resulting in an overall on-resistance and chip size increase. Instead, the monolithic implementation of a bidirectional GaN HEMT allows much lower conduction losses, a more compact solution, with reduced parasitic and identical driving as the solution with two separate unidirectional devices connected in anti-series. Given all these considerations and the fact that unidirectional GaN HEMTs have reached a good maturity level, it is not strange to see many recent papers about this topic [4-8], also proposing very high voltage solutions [9] and the expectation is that this interest will continue also for the next years. However, one of the main issues of the monolithic integration of bidirectional p-GaN HEMTs is the managing of the shared silicon substrate: in fact, in order to avoid malfunctioning and high dynamic R_{on}, the Si-substrate is usually shorted with source in the case of unidirectional p-GaN HEMTs. However, in the case of bidirectional p-GaN HEMTs there are two sources that alternatively act as effective source or effective drain of the overall device, depending on the voltage polarity, and therefore it is not obvious where to connect the substrate. As a consequence, bidirectional p-GaN HEMTs require dedicated substrate bias networks for the management of this issue, which otherwise would highly impact on the dynamic R_{on} [1,10]. The need for an additional bias network is something that increases the die size of the overall device, but it can be optimized by monolithically integrating the circuit together with the power HEMT. However, the details of this substrate issue and of the possible solutions will not be discussed in this thesis.

Given the fact that there are two gates in the device, four possible operation modes exist for bidirectional p-GaN HEMTs, depending on the combination of on and off state of the two gates.

GATE1	GATE2	Operation mode
OFF	OFF	Off state (both directions)
ON	ON	On state (both directions)
OFF	ON	Reverse conduction/blocking
ON	OFF	Reverse blocking/conduction

Table I: Operation modes of the monolithic bidirectional switch.

In the following sections, a study of the DC and AC characteristics of bidirectional p-GaN HEMTs in different operating conditions is presented through TCAD simulations and experimental characterizations. The results are then compared to a unidirectional device fabricated on the same wafer, sharing the same epitaxy and process. In particular, both unidirectional and bidirectional devices presented later (DUTs) are 650 V rated grown on a Si-substrate (111) in a MOCVD reactor. Both are enhancement-mode devices obtained with p-GaN gate, where the contact between gate metal and p-GaN is of Schottky type, with nominal gate voltage driving at +6 V. The pitch lateral dimension of the bidirectional DUTs is just +8% with respect to the unidirectional DUTs.

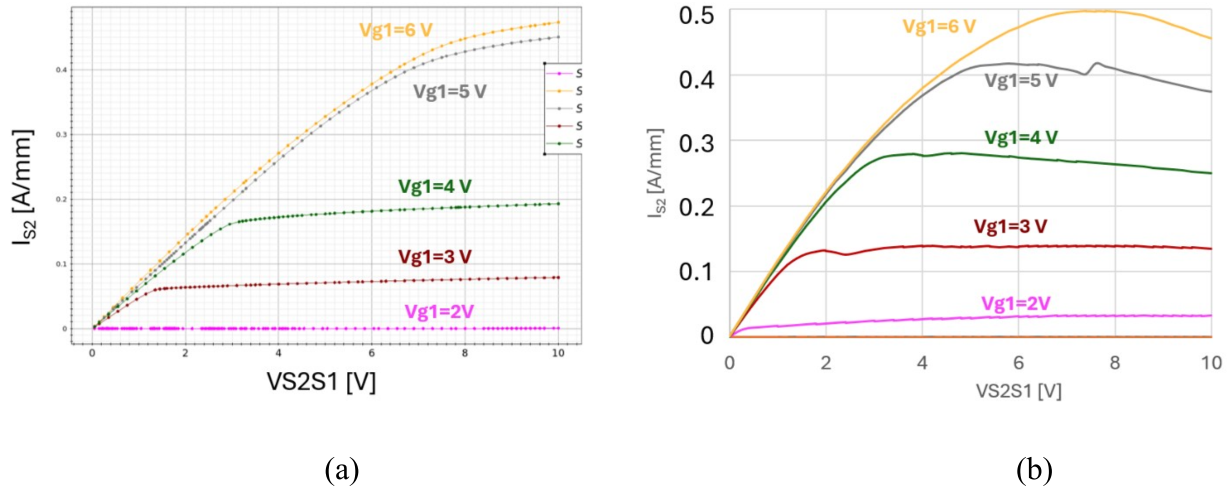
Other common implementations for bidirectional GaN HEMTs include variations like ohmic contact between gate metal and p-GaN (GIT bidirectional devices) or absence of p-GaN in the case of D-mode devices (cascaded solutions with silicon MOSFETs driving) but they will not be treated in this thesis.

5.1 DC simulation & characterization

As a first step, bidirectional GaN switches have been simulated in DC conditions in order to have a general idea of the device behavior. For the setup of the simulations, the same approach as in the previous chapter was used: material parameters set to the default simulator values, drift-diffusion model to solve transport equations, Shockley–Read–Hall model, high-field mobility model and Farahmand mobility model. Then, the calibration of the fixed charges emulating the spontaneous and piezoelectric polarization, of the Schottky contact and of the acceptor doping in p-GaN and GaN buffer was maintained like in the previous chapter since unidirectional DUTs analyzed in this chapter are fabricated through the same epitaxy/process recipe. Then, experimental measurements have been performed to check the actual behavior of the DUTs. The results coming from TCAD simulations and experimental characterizations have been grouped depending on the specific operating mode of the bidirectional and are presented in the following.

5.1.1 V_{GS1} = 0 V → 6 V & V_{GS2} = 6V or vice versa

At full on state, both gates are turned on (at nominal gate voltage) with respect to their source. To reach this condition starting from zero bias, either both gates are turning on at the same time or only one is sweeping while the other is already turned on. In this section, the first case will be analyzed as it results in IV behaviors more similar to the ones of a unidirectional device. In fact, starting from the output function (which in this case plots one of the two source currents vs source-to-source voltage), the TCAD simulation results already show a trend which is usually obtained in a unidirectional device. Of course, in the case of bidirectional devices, the first quadrant operation can be mirrored also in the third quadrant because of the symmetrical structure. Experimental results confirm the simulated trend and show a knee voltage of about 6 V for the bidirectional DUTs (Figure 5.4). From the output function, both the on-resistance and the saturation current can be extracted, as commonly done for unidirectional devices.



(a) (b)

Figure 5.4: Comparison between on-state output IV evaluated from (a) TCAD simulations and (b) experimental measurements on bidirectional DUTs with VGS2=6V.

Figure 5.5 shows the comparison of the measured R_{on} for the unidirectional and bidirectional device.

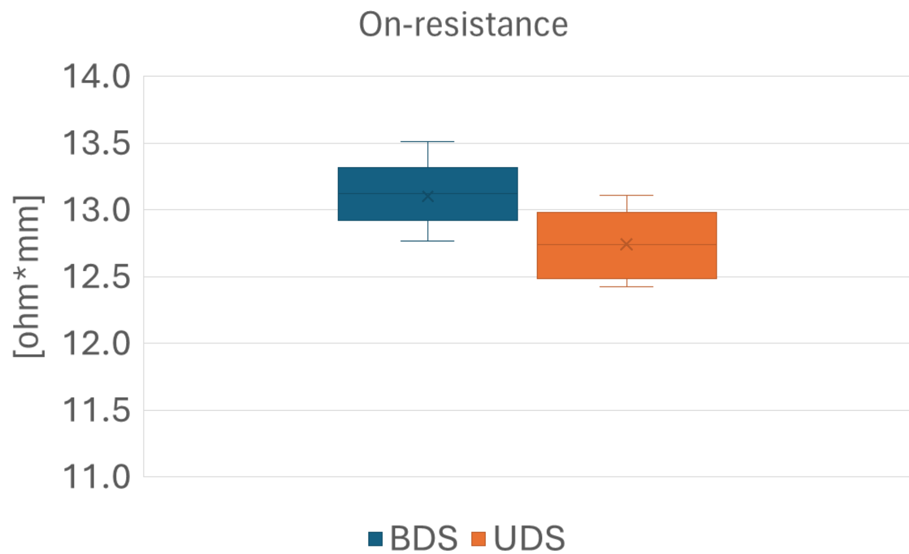


Figure 5.5: Comparison between on-resistance measured on bidirectional and unidirectional p-GaN HEMTs.

As can be seen, only a small worsening is present in the bidirectional case, thanks to the improved shrinking of the structure, made possible by the monolithically-integrated solution. In particular, by comparing the on-resistance of different bidirectional structures versus their gate-to-gate length, a correlation was made (Figure 5.6): this correlation is explained by the fact that the main contribution to the overall on-resistance of the bidirectional p-GaN is given by the 2DEG resistance of the shared drift region between the two gates. Therefore, by decreasing this distance,

the on-resistance can be optimized with no significant reduction of the source-to-source breakdown voltage, as shown later.

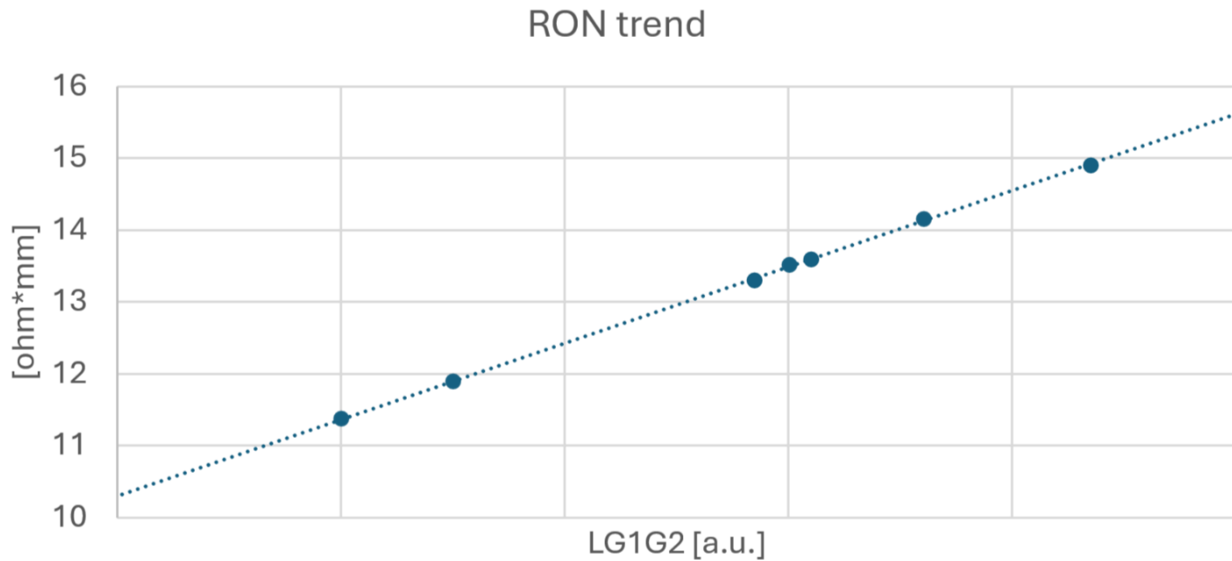


Figure 5.6: Bidirectional on-resistance trend with reduction of the gate1-gate2 distance reduction.

The breakdown voltage has been evaluated in off state for bidirectional devices with difference gate-to-gate length and the results show very good blocking voltage capability for all the distances taken into account (Figure 5.7), with all the structures sustaining voltages higher than 900 V. This observation shows that it is possible to obtain a good trade-off between the on-resistance and the breakdown voltage also for bidirectional p-GaN HEMTs.

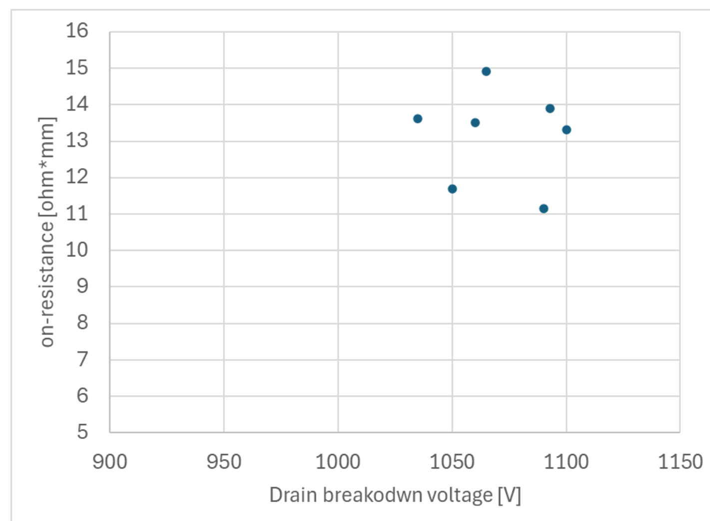


Figure 5.7: Bidirectional on-resistance versus drain breakdown voltage.

Of course, a possible trade-off between gate1-gate2 distance and dynamic R_{on} behavior could be present and has to be considered for the bidirectional structure optimization as well as the design of the field plates: however, these aspects are out of the scope of this work and will not be analyzed. Another useful characterization that gives additional information on the device, namely the threshold voltage, is the transfer characteristic, where the source-to-source voltage is fixed at low voltage (e.g., 0.5 V) and only one of the two gates is sweeping. In this case (Figure 5.8), it can be observed that there is (as expected) full symmetrical behavior of the two gates and that the threshold voltage is just above 1 V, as in the unidirectional device (no difference induced by the bidirectionality on the threshold level). Also from this characterization, the on-resistance can be extracted.

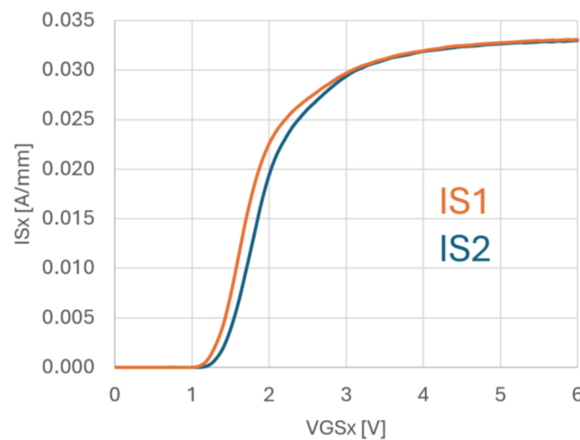


Figure 5.8: Linear IV transfer characteristic evaluated alternatively for gate1 and gate2.

Figure 5.9 shows the comparison of the measured V_{TH} for the unidirectional and bidirectional device extracted from the transfer characteristic.

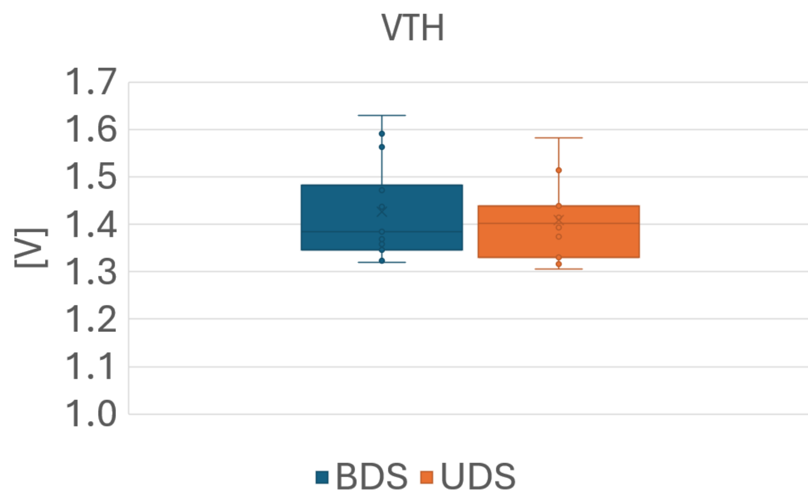
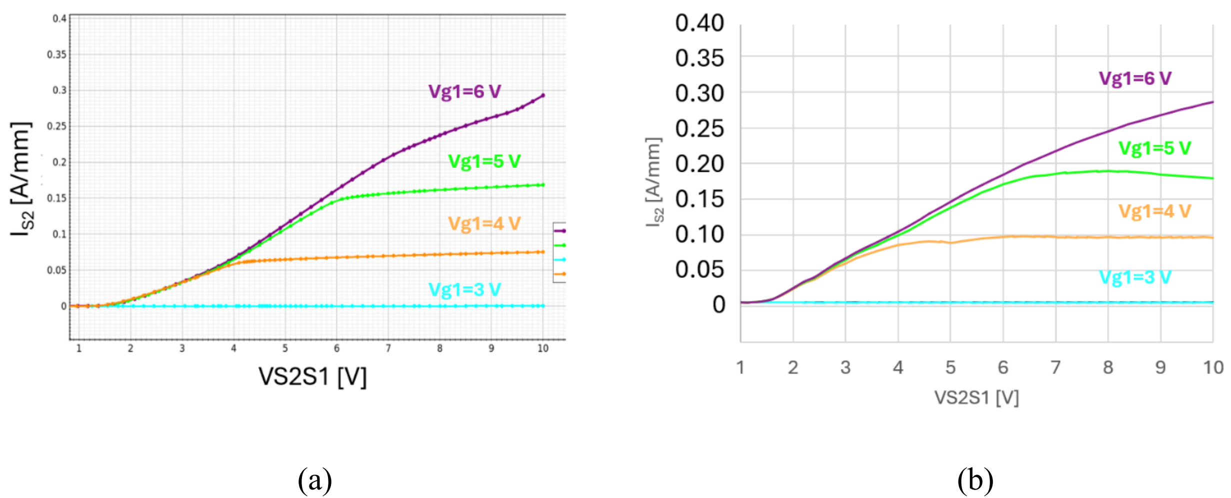


Figure 5.9: Comparison between threshold voltage measured on bidirectional and unidirectional p-GaN HEMTs.

5.1.2 $V_{GS1} = 0\ V \rightarrow 6\ V$ & $V_{GS2} = 0\ V$ or vice versa

As mentioned at the beginning, bidirectional devices feature also intermediate operation between on state and off state, where only one of the two gates is on while the other remains off. This condition is sometimes referred to as "diode-mode": actually, depending on the source-to-source voltage polarity it can be interpreted as a reverse conduction or reverse blocking from the point of view of the gate that is off while the other gate voltage is only modulating the current level. In this case, the current level starts to increase after that the source-to-source voltage overcomes the threshold voltage, just like what is happening for a unidirectional device under reverse conduction. Also in this case, TCAD simulations have been performed at first, in order to have an insight into the device behavior. Then, experimental results have confirmed the expected trend, and the results are summarized in Figure 5.10.



(a) (b)

Figure 5.10: Comparison between reverse conduction IV evaluated from (a) TCAD simulations and (b) experimental measurements on bidirectional DUTs.

Differently from the previous mode of operation, in this case third quadrant conduction does not mirror the first quadrant: of course, this asymmetry is the result of forcing the second gate to off state. In fact, for negative V_{S2S1}, the current conduction is only made by a leakage contribution (see in section 5.1.4).

5.1.3 $V_{GS1} = 0\ V \rightarrow 6\ V$ & $V_{GS2} = 0\ V \rightarrow 6\ V$

When fully turning the bidirectional device to on-state condition, the bidirectional device suffers a leakage coming from both gates. Therefore, it can be expected that when both gates are fully on (at nominal driving voltage), the overall leakage is doubled with respect to the one of a unidirectional device. Nonetheless, this is generally a limited concern, especially in Schottky-type p-GaN gates where the leakage is usually maintained quite low.

Figure 5.11 shows the gate leakage contributions of both gates when sweeping both of them from off state to nominal gate voltage. As expected, the two contributions are identical.

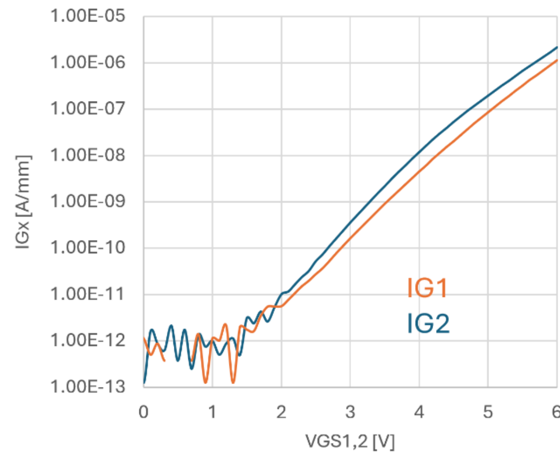


Figure 5.11: Gate leakage evaluation on both gate1 and gate2 while sweeping both gates together.

Figure 5.12 reports instead the overall gate leakage of the bidirectional p-GaN HEMT (obtained by summing the contributions of the two gates) compared to the unidirectional device. Of course, similar shape is obtained and only leakage level is different between the two devices.

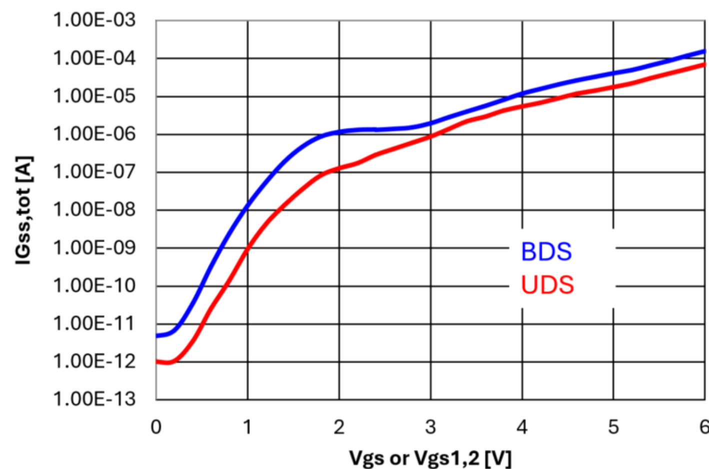


Figure 5.12: Total gate leakage comparison between bidirectional and unidirectional DUTs.

5.1.4 $V_{GS1} = 0$ V & $V_{GS2} = 0$ V or $V_{GS2} = 6$ V

For comparing the high voltage behavior of the bidirectional and the unidirectional DUTs, in both cases, the substrate bias has been forced to the one of the source terminals (i.e. the low-voltage source in the case of bidirectional). First, when both gate-source voltages of the bidirectional are below the threshold value, the bidirectional device is completely turned off and

has the capability of sustaining high voltage on both sides. Under this condition, there is a leakage concentrated at the high voltage source that is composed by source-to-source leakage, gate and substrate contributions (Figure 5.13).

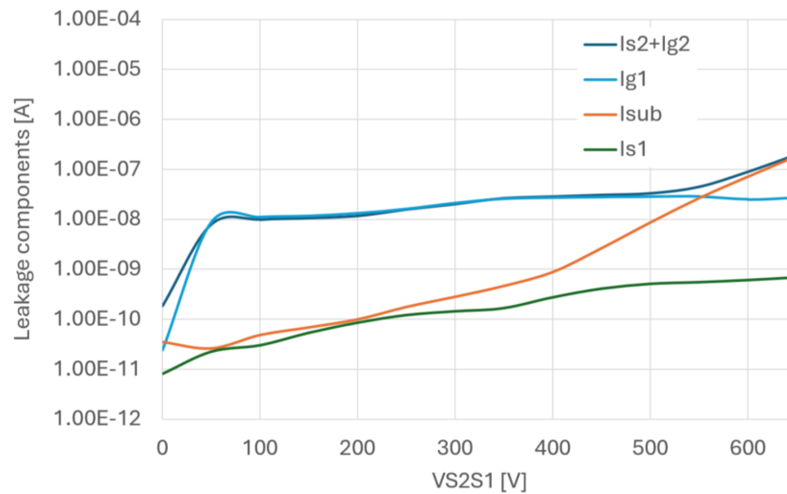


Figure 5.13: Leakage current contributions in off state measured on bidirectional DUTs.

The comparison with unidirectional device shows negligible difference in the off-state leakage, as expected for the structure. Figure 5.14 shows the comparison of off-state leakage contribution for unidirectional and bidirectional p-GaN HEMTs: negligible difference is observed between the two devices

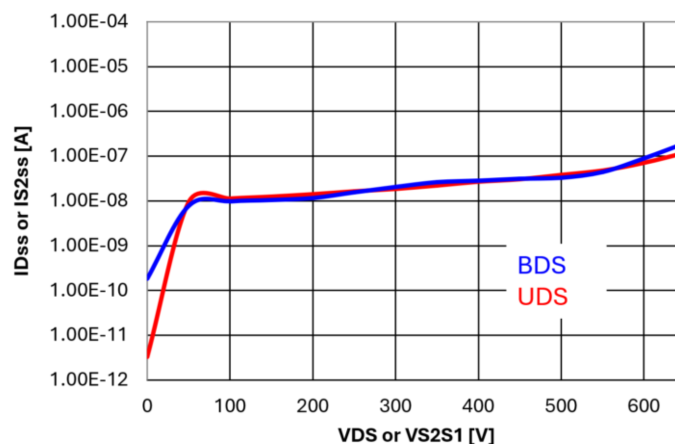


Figure 5.14: Off-state leakage measurements performed on bidirectional and unidirectional DUTs.

In the following, instead, one last mode of operation for the bidirectional is shown. In particular, when one of the two gates is off while the other is on and the source-to-source voltage is increased in the direction of the on-state gate, the bidirectional is in reverse blocking mode. In this case, the leakage is modified with respect to the full off state because one of the two gates is on: for what concerns the gate in on state, the leakage is dominated by the gate leakage flowing between gate and source, as shown in Figure 5.15.

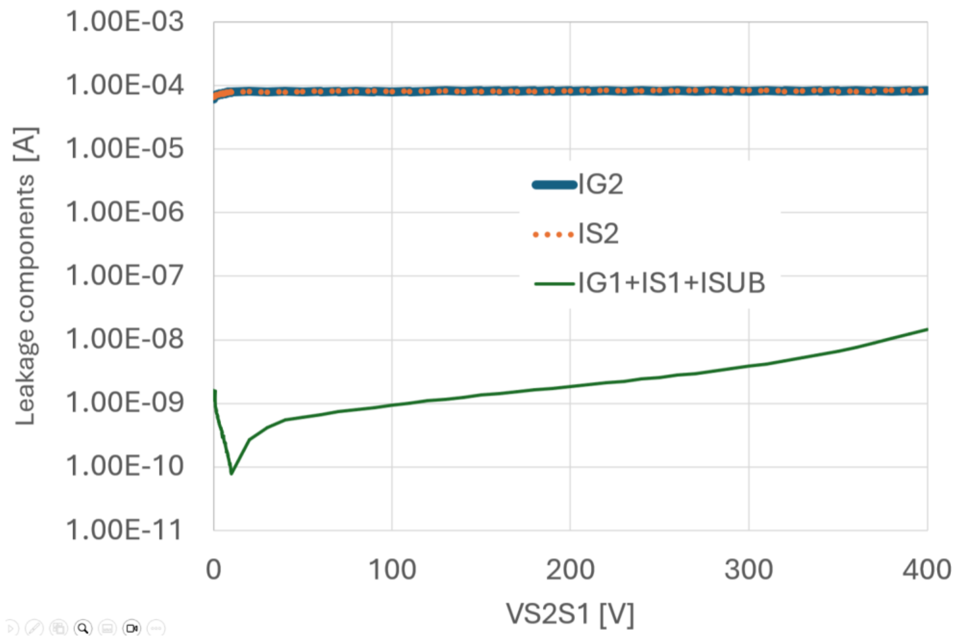


Figure 5.15: Reverse blocking leakage measurements performed on bidirectional DUTs.

5.2 AC simulation & characterization

In order to obtain information about the intrinsic reactive contributions of the bidirectional DUTs, an AC evaluation has to be performed. In particular, for measuring the capacitances, CV characterizations must be performed with no relevant current conduction on the device, i.e. when only negligible leakage is flowing, otherwise the result of the measurements would be distorted and unreliable. Thus, aimed at this characterization, three main regions of operations will be explored: a) both gates off and sweeping source-to-source voltage (off state); b) main gate is off, secondary gate is on, sweeping source-to-source voltage (reverse blocking), c) zero source-to-source voltage and sweeping gate voltages. In particular, the comparison of the first two regions will be quite informative regarding the full understanding of the bidirectional behavior, and it will be particularly helpful in the comparison with the unidirectional results.

All the measurements have been performed through a B1505A parameter analyzer interfaced to the on-wafer DUTs through a Microtech Cascade Probe System. Moreover, a custom circuit for the direct extraction of the input, output and reverse capacitance (C_{ISS}, C_{OSS}, C_{RSS}) has been exploited. Instead, for the gate capacitance measurement, the B1505A was directly connected to

the DUTs without additional circuitry in the middle (Figure 5.16).

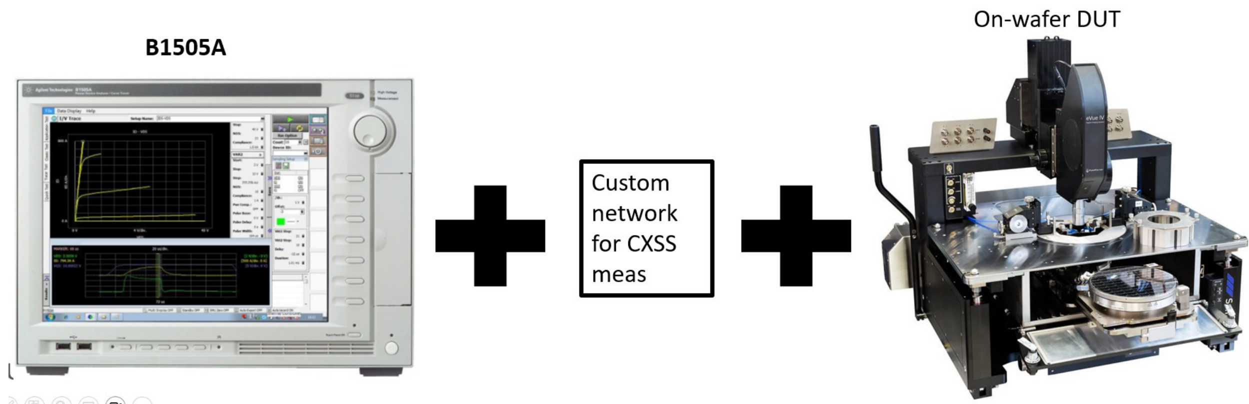


Figure 5.16: Test setup used for the capacitance measurements on bidirectional DUTs.

Also in this case, TCAD simulations are presented in comparison with experimental measurements and as tool for understanding the underlying physic behavior leading the observed phenomena.

5.2.1 C_{ISS}, C_{OSS}, C_{RSS} - $V_{GS1} = 0$ V & $V_{GS2} = 0$ V

This first condition is characterized by both gates of the bidirectional device in off state. As reported later, the TCAD simulated data of C_{ISS}, C_{OSS} and C_{RSS} are in good agreement with the experimental measurements performed on DUTs (Figure 5.17-5.19). The gap between TCAD and experimental observed in the C_{ISS} case has been attributed to non-idealities of the measured structure (pad contribution that is not taken into account in the TCAD structure).

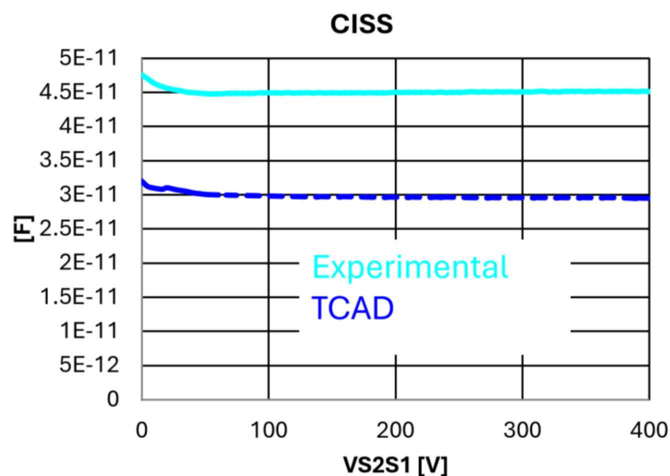


Figure 5.17: Input capacitance on bidirectional DUTs compared between measurements and TCAD simulations.

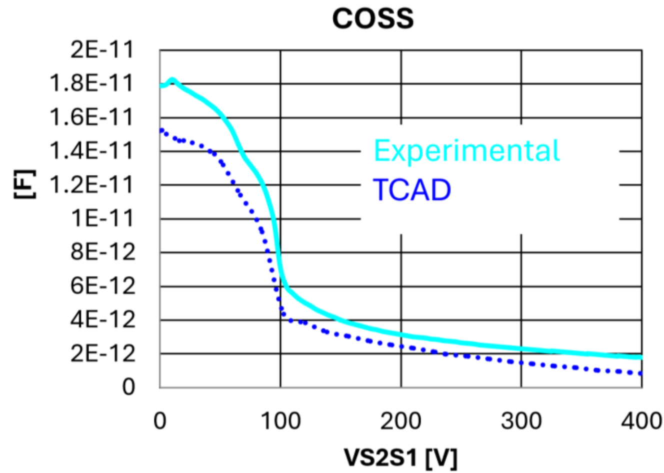


Figure 5.18: Output capacitance on bidirectional DUTs compared between measurements and TCAD simulations.

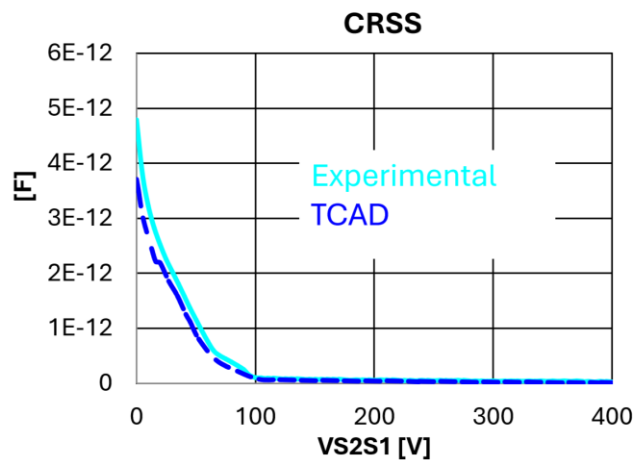


Figure 5.19: Reverse capacitance on bidirectional DUTs compared between measurements and TCAD simulations.

By comparing the results obtained on the bidirectional DUTs with the ones obtained for the unidirectional, it can be seen that there are some differences. In fact, the two types of devices differ at low voltage (within 100 V) while at high voltage, the curves are pretty much aligned (Figure 5.20).

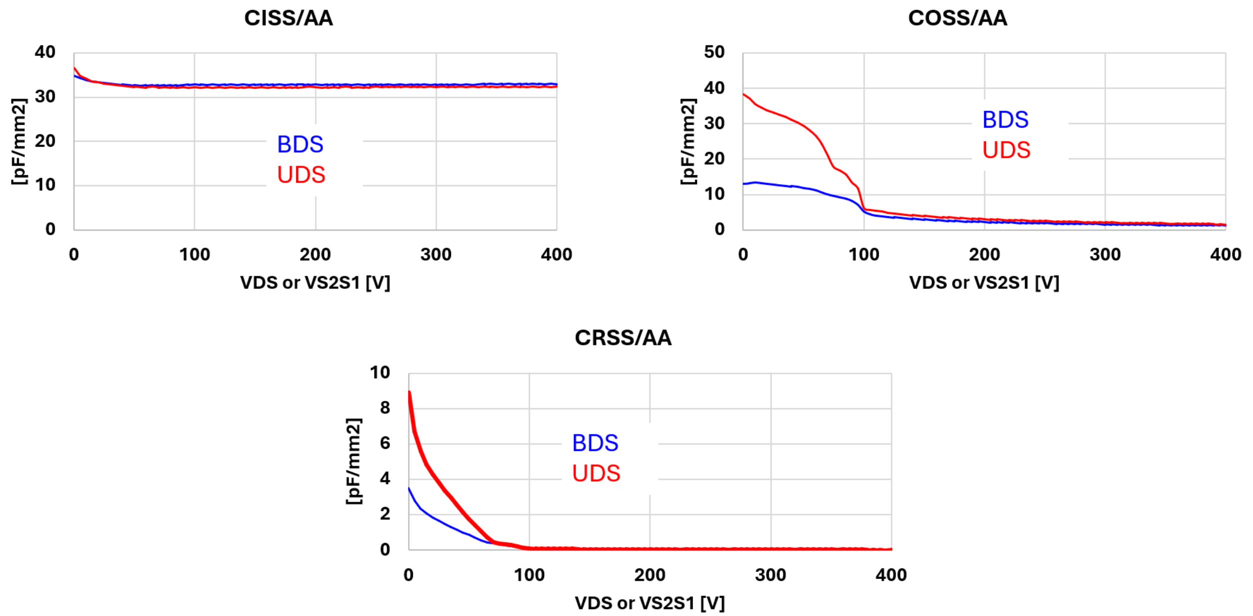


Figure 5.20: Comparison of C_{ISS}, C_{OSS} and C_{RSS} measurements performed on unidirectional and bidirectional DUTs.

In order to better investigate this discrepancy, it is useful to simulate for both unidirectional and bidirectional the 2D electron distribution at zero and high drain (or source-to-source) voltage in the cross section of the structure with TCAD. The results of this evaluation are reported in Figure 5.21 and 5.22.

Figure 5.21: TCAD simulation of the 2D electron concentration of the bidirectional DUT in off state (zero source-to-source voltage).

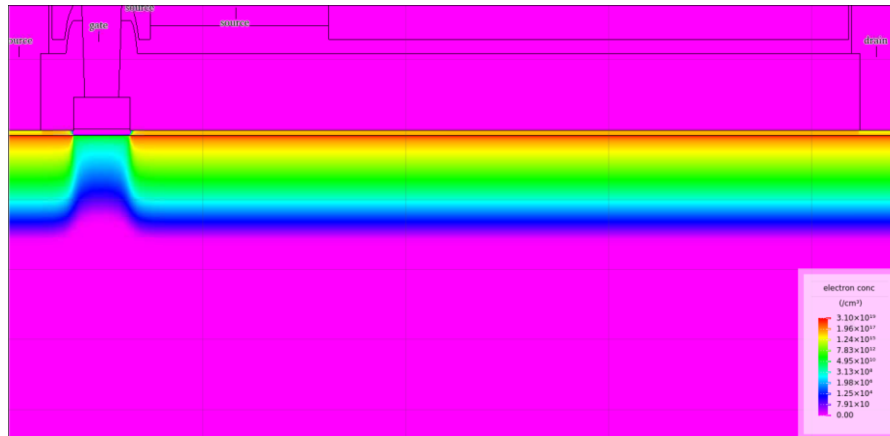


Figure 5.22: TCAD simulation of the 2D electron concentration of the unidirectional DUT in off state (zero drain voltage).

The main difference between the two distributions is that in the case of unidirectional devices the drain contact is virtually close to the p-GaN thanks to the 2DEG prolongation in the GATE-DRAIN access region while for the bidirectional this path is interrupted by the second p-GaN which is in off state. Therefore, for the bidirectional device, the source terminal sweeping from low to high voltage is shielded by the 2DEG in the middle (which is floating) and it is not close to the p-GaN of the main gate. This farther electrical distance between the two sources in the case of bidirectional implies a reduction of the capacitive contributions referred to the source which is acting as "drain", namely the gate-drain and source-drain capacitances. This is the explanation for the observed differences at low voltage in the experimental results between unidirectional and bidirectional. At high voltage, instead, there is a 2DEG depletion in the drift region, therefore when all the 2DEG has been depleted, both unidirectional and bidirectional structures share the same electron distribution, i.e. more or less the same capacitance.

5.2.2 C_{ISS}, C_{OSS}, C_{RSS} - $V_{GS1} = 0$ V & $V_{GS2} = 6$ V or vice versa

This condition represents the reverse blocking mode and the corresponding TCAD simulated data are reported and compared to the experimental results for C_{ISS}, C_{OSS} and C_{RSS} in Figure 5.23-5.25. In this case, TCAD simulations results were compared to experimental characterization only for the C_{OSS}.

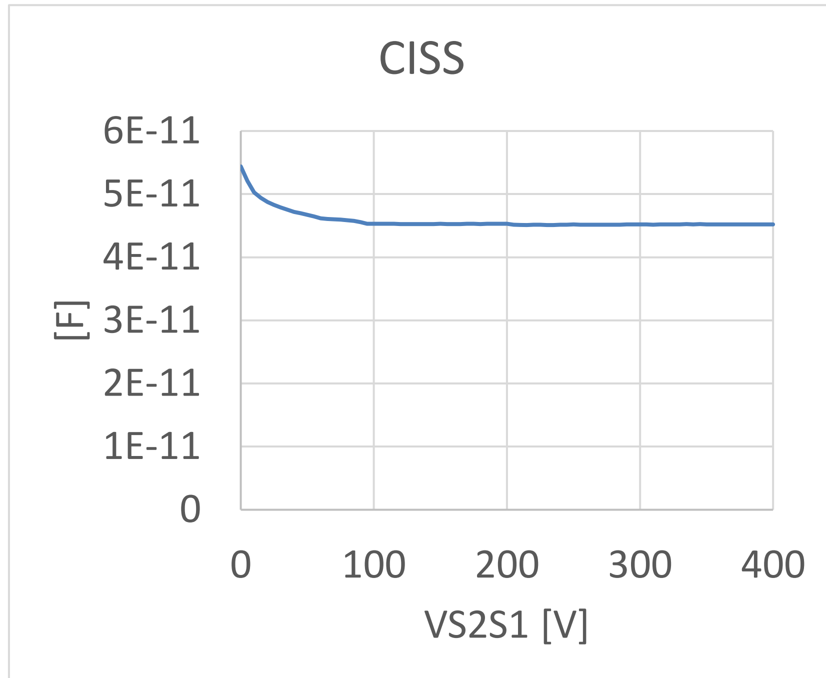


Figure 5.23: Input capacitance measured on bidirectional DUTs.

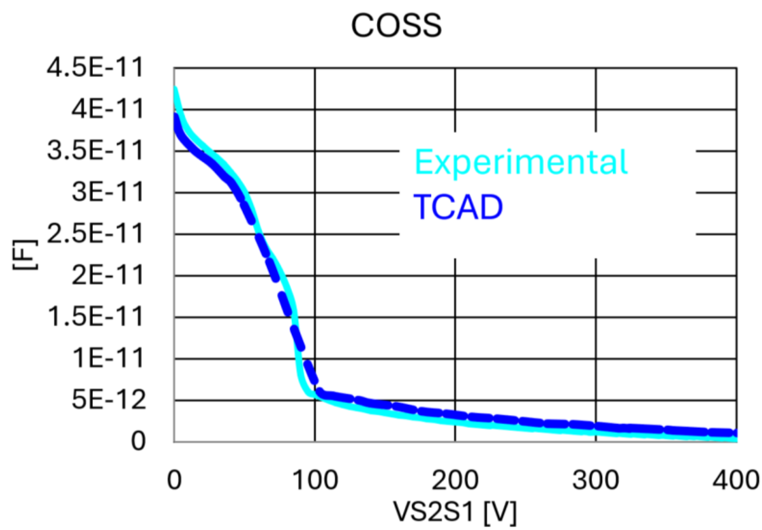


Figure 5.24: Output capacitance on bidirectional DUTs compared between measurements and TCAD simulations.

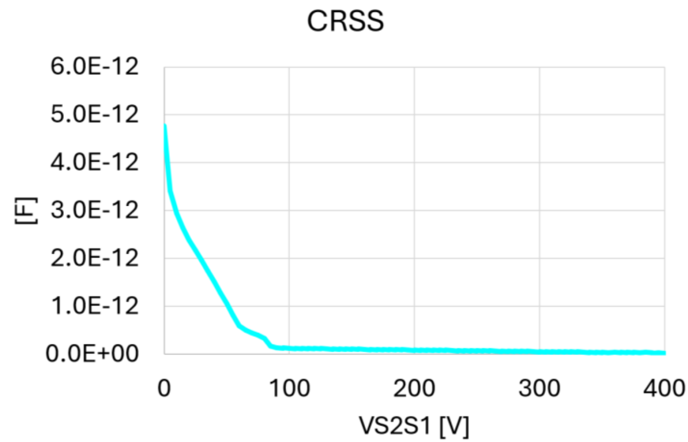


Figure 5.25: Reverse capacitance measured on bidirectional DUTs.

However, from the plots, it can be observed that in this mode the capacitance values are increased with respect to the previous case, especially at low voltage (Figure 5.26), and thus making the values are more similar to ones measured on the unidirectional DUTs.

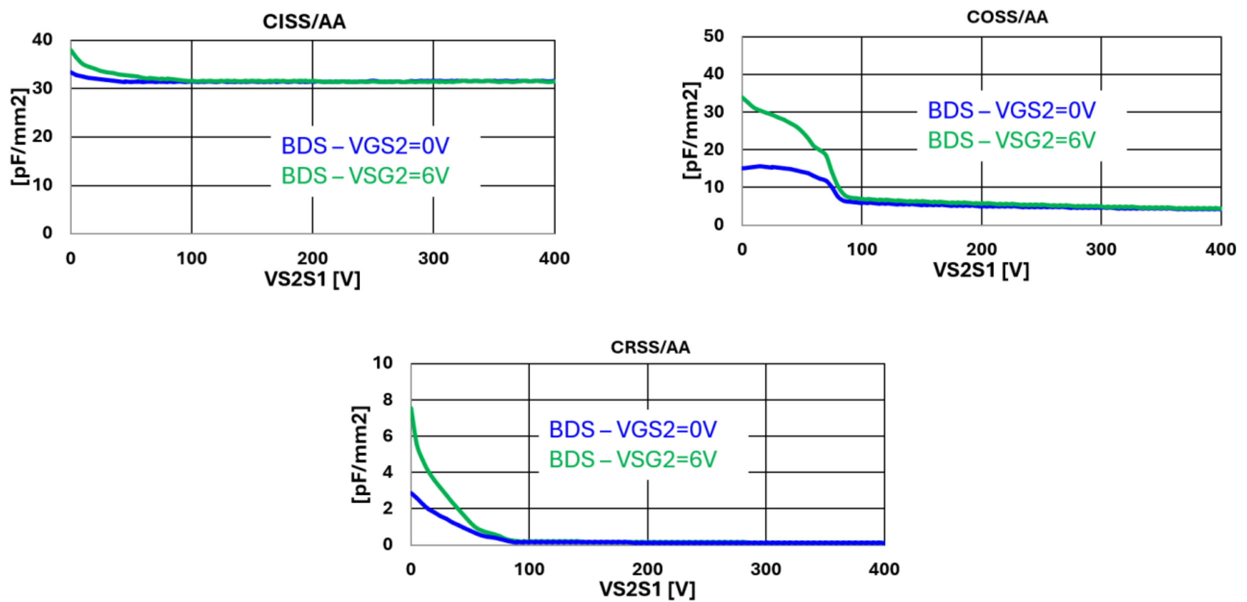


Figure 5.26: Comparison of C_{ISS}, C_{OSS} and C_{RSS} measurements performed on bidirectional DUTs in off and reverse blocking mode.

Also in this case, it is worth evaluating the 2D electron distribution at zero drain (or source-to-source) voltage simulated at TCAD for a better understanding of the phenomenon and the results are shown in Figure 5.27.

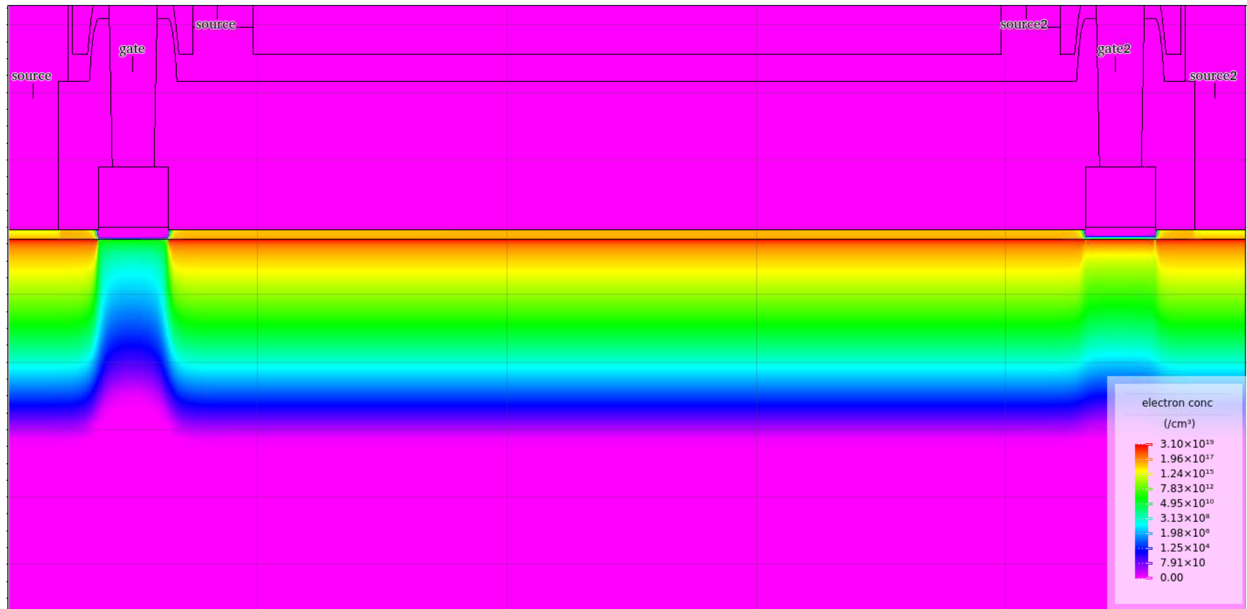


Figure 5.27: TCAD simulation of the 2D electron concentration of the bidirectional DUT in the case of zero source-to-source voltage and gate2 in on state.

Differently from the previous case, this time the second gate is on, therefore in the bidirectional device the source contact acting as drain is not interrupted by its p-GaN. As a consequence, it is connected to the 2DEG reaching the main p-GaN, thus reducing the effective distance between main gate/source and second source acting as drain. This condition is similar to what happens in a unidirectional device and that is why there is a good matching in all the capacitances in this case.

These two modes of operation are useful to investigate the capacitive contributions accounting for Q_{GD} and Q_{OSS} charges (which are usually reported in datasheets) and that can be related to either hard-switching or soft-switching losses.

5.2.3 C_G - $V_{GS2} = 0\ V \rightarrow 6\ V$ & $V_{GS1} = 0\ V \rightarrow 6\ V$

This last mode of operation involves no source-to-source (or drain-source) sweep but only gates (or gate) voltage sweeps, and it is useful to evaluate the gate capacitance. As in the previous sections, at first, TCAD simulations of the gate capacitance (C_G) and experimental results are shown and compared together. Also in this case, a good agreement between the two evaluations is observed, as shown in Figure 5.28.

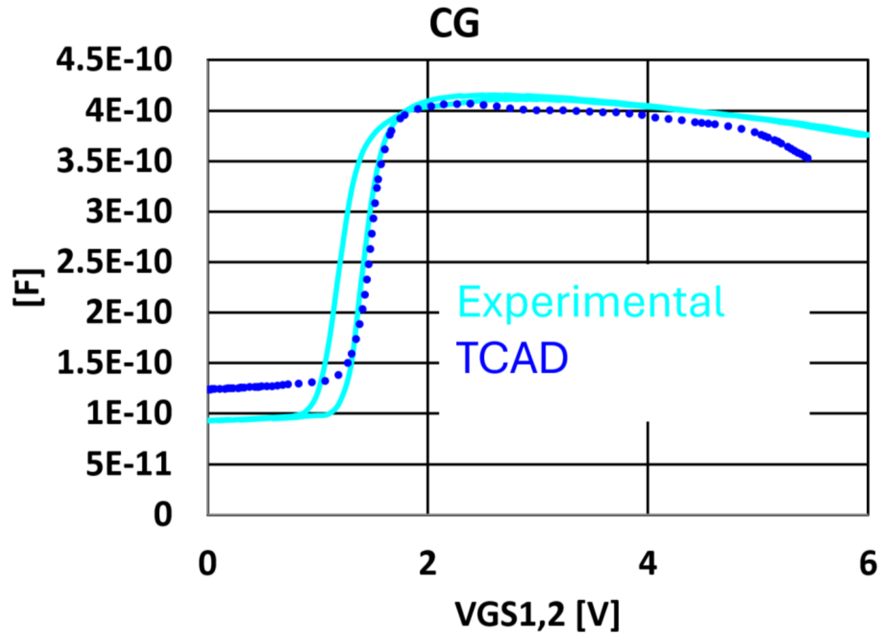


Figure 5.28: Gate capacitance on bidirectional DUTs compared between measurements and TCAD simulations.

Then, a comparison between the experimental results coming from bidirectional and unidirectional devices is shown in Figure 5.29.

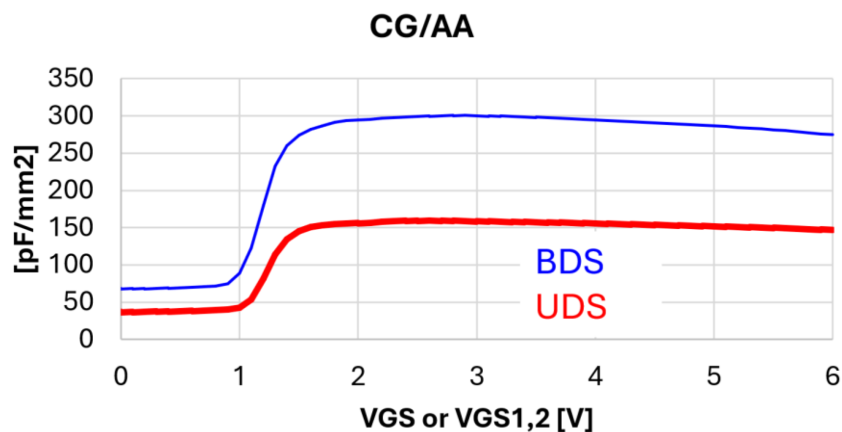


Figure 5.29: Comparison of gate capacitance measurements performed on unidirectional and bidirectional DUTs.

As can be seen, the value obtained for the bidirectional is approximately double what measured for the unidirectional. This phenomenon can be easily explained by the fact that in the bidirectional there are two gates with related p-GaN and, as already explained in Chapter 2, the main contribution to the gate capacitance comes from the p-GaN module (Figure 2.7). Also in

this case, 2D electron distributions have been simulated to compare the behavior of the unidirectional and bidirectional devices.
The gate capacitance can be of great interest both because it gives information regarding the Mg activation and both because can be used to estimate the total gate charge (Q_G) required to be "moved" when turning on the device.

5.3 Gate robustness

Bidirectional p-GaN devices discussed and presented in this chapter have been processed with the surface treatment for the gate reliability improvement, show in the previous chapter for the unidirectional. Therefore, the gate screening method discussed in Chapter 3 is here applied and extended for the case of bidirectional p-GaN HEMTs. In fact, in this case, the gate stress has been applied to both gates and therefore, two different gate currents have been monitored in order to check for a possible failure. Figure 5.30 shows the gate leakage monitoring for the stress test at 7 V (for both gates) at 25 °C, lasting 10,000 seconds.

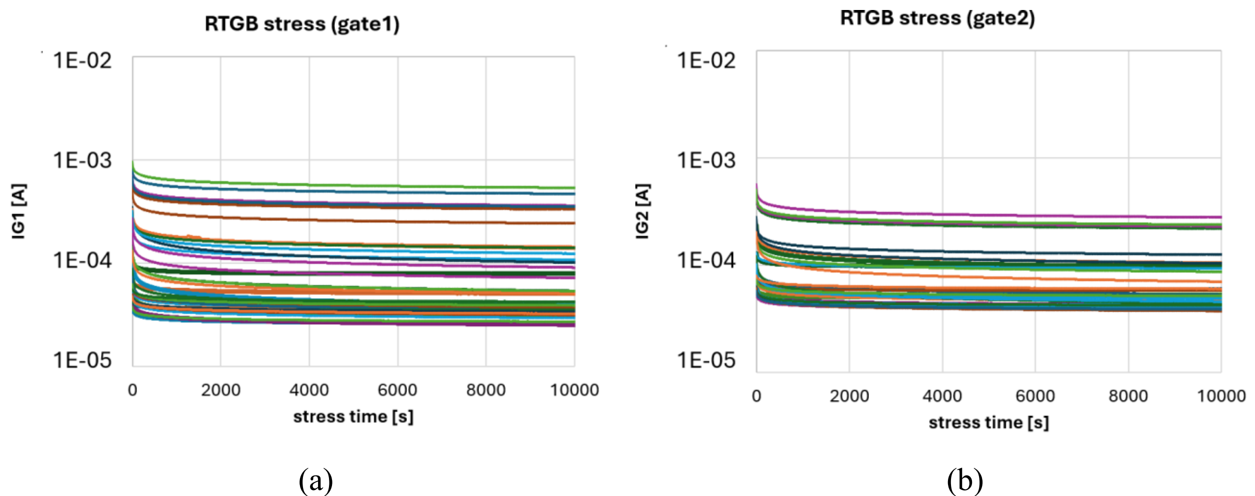


Figure 5.30: Gate leakage monitoring on both (a) gate1 and (b) gate2 on bidirectional DUTs under RTGB stress on both gates.

As shown in Figure 5.30, the surface treatment gives good preliminary gate reliability results also in the case of bidirectional devices. Of course, this characterization is only a starting point for the evaluation of the full reliability that must be then assessed on packaged devices with more advanced characterizations. However, it is important to underline that bidirectional devices require dedicated stress test because of their intrinsic structure (two gates) and for their target application as AC switches: for example, DHTOL tests have to be applied with AC voltage in order to approximate the actual waveforms that these kind of devices will experience during their functioning inside more complex circuits [1].

5.4 Conclusions

Bidirectional switches are efficiently enabled by lateral GaN HEMT technology and allow for strong integration / reduced area consumption. In this chapter, a full DC and AC experimental characterization has been shown for on-wafer bidirectional p-GaN HEMTs. Moreover, the experimental characteristics of the different operating modes (given by the combination of on and off states of the two gates) have been compared to the TCAD simulated ones, showing good agreement. The experimental results have been then compared to the ones obtained for unidirectional devices and TCAD simulations of both structures have been used for getting a comprehensive understanding of the similarities and differences between the two structures. For the bidirectional transistors, novel results were obtained by combining AC characterizations and simulations, explaining the reason for different capacitance profiles in the case of secondary gate on or off. Finally, a preliminary gate reliability characterization of the bidirectional DUTs has been shown, highlighting the difference with respect to the unidirectional case. Bidirectional devices showed good gate robustness under the considered stress conditions. The monolithic integration of bidirectional p-GaN HEMTs is one of the most promising results of p-GaN technology and it will require standardized reliability testing and special care for the substrate management for the dynamic R_{on} issue.

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6 Conclusions

In this work, several results about GaN HEMTs for power applications were presented and discussed. All the analyses were conducted by means of experimental characterization and TCAD simulations, showing the importance of combining these two types of evaluation for the understanding of the device physics, aimed at the improvement of the technology. Moreover, TCAD simulations are also a way to predict the results of new and unexplored solutions, before they are implemented in the fabrication of a device. Moreover, dedicated experimental measurements performed on devices already at wafer level allow to anticipate the application performance of the packaged devices, by focusing on single device behavior in specific biasing/temperature conditions, making it easier and faster to make process adjustments to the technology, reducing the time required for the learning cycles. This approach is general, and it could be followed also for developing other next-gen power technologies, like the UWBGs. However, in this thesis, this double approach (simulations and characterizations) has been pointed towards the study of normally-off 100 V and 650 V p-GaN HEMTs, with focus on the role of the p-GaN region on the device behavior, evaluated from different points of view. First, the role of p-doping by Mg was simulated and analyzed in detail comparing the behaviors of devices with no doping with others characterized by intentional Mg-doping and different activation annealing. In this case, CV measurements proved to be a very important tool for analyzing the p-GaN gate. Through the help of SIMS analyses, the impact of the Mg and H relative concentration profiles was interpreted. Moreover, some general indications were given about the influence of Mg-acceptor concentration and activation on many key parameters of the HEMT, like the pinch-off/threshold voltage, the transconductance and the on-resistance. Then, the analysis has been focused on the temperature behavior of GaN HEMTs, a crucial aspect for power switching devices. In this case, the impact of the p-GaN layer on the on-resistance and threshold voltage increase at high temperatures has been studied and evaluated in the case of 100 V devices, where the role of the resistance under the p-GaN was proved to be very important. Moreover, two different solutions with different p-GaN processing have been characterized and compared to the reference solution, confirming how both the gate leakage and the p-GaN activation level can be tuned for optimizing the high-temperature performance of GaN HEMTs. At different temperatures, dynamic on-resistance has been also studied, and it has been confirmed and demonstrated the invariance of the relative dynamic R_{on} increase from the temperature, in the case of C-doped buffers responsible for a single trapping mechanism. Moving further, some results about the drain and gate reliability of p-GaN HEMTs were discussed. Firstly, the degradation of the R_{on} after HTRB on 650 V rated devices was analyzed and interpreted through TCAD simulations. As a consequence, a process improvement was implemented on the devices, which showed better performance after HTRB. Then, an accelerated gate stress test has been proposed to have a preliminary evaluation of the p-GaN gate reliability and screen different technologies already at wafer level in not too large time-windows. This test already showed a weakness in some p-GaN implementations, where it produced a large degradation of the gate leakage of the device. Then, the performance of some possible solutions to make the p-GaN gate more robust were compared and, also in this case, TCAD simulations helped in understanding the weakness of an insulated p-GaN solution with respect to the standard p-GaN gate approach. Finally, the importance of the p-GaN gate was even more clarified by showing how monolithically-integrated bidirectional p-GaN HEMTs are

realized. In fact, these devices feature two gates (two p-GaN modules in the case of p-GaN-based) technologies and are very promising devices characterized by high voltage capabilities in both directions and high-power density enabled by the later GaN manufacturing. These devices were first simulated by TCAD and then the results were compared to both DC/AC experimental measurements, showing good match. TCAD simulations were also used to interpret the behavior of bidirectional p-GaN HEMTs in all the different operating modes (depending on the states of the two gates) with respect to the results coming from a conventional unidirectional (one-gate) p-GaN HEMT.

List of Publications

List of published contributions covered in the PhD thesis.

[1] Unveiling the Role of Hole Barrier Traps on ON-Resistance Instability after Gate Bias Stress in p-GaN Power HEMTs / Zagni, Nicolo'; Chini, Alessandro; Verzellesi, Giovanni; Cioni, Marcello; Giorgino, Giovanni; Nicotra, Maria Concetta; Eloisa Castagna, Maria; Iucolano, Ferdinando. - (2023). (Intervento presentato al convegno 2023 IEEE International Integrated Reliability Workshop (IIRW) tenutosi a South Lake Tahoe, CA, USA nel 8-12 Ottobre 2023) [10.1109/iirw59383.2023.10477714].

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