Flexible CMOS electronics based on p-type $Ge_2Sb_2Te_5$ and n-type $InGaZnO_4$ semiconductors

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***Abstract*—**Ultra-thin p-type chalcogenide glass $Ge_2Sb_2Te_5$ (GST) semiconductor layers are employed to form flexible thin-film transistors (TFTs). For the first time, TFTs based on GST show saturating output characteristics and an ON/OFF ratio up to 388, exceeding present reports by a factor of ~20. The channel current modulation is greatly enhanced by using ultra-thin 5 nm thick amorphous GST layers and 20 nm thick high-k Al_2O_3 gate dielectrics. Flexible CMOS circuits are realized in combination with the n-type oxide semiconductor $InGaZnO_4$ (IGZO). The CMOS inverters show voltage gain of up to 69. Furthermore, flexible NAND gates are presented. The bending stability is shown for a tensile radius of 6 mm.

I. Introduction

Flexible electronics have been emerging in the last years projecting a future with novel applications in displays, healthcare, mobile devices, internet of things (IoT) and human-machine interfaces [1, 2]. Although flexible complementary electronic circuits have been shown for organic semiconductors [3], the realization of entirely inorganic flexible CMOS is highly desirable for high performance electronics where thin-film transistors (TFTs) require large carrier mobilities [1, 2]. Although n-type oxide semiconductors (*i.e.*, In-Ga-Zn-O (IGZO)) serve with mobilities > 10 cm^2/Vs, the challenges of finding a suitable inorganic p-type semiconductor still remain. Thus, n-type oxide semiconductors are usually employed in unipolar technology [4]. However, this approach lacks the advantages of CMOS which enables low power consumption, high gain, superior noise immunity and simplified circuit design [5]. Recently, efforts have been undertaken to realize complementary technology with oxide semiconductors involving p-type carbon nanotubes [2, 6, 7] or p-type SnO [5]. GST is an alloy of Ge, Sb and Te belonging to the family of chalcogenide glasses. So far, it has not received much attention as a transistor material despite its large popularity in phase-change memory technology [8] and its known p-type semiconducting properties [9] with large hole mobilities in the crystalline phases ranging from 15-200 cm^2/Vs depending on the material composition [10, 11]. Prior works on GST TFTs have found poor drain current I_D modulation with ON/OFF ratios hardly exceeding a factor of 20 [12] even when the GST thickness was scaled down to 10 nm [13]. In this work, we further reduce the GST thickness to 5 nm and enhance the gate control by employing a 20 nm thick Al_2O_3 high-k gate dielectric. As a consequence, we achieve a ~20-fold improvement in ON/OFF ratio and, for the first time, report saturating TFT output characteristics for amorphous GST TFTs. Furthermore, we show their application in flexible CMOS inverters and NAND gates combined with IGZO TFTs. The devices show a bending stability down to a tensile radius of 6 mm.

II. Device Fabrication

The devices were fabricated on a free-standing flexible 50 µm thick polyimide foil. The schematic process flow is shown in Fig. 1. Initially, the substrate was cleaned by sonication in acetone and isopropanol, and subsequently annealed at 200 °C in air. Prior to the device fabrication, the substrate was passivated by plasma-enhanced chemical vapor deposition of SiN_x at 150 °C. First, a Ti/Au/Ti (5/30/5 nm) gate metal was deposited by e-beam evaporation and structured by lift-off. Then, the surface was cleaned by a UV ozone treatment for 1 min. The 20 nm thick Al_2O_3 gate dielectric was deposited by atomic-layer deposition at 150 °C. The 15 nm thick amorphous $InGaZnO_4$ n-type semiconductor was RF magnetron sputtered and wet chemically etched to form islands. The 5 nm thick amorphous $Ge_2Sb_2Te_5$ p-type semiconductor was dc magnetron sputtered as described in [14] and structured by lift-off. Instead of standard photoresist, the GST structuring was performed by deep-UV lithography and PMMA photoresist to protect the Al_2O_3 surface. Both sputter depositions were performed at room temperature. Afterwards, via holes were wet-chemically etched into Al_2O_3 to access the gate contacts. Finally, both source/drain contacts were e-beam evaporated and structured by lift-off. Ge/Ni/Au (5/5/30 nm) and Ti/Au (10/60 nm) were used for GST and IGZO, respectively. A photograph of the fully-fabricated devices is shown in Fig. 2, and the schematic and optical micrograph of a CMOS inverter are presented in Fig. 3.

III. Results and Discussion

The devices were characterized with a semiconductor device analyzer (Agilent technologies, B1500A) on a probe station at ambient conditions. First, the TFTs of the inverter, shown in Fig. 3, were characterized separately. In Fig. 4, the TFT transfer (a), (c) and output (b), (d) characteristics of IGZO and GST, respectively, are displayed. The IGZO TFTs exhibit typical performance with an effective field-effect mobility $\mu_{FE,\,eff}$ of 24.9 cm^2/Vs and an ON/OFF ratio of ~$8 \cdot 10^4$. The GST TFTs show the desired p-type behavior with an ON/OFF modulation of 388, which is ~20-fold higher than present work [12]. Their $\mu_{FE,\,eff}$ is ~0.04 cm^2/Vs, which is expected for the amorphous phase [11]. We attribute the large counterclockwise I_D hysteresis to defects in GST or at the

GST/Al_2O_3 interface. However, the GST TFTs exhibit a saturating output characteristic with small hysteresis. The TFT device parameters for GST and IGZO are extracted at a drain-source voltage V_{DS} = -100 mV and +100 mV, respectively and can be reviewed in Table 1. The small-signal capacitance-voltage (CV) characteristics of the GST and the IGZO TFTs with equal gate areas are shown in Fig. 5, while the corresponding optical micrographs are displayed in Fig. 6. The IGZO shows the commonly observed CV curve indicating the value of the Al_2O_3 capacitance at +5 V [15]. The GST CV characteristic shows the p-type transition reaching the Al_2O_3 capacitance value at -5 V and a frequency of 1 kHz. For higher frequencies, the complete GST accumulation is not achieved which also indicates the existence of defects within the material. The accumulation capacitance of 0.34 µF/cm^2 reveals an Al_2O_3 dielectric constant of 7.6, comparable to prior reports [16], which is used in all calculations for $\mu_{FE, eff}$. The inverter dc characteristics are displayed in Fig. 7. The transfer characteristic shows the successful modulation of V_{out} at V_{dd} = 2 V, 3 V, 4 V and 5 V. We find the maximum gain of 54 at V_{dd} = 5 V. The maximum static power consumptions for the V_{in}-sweep from 0 V to 5 V and from 5 V to 0 V are 0.8 µW and 6 µW, respectively. Despite the GST hysteresis, we find noise margins above 50 %. The ac characteristics of the logic gates are investigated with a 2-channel waveform generator (Keysight, 33600A) connected to the input(s) and a precision source/measure unit (Keysight, B2902A) for the static supply of V_{dd}. The output is monitored on an oscilloscope (Agilent technologies, MSO-X 3014A, C_L = 14 pF, R_L = 1 MΩ). Fig. 8 displays the ac characteristic of the inverter at 500 Hz. Furthermore, a CMOS NAND gate together with its ac modulation is presented in Fig. 9.

Finally, the bending characteristics are investigated by attaching the flexible polyimide substrate to a metallic rod with a radius R = 6 mm (see Fig. 10). Thus, the IGZO TFT and GST TFT are subjected to tensile strain parallel and perpendicular to the channel direction, respectively. The IGZO TFT shows changes in the subthreshold characteristic whereas the above-threshold I_D remains nearly unchanged (Fig. 11 (a), (b)). The GST TFT encounters a reduction in I_D and $\mu_{FE, eff}$ as well as a negative threshold voltage shift (Fig. 11 (c), (d)). The TFT changes with bending are summarized in Table 2. Fig. 12 displays the inverter characteristics in flat and bent conditions. The inverter characteristics slightly improve when the devices are bent. The gain increases to a value of 69 and the maximum static power consumption and the noise margins decrease and increase, respectively (Table 3). This can be attributed to a slightly reduced hysteresis in the GST TFT (Fig. 11 (c)).

IV. Conclusion and Outlook

We have shown the successful integration of p-type GST TFTs and n-type IGZO TFTs on flexible polyimide foil with bending stability at a radius of 6 mm. The GST TFTs have a 20-fold improvement of the ON/OFF ratio compared to previous work and show, for the first time, fully saturating output characteristics. The $\mu_{FE, eff}$ is ~0.04 cm^2/Vs. We also tested the crystallization of the TFTs which deteriorated the device performance, indicating that the ultra-thin GST layer undergoes degradation at the source/drain contacts at 200 °C, which needs to be further studied for different source/drain materials. In future, the successful crystallization of GST may enhance the $\mu_{FE, eff}$ to levels which render it an equal counterpart to n-type oxide semiconductors. Nevertheless, the here presented semiconductor deposition processes are fully compatible with room temperature and large-area fabrication which could enable flexible electronics even on substrates like paper. The realization of flexible CMOS inverters with high gain up to 69 and NAND gates is a first demonstration for hybrid complementary circuits based on oxide semiconductors and chalcogenide glasses (*i.e.*, GST).

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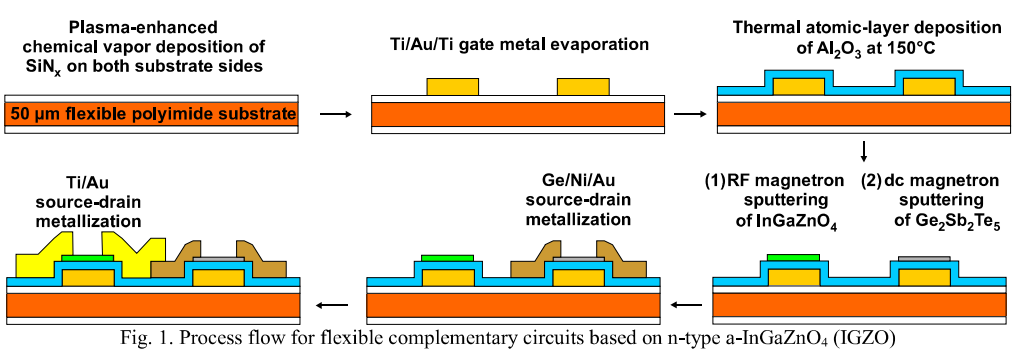

Fig. 1. Process flow for flexible complementary circuits based on n-type a-$InGaZnO_4$ (IGZO) and p-type a-$Ge_2Sb_2Te_5$ (GST) semiconductors.

Fig. 2. Flexible complementary circuits and thin-film transistors on a 50 µm thick polyimide foil.

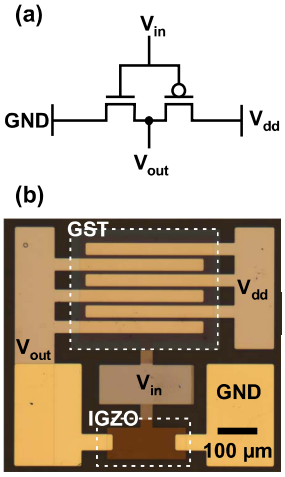

Fig. 3. CMOS inverters. (a) Schematic circuit. (b) Optical micrograph, where the $Ge_2Sb_2Te_5$ (GST) thin-film transistor (TFT) and $InGaZnO_4$ (IGZO) TFT have channel widths of 1500 µm and 40 µm, and channel lengths of 10 µm and 160 µm, respectively.

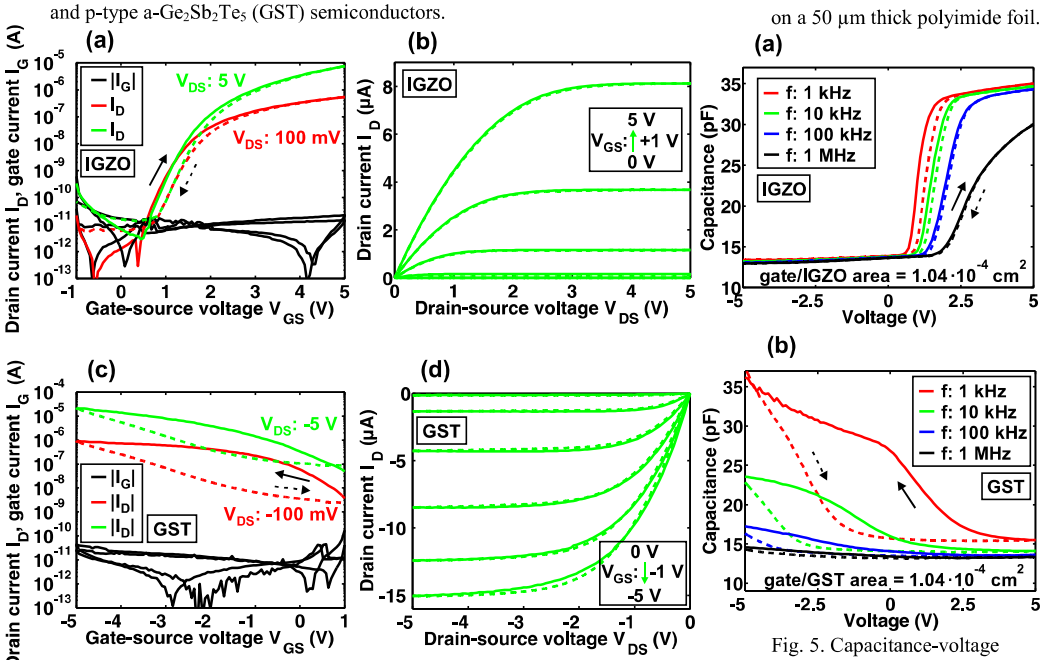

Fig. 4. Transfer (a), (c) and output (b), (d) characteristics of n-type $InGaZnO_4$ (IGZO) and p-type $Ge_2Sb_2Te_5$ (GST) thin-film transistors (TFTs) at different drain-source voltages V_{DS}, respectively. The GST TFT and IGZO TFT have channel widths of 1500 µm and 40 µm, and channel lengths of 10 µm and 160 µm, respectively.

Fig. 5. Capacitance-voltage characteristics at different frequencies f. (a) $InGaZnO_4$, (b) $Ge_2Sb_2Te_5$.

	IGZO	GST
V_{Th} (V)	2.44	0.13
$\mu_{FE,\,eff}$ (cm^2/Vs)	24.9	0.039
SS (mV/dec)	281	1581
ON/OFF	~$8 \cdot 10^4$	388

Table 1. Thin-film transistor device parameters: Threshold voltage V_{Th}, effective field-effect mobility $\mu_{FE,eff}$, subthreshold swing SS and ON/OFF ratio.

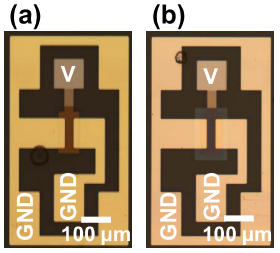

Fig. 6. Optical micrographs of thin-film transistors (TFTs) used for the capacitance-voltage measurements. The gate area of each TFT is $1.04 \cdot 10^{-4}$ cm^2. The voltage V was applied to the gate and, source and drain were connected to ground (GND). (a) $InGaZnO_4$. (b) $Ge_2Sb_2Te_5$

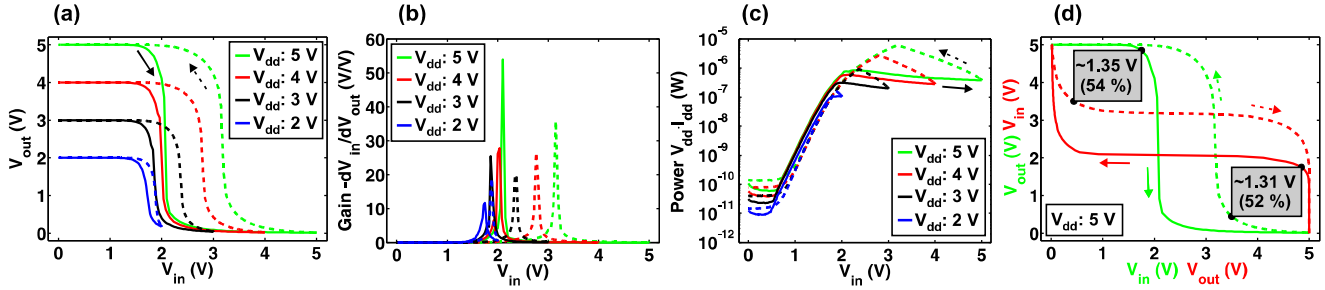

Fig. 7. Flexible CMOS inverter dc characteristics at different supply voltages V_{dd}. (a) Transfer characteristics. (b) Gain. The solid and dashed lines represent the V_{in}-sweeps from 0 V to 5 V and from 5 V to 0 V, respectively. (c) Static power consumption. (d) Noise margin for V_{dd} = 5 V.

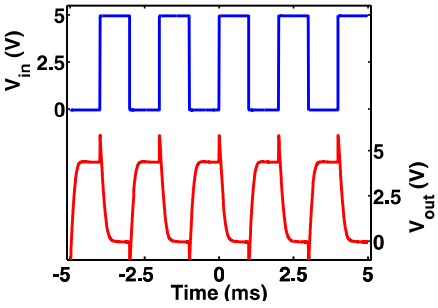

Fig. 8. The ac characteristics of a flexible CMOS inverter at a frequency of 500 Hz and V_{dd} = 5 V.

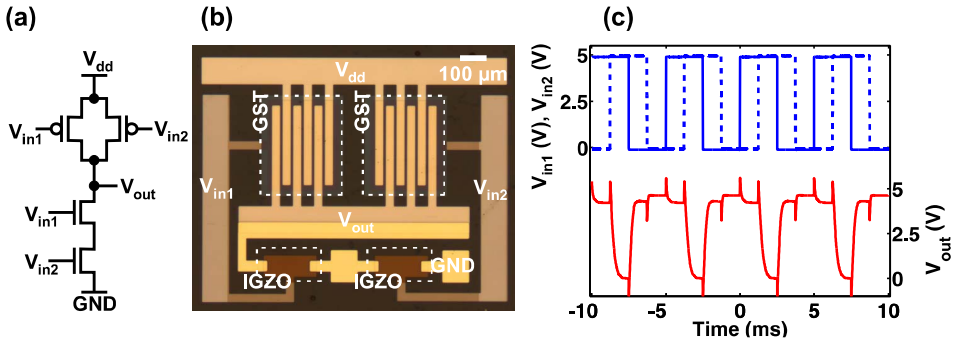

Fig. 9. CMOS NAND gate. (a) Schematic circuit. (b) Optical micrograph where the $Ge_2Sb_2Te_5$ (GST) thin-film transistors (TFTs) and $InGaZnO_4$ (IGZO) TFTs have channel widths of 1500 µm and 40 µm, and channel lengths of 10 µm and 160 µm, respectively. (c) The ac characteristics at input frequencies of 200 Hz and V_{dd} = 5 V.

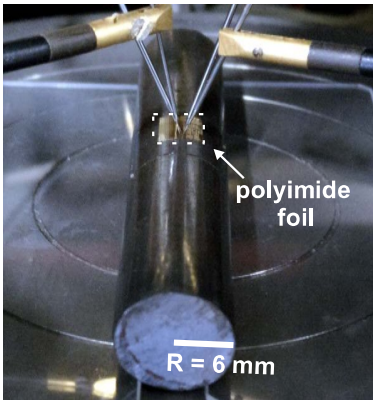

Fig. 10. CMOS circuits and thin-film transistors on flexible polyimide foil bent around a metallic rod with a radius R = 6 mm.

	flat		R = 6 mm	
	IGZO	GST	IGZO	GST
V_{Th} (V)	2.27	0.09	2.30	-0.04
$\mu_{FE,\,eff}$ (cm^2/Vs)	25.3	0.044	25.5	0.034
SS (mV/dec)	274	1421	295	1642
ON/OFF	$1.6 \cdot 10^5$	307	$2.3 \cdot 10^5$	290

Table 2. Thin-film transistor device parameters in flat condition and bent to a radius R = 6 mm. Threshold voltage V_{Th}, effective field-effect mobility $\mu_{FE,eff}$, subthreshold swing SS and ON/OFF ratio.

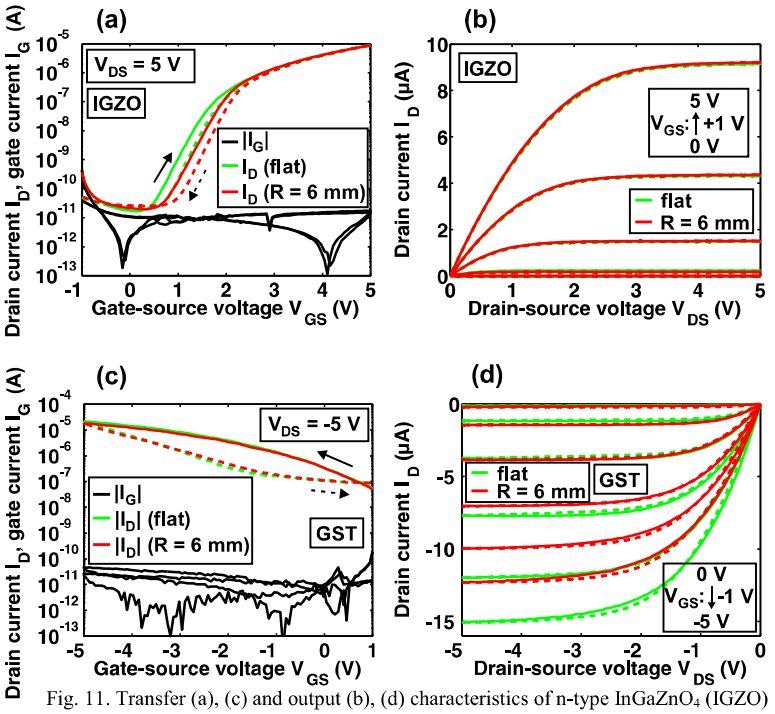

Fig. 11. Transfer (a), (c) and output (b), (d) characteristics of n-type $InGaZnO_4$ (IGZO) and p-type $Ge_2Sb_2Te_5$ (GST) thin-film transistors (TFTs), respectively, comparing bent (radius R = 6 mm) and flat condition. The GST TFT and IGZO TFT have channel widths of 1500 µm and 40 µm, and channel lengths of 10 µm and 160 µm, respectively.

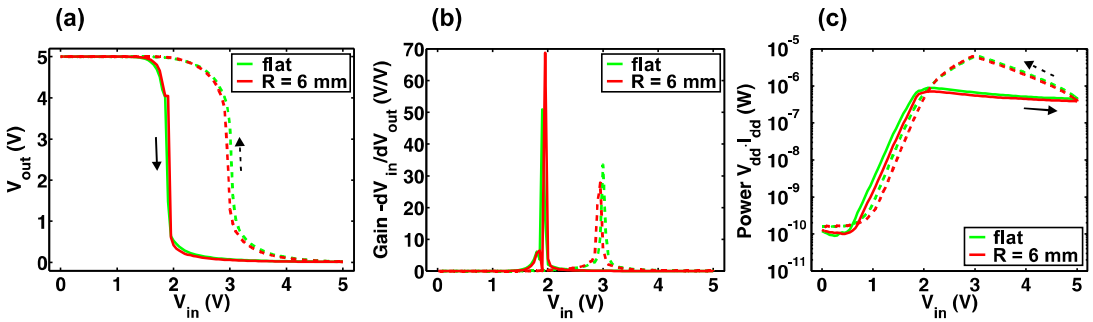

Fig. 12. Flexible CMOS inverter dc characteristics at a supply voltages V_{dd} = 5 V in bent (radius R = 6 mm) and flat conditions. (a) Transfer characteristics. (b) Gain. The solid and dashed lines represent the V_{in}-sweeps from 0 V to 5 V and from 5 V to 0 V, respectively. (c) Static power consumption.

	flat	R = 6 mm
Gain (V/V)	51	69
P_{max} (µW)	6.5	6.2
NM_H (V)	1.52	1.58
NM_L (V)	1.13	1.21

Table 3. CMOS inverter characteristics in flat condition and bent to a radius R = 6 mm. Gain, Maximum static power consumption P_{max}, noise margin high NM_H and noise margin low NM_L.