Pushing the limits of NAND technology scaling with ferroelectrics

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Artificial intelligence (AI) continues to drive transformative advancements across various industries. The data-intensive nature of AI training (and inferencing) has resulted in the generation of unprecedented volumes of data with machine-generated content surpassing human-generated data by more than 100-fold in 2025. Efficiently managing this data influx necessitates advanced digital storage technologies. However, traditional NAND flash memory, which is critical for supporting data flows in AI systems—alongside high-bandwidth memory, for AI training—faces fundamental scaling limitations as it approaches the 1000-layer milestone, encompassing more than 40 trillion transistors. This article delves into the potential of hafnia-based ferroelectric materials as a breakthrough solution to these challenges. Recent advancements indicate that the intrinsic limitations of ferroelectric field-effect transistors (FEFETs) can be mitigated through material and device-level engineering. These advancements enable FEFETs to meet the stringent density, reliability, and scalability requirements of future three-dimensional NAND technology. The role of ferroelectrics in addressing NAND scaling challenges and expanding storage capabilities presents a promising avenue for meeting the storage demands of the AI-driven era.

Introduction

The explosive growth of artificial intelligence (AI), particularly large language models (LLMs), is fundamentally transforming data generation and storage technologies. Modern LLMs have scaled to extraordinary sizes, with leading models in 2025 such as OpenAI's GPT-4o and Meta's Llama 3.1 containing hundreds of billions to greater than 1 trillion parameters, driving a surge in both the volume and complexity of data required for training and inference. This rapid expansion is reflected in the booming LLM market, projected to grow from USD$7.77 billion in 2025 to more than USD$123 billion by 2034, as organizations across industries adopt these technologies for automation, analytics, and decision making.[1] The resulting data deluge is reshaping storage infrastructure: solid-state drives (SSDs) based on vertical NAND (V-NAND) technology have become essential for active, high-speed data

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storage in data centers, offering twice the speed and greater reliability compared to earlier technologies, while hard disk drives (HDDs) remain the cost-effective choice for storing cold, infrequently accessed data. Looking ahead, V-NAND SSDs are evolving along two critical fronts: first, the push for ultrahigh-density storage, with current SSDs stacking more than 300 layers of NAND cells to deliver massive capacities that rival or surpass the less-dense HDDs; and second, the integration of in-storage compute capabilities, enabling AI inference and analytics to occur directly within the storage device, which dramatically reduces latency and energy consumption for edge and on-device AI workloads. These advancements ensure that storage technologies can keep pace with the unprecedented scale and speed of AI-driven data generation, empowering enterprises and consumers alike to harness the full potential of next-generation AI systems.

Over the past decade, NAND has been the cornerstone of long-term storage, maintaining a 50× per decade increase in data density for nearly three decades, since its introduction in 1987.[2] Initially developed with a 1-μm feature size, two-dimensional (2D) NAND technology underwent significant advancements in material, process, device, and design technologies.[3] This enabled the 2D NAND technology to overcome scaling barriers and shrink down to 15 nm by the 2010s. The introduction of three-dimensional (3D) NAND in 2007, with the first 24-layer multi-level cell (MLC) NAND product by Samsung in 2014, revolutionized the industry by allowing vertical stacking of memory cells.[4–6] Alongside these advancements, improvements in multilevel cell technology have increased the bits per cell, enhancing storage capacity and reducing costs. Current 3D NAND technology has reached more than 300 layers achieving greater than a one-million fold increase in bit areal density over 37 years.[3]

Several key processing innovations have contributed to these advancements. The introduction of self-aligned shallow trench isolation (SA-STI) improved reliability, while pitch doubling and quadrupling enabled cell patterning beyond photolithography capabilities.[7] Air-gap architecture reduced interconnect capacitance and cell-to-cell interference.[8,9] Initially, floating gate transistors based on Fowler–Nordheim tunneling, used in planar NAND devices[2] and charge trap flash (CTF), where data were stored by trapping charges in a nitride layer, were commercialized in the early 2000s. During the transition to 3D NAND, the enhanced erase and retention characteristics of BE-TANOS (band engineered TaN/AlO/SiN/Oxide/Si)-based charge trap flash prompted their adoption in the late 2000s and early 2010s.[10,11] Today, CTF-based 3D NAND dominates the NAND market. Gate-all-around (GAA) cell architecture improved gate-to-channel coupling and reduced cell-to-cell interference, while the use of tungsten for wordlines reduced resistivity. The CMOS under array (CuA) architecture reduced die size and improved program/read performance, and GIDL-erase provided body biasing in floating body cells.[12,13]

These innovations have led to the achievement of bit areal densities with the latest reports at the IEEE International Solid-State Circuits Conference (ISSCC) 2025 by SK Hynix demonstrating a 321-layer quad-level cell (QLC) NAND with a data density of 28.8 Gb/mm^2,[14] and Samsung demonstrating a 400+ layer triple-level cell (TLC) NAND with 28 Gb/mm^2 data density.[15] Future scaling directions include logical scaling that involves increasing bits per cell to enhance data density, physical scaling, which explores new cell architectures such as split cell and process techniques such as nitride-cut and cryogenic etching and performance scaling which focuses on improving interface I/O performance and array program/read bandwidth. However, scaling past 1000 layers and 4-bit per cell (QLC), which is crucial to maintaining the bit areal density scaling in 3D NAND, is becoming increasingly challenging with CTF devices facing reliability challenges even at the current scaled dimensions.[16]

Challenges to scaling in 3D NAND

The challenges in 3D NAND scaling stem from the charge trap flash cells and the processing challenges associated with the shrinking dimensions (**Figure** 1).

CTF memory, despite its advantages, faces several limitations that impact its scalability and performance. One of the primary challenges with CTF is the retention and endurance of the memory cells. The charge-trapping layer, typically made of silicon nitride, can suffer from charge loss over time, which affects the retention characteristics of the cell. These reliability challenges are exacerbated by the high electric fields required for programming and erasing the cells, leading to charge leakage in adjacent cells and increased degradation of the memory window even at current 3D NAND dimensions. This, in turn, limits logic scaling as large write voltages are required for TLC/QLC operation.

Another significant limitation of CTF with logic scaling is the reducing number of electrons being trapped per level. This combined with the non-uniform distribution of trapped charges increases the variability in the threshold voltage (V_T). This variability could result in increased read errors and reduced reliability of the memory array. The presence of traps in the silicon nitride layer could also lead to increased random telegraph noise (RTN), further degrading the performance of the memory cells. Additionally, the scaling of CTF memory is constrained by the physical limitations of the charge-trapping layer. As the memory cells are scaled down, maintaining a high density of trapped charges without significant charge loss becomes increasingly difficult.

Ferroelectrics as a drop-in alternative

With CTF devices approaching fundamental scaling and reliability barriers, new memory elements are being pursued. The discovery of ferroelectricity in CMOS-compatible zirconia-doped hafnium oxide renewed interest in ferroelectric memories, which offer intrinsic nonvolatility, endurance, and scalability. Early demonstrations showed the limitations of other use cases, ferroelectric NV-DRAM highlighted the high switching voltages, while FEFETs for embedded applications

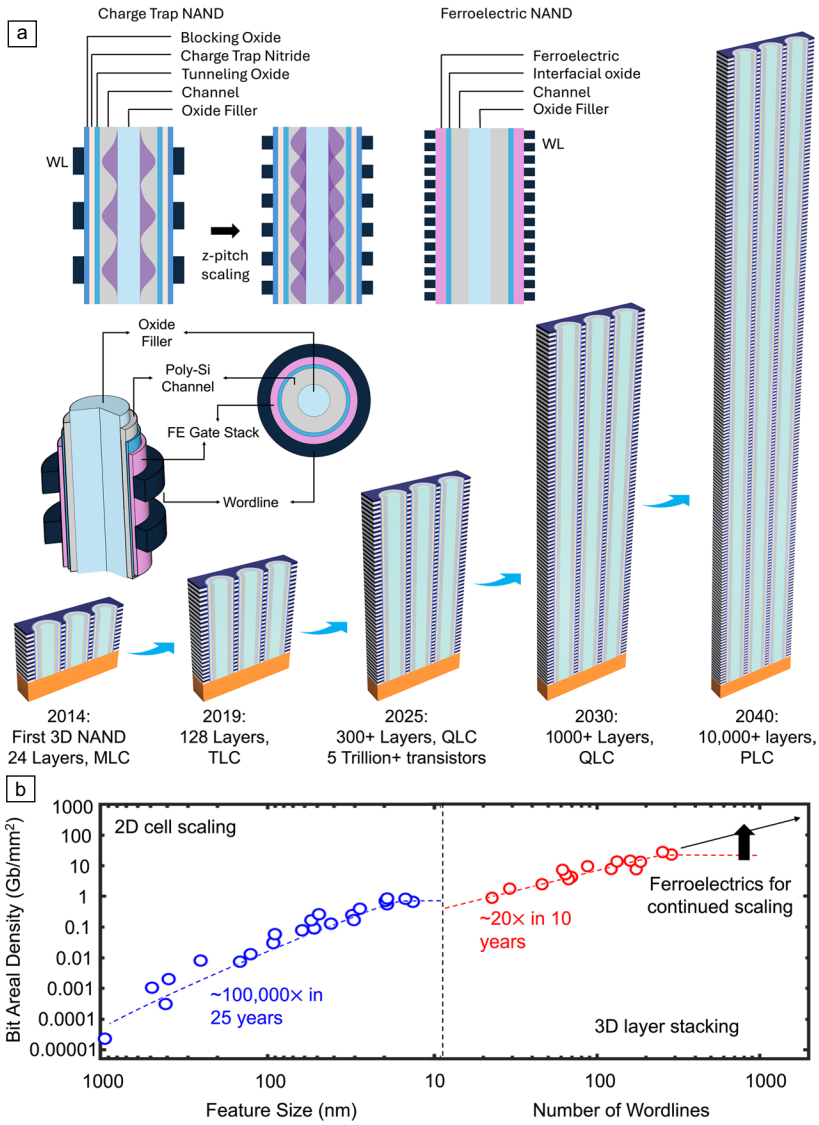

Figure 1. (a) This figure summarizes scaling in NAND across decades enabled by novel innovations in processing, device structures, and array architecture. However, continuing this trend requires innovations to overcome the reliability, processing, and cost barriers associated with further scaling.[3] (b) As the number of layers increase, the current *z*-pitch becomes challenging due to processing difficulties and reliability challenges, and vertical NAND faces the unique problem of exceeding its package height, a problem no other semiconductor technology is at the risk of facing.[16] Decreasing the *z*-pitch is also complicated due to lateral charge migration and associated reliability challenges such as retention loss.[3,16] The introduction of ferroelectrics is proposed as a solution to drive *z*-scaling in FE-NAND devices.[17–19] WL, word line; MLC, multilevel cell; TLC, triple-level cell; QLC, quad-level cell; PLC, penta-level cell; HLC, hexa-level cell; HeLC, hepta-level cell.

are limited by high write voltage and low memory window. NAND, with its tolerance for higher write voltages and need for large coercive voltages, is particularly well-suited to benefit from ferroelectric integration, making ferroelectrics a compelling successor to charge trap layers.

Over the last two years, hafnia-based ferroelectrics have emerged as a potential replacement for charge trap layers in 3D NAND, enabling projected data densities exceeding 100 Gb/mm^2 through *z*-scaling beyond 1000 layers. Ferroelectric field-effect transistors (FEFETs) store data via bound ferroelectric polarization, with operational states controlled by gate voltage: a positive pulse aligns polarization towards the channel, lowering the threshold voltage (V_T) to a "program" (PGM) state, while a negative pulse reverses polarization, raising V_T to an "erase" (ERS) state. This polarization-driven V_T modulation eliminates reliance on trapped charges, improving retention and endurance at scaled dimensions, thereby enhancing scalability at higher logic levels. FEFETs also operate at low voltages and nanosecond speeds, mitigating endurance degradation at higher logic levels. However, ferroelectric hafnia-based FEFETs face limitations, with low memory windows (<3 V) even at 20-nm gate stack thicknesses, constraining their multilevel capability despite these intrinsic advantages.

The ferroelectric gate stack had to be engineered to meet the conventional NAND specifications while achieving better performance to develop as a drop-in replacement for the charge trap layer. These specifications include the following: (1) achieving TLC/QLC compatible operation (MW $\geq$ 7.5) at, (2) low write voltage (V_{write} < 15 V), and (3) 3D NAND compatible thickness (t_{stack} < 20 nm).

Yoon et al. demonstrated at the Very Large Scale Integration (VLSI) Symposium 2023 that insertion of a dielectric layer next to the gate increases the memory window (MW) to 10.5 V at write voltages lower than 15 V, thereby enabling penta-level (PLC) operation at nearly half the operating voltage of conventional 3D NAND.[17] By demonstrating the viability of integrating ferroelectrics in a Marconi structure-based 3D NAND, they made a case for band-engineered HZO gate stacks with dielectric inserts as a potential drop-in solution to the CTF layer. Following this, several efforts engineered the FE-NAND devices to improve different properties, including MW, incremental step pulse program/erase (ISPP/E) slope, retention, and disturb. **Figure** 2 summarizes the wide variety of materials and gate stacks explored over the past two years.

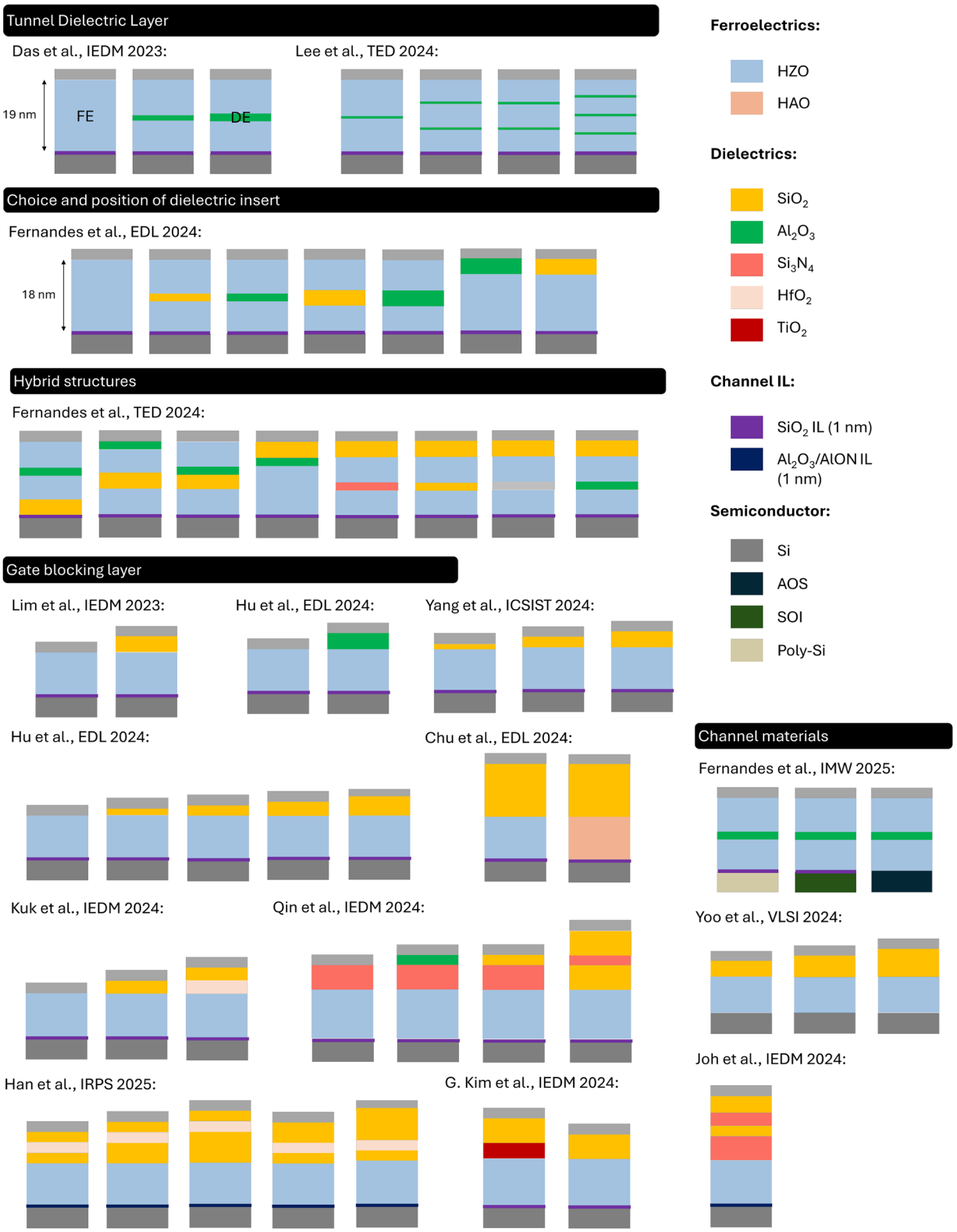

Figure 2. Insertion of dielectric (DE) has been shown to increase the memory window of the ferroelectric gate stack. The figure shows a summary of the most prominent works on gate stack engineering for FE-NAND.[18–32] It is worth noting the wide variety of materials used in the devices: ferroelectrics (HZO and HAO), dielectrics (SiO_2, Al_2O_3, Si_3N_4, HfO_2, and TiO_2), channel interlayers (ILs) (SiO_2 and Al_2O_3), and channel materials (bulk Si, poly-Si, silicon-on-insulator, amorphous oxide semiconductors).

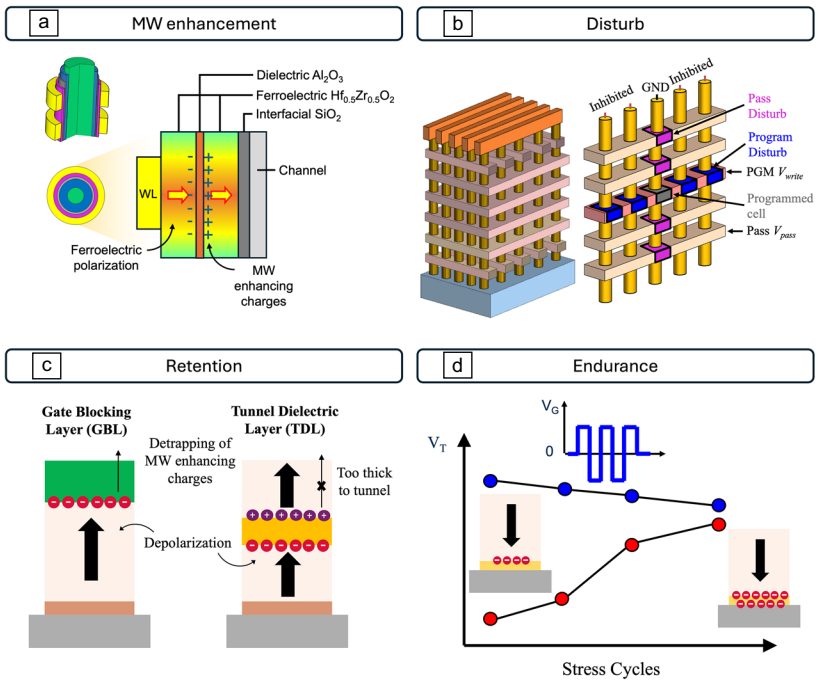

Figure 3. Engineering ferroelectric gate stacks for NAND applications largely involves four major challenges: (a) Memory window (MW) engineering: conventional ferroelectric gate stacks with only a ferroelectric layer exhibit low memory window (<3 V) even at 20-nm thicknesses.[18,19] The interplay between trap dynamics and polarization switching in ferroelectric field-effect transistors should be engineered carefully to achieve (b) disturb-free devices with (c) robust retention and (d) high write endurance. WL, word line; GND, ground; PGM, program.

Further, this article highlights the retention, endurance, and disturb challenges that come with the complicated coupling between traps and ferroelectric polarization. Understanding the interplay between trap dynamics and polarization switching will be essential to engineering large memory window devices for QLC or higher logic-level operation while meeting the specifications for retention, endurance, and disturb-free operation (**Figure** 3).

Engineering large memory window in FEFETs

Different geometries and material choices, especially for the dielectric insert, have been explored. The explored solutions largely fall into two categories depending on the location of the dielectric insert: (1) Tunnel dielectric layer (TDL)—dielectric is inserted in the middle of the ferroelectric gate stack, and (2) Gate blocking layer (GBL)—dielectric is inserted between the ferroelectric layer and the gate.

Figure 4a shows the enhancement in MW engineered by the insertion of a dielectric layer alongside the other components of a FE-NAND device, including the ferroelectric layer, channel interlayer, and channel materials resulting in memory windows as high as 19.4 V.[33]

The origin of these large MWs by using a dielectric insert is attributed to charge trapping at the ferroelectric–dielectric interface. In GBL, these charges enter the interface through gate-side injection.[18] While the origin of these MW enhancing charges is not known in the case of TDL-based FEFETs, they switch polarities by tunneling through the dielectric insert during polarization switching, hence the name, tunnel dielectric layer.[19] A detailed theoretical framework for MW enhancement was presented in Reference 19. A simpler and more commonly used analytical framework was presented by Lim et al.,[18] where the engineered memory window of these gate stacks is given by:

$$MW = \frac{(P_r - Q_{it})}{C_{FE}} + \frac{(Q'_{it} - Q_{it})}{C_{TDL/GBL}}$$

where, P_r is the remanent polarization and Q_{it} and Q'_{it} are the screening charge density at the FE–channel IL interface and the MW enhancing charge density at the FE-GBL/TDL interface.

The majority of recent studies focus on GBL-based FEFETs,[17,18,20–24] leveraging engineered gate stacks such as oxide/nitride/oxide (ONO) and high-k charge trap layers to optimize charge trapping and injection. For instance, GBL devices utilizing $SiO_2/HfO_2/SiO_2$ stacks have achieved record-high MWs of up to 19.4 V,[33] while Qin et al. reported a 16.05 V MW using an ONO charge-trapping layer.[22]

Additionally, amorphous oxide semiconductor (AOS) channels, such as oxygen-deficient IGZO, have been employed to further boost MWs. Yoo et al. demonstrated a 17.8 V MW with a total gate stack thickness of just 12 nm.[23] This remarkable performance in AOS-based GBL devices is attributed not only to efficient gate-side injection, but also to the absence of screening charges on the channel side, underscoring the critical role of gate stack and channel engineering in achieving ultrahigh MWs.

A series of publications from Fernandes et al. and Das et al. explored TDL-based FEFETs, optimizing the gate stack on two terminal ferroelectric MOSCAPs.[19,25,26,34,35] They identified that Al_2O_3 acted as the best TDL while SiO_2 was more suited as a GBL, in terms of achieving large MWs and higher ISPP/E slopes. Combining these insights, they demonstrated an 11-V MW on a hybrid gate stack 6/2(Al)/6/4(Si) with 2-nm Al_2O_3-TDL and 4-nm SiO_2-GBL. GBL devices, which enhance MWs by promoting gate-side charge injection at the FE–DE interface, have consistently demonstrated significantly higher MWs than TDL devices, although reports on TDL performance remain limited.

FEFETs have been known to have low write voltages compared to CTF NAND. While the insertion of the dielectric

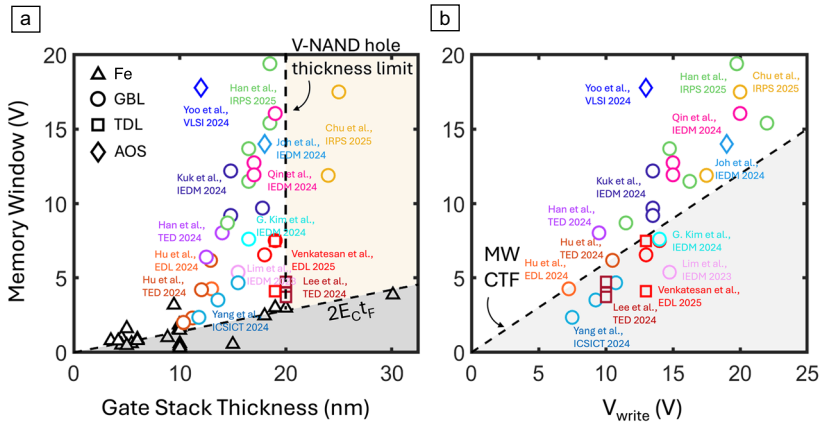

Figure 4. (a, b) Innovations over the past three years have resulted in the optimization of gate stacks to achieve ultrahigh MW, especially in GBL-type structures, (e.g., 16.05 V MW with the introduction of novel GBLs comprising of charge trap layers such as ONO[22] and a 17.8 V MW achieved by engineering the oxide semiconductor channels).[23] AOS, amorphous oxide semiconductor; CTF, charge trap flash.

layer to enable large MWs increases the write voltages, the engineered FEFETs achieve these large MWs at lower write voltages compared to their CTF counterparts, especially at ultrahigh MWs as shown in Figure 4b.

Reliability challenges in FE-NAND

While most of the initial efforts focused on achieving a large memory window, to enable broader adoption of the ferroelectric NAND, reliability challenges such as disturb, retention, and endurance need to be extensively characterized, modeled, and mitigated through device-, array- and system-level solutions.

Disturb

Pass disturb is a critical reliability concern in NAND. In a NAND array, a pass voltage is applied to turn on unaddressed cells while accessing a cell along the bit line (Figure 3). This pass voltage could disturb the V_T of the unaddressed cells. In ferroelectric NAND, in particular, a net electric field experienced by the ferroelectric gate stack is a combination of the pass voltage V_{pass} and the depolarization field E_{dep} due to the ferroelectric polarization. The origin of pass disturb depends on whether the cell is programmed or erased.

In the PGM state (state after positive write voltage), when the polarization is pointing towards the channel, E_{dep} and E_{pass} point in opposing directions. This prevents polarization backswitching but results in electron trapping, resulting in a positive shift in the threshold voltage. In most cases, disturb effects in the program state are observed to be significantly higher than those in the erase state (achieved by applying a negative write voltage), as demonstrated in the benchmark data shown in **Figure** 5a. Venkatesan et al. proposed and demonstrated a disturb mitigation scheme involving a periodic negative pulse to detrap the trapped electrons and reset the state of the cell as shown in Figure 5b–c.[27]

Contrary to this, in the ERS state, the amplification of the depolarization field due to the pass voltage increases the possibility of ferroelectric polarization backswitching. Ferroelectric gate stacks with large switching voltage and steep polarization switching have been proposed to mitigate polarization backswitching.[34] For instance, inserting a TiO_2 layer in the ferroelectric gate stack has been demonstrated to increase the steepness of polarization switching and reduce disturb in the ERS state significantly (Figure 5e).[28]

While the previously discussed methods focus on engineering the ferroelectric gate stack, Zhao et al. and Joh et al. proposed a dual-port FE-NAND array, including a dedicated gate for applying the pass voltage, thereby, eliminating pass disturb in its entirety as depicted in Figure 5f–h.[36,37]

Retention

As a long-term storage device, retention is a key reliability consideration for NAND devices. In conventional CTF NAND, charge loss due to detrapping through the oxide layers and lateral charge migration due to cell-to-cell coupling are the major contributors to retention loss. Ferroelectric NAND eliminates charge loss concerns by storing the data in the form of ferroelectric polarization. However, the introduction of trapped charges to enhance the MW of FEFETs has renewed retention concerns. Additionally, FE devices have previously not been leveraged for long-term storage solutions and lack extensive temperature-dependent retention characterization and modeling.

While early efforts achieved large MWs in FE gate stacks, retention loss, especially in GBL-based FEFETs, was high (between 25 and 50%). TDL-based FEFETs, however, were able to achieve robust retention while ensuring MW enhancement as shown in **Figure** 6a.[38] A detailed account on retention loss mechanisms and their dependence on the position of the dielectric insert was presented in Reference 39.

Additionally, it is worth noting that TDL-based FEFETs maintain a constant initial memory window across temperatures, while GBL-based FEFETs (including those with high-k inserts) show a lower initial MW at higher temperatures compared to room temperature. Future efforts aimed at improving the thermal stability of the threshold voltage and conducting extensive retention bake tests will be essential for engineering robust FE-NAND stacks (Figure 6b).

Kuk et al. demonstrated that such robust retention both at RT and 85°C could be achieved in GBL FEFETs with large MWs by inserting a high-k layer between the GBL and FE layers as

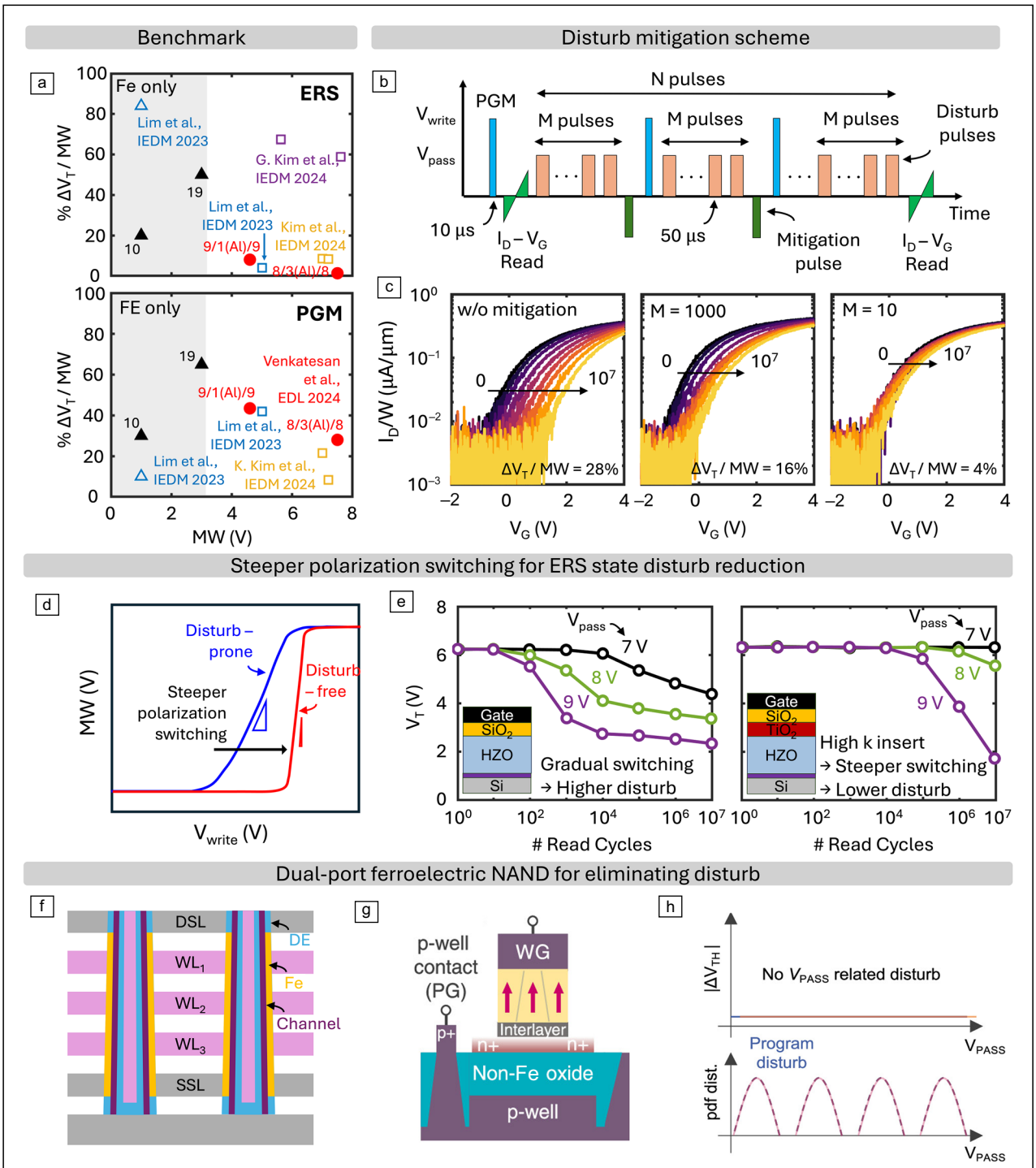

Figure 5. (a) A benchmark of the disturb in the erase (ERS) and program (PGM) states as a fraction of the total memory window (MW) shows significant pass disturb in the PGM state in FE-NAND devices. (b, c) Electron trapping was identified a key cause of positive V_T shift in the PGM state of large MW ferroelectric field-effect transistors (FEFETs) during read/disturb cycling. A mitigation scheme was proposed by Venkatesan et al. to detrap the electrons and enable 7× reduction in pass disturb.[27] Reprinted with permission from Reference 27. © 2024 IEEE. (d) In order to mitigate polarization backswitching, a steeper ISPP/E curve is suggested. (e) At a material level, using TiO_2 has been shown to improve the steepness of the polarization switching curves and thereby enable disturb-free operation up to 10k read cycles.[28] Adapted with permission from Reference 28. © 2024 IEEE. (f–h) At the array level, moving to a dual-port-based FE-NAND with a dedicated pass gate has been suggested as a potential solution to eliminating pass disturb.[36,37] Adapted with permission from Reference 36. © 2024 American Chemical Society. DSL, drain select line; WL, word line; SSL, source select line; DE, dielectric; PG, pass gate; WG, write gate.

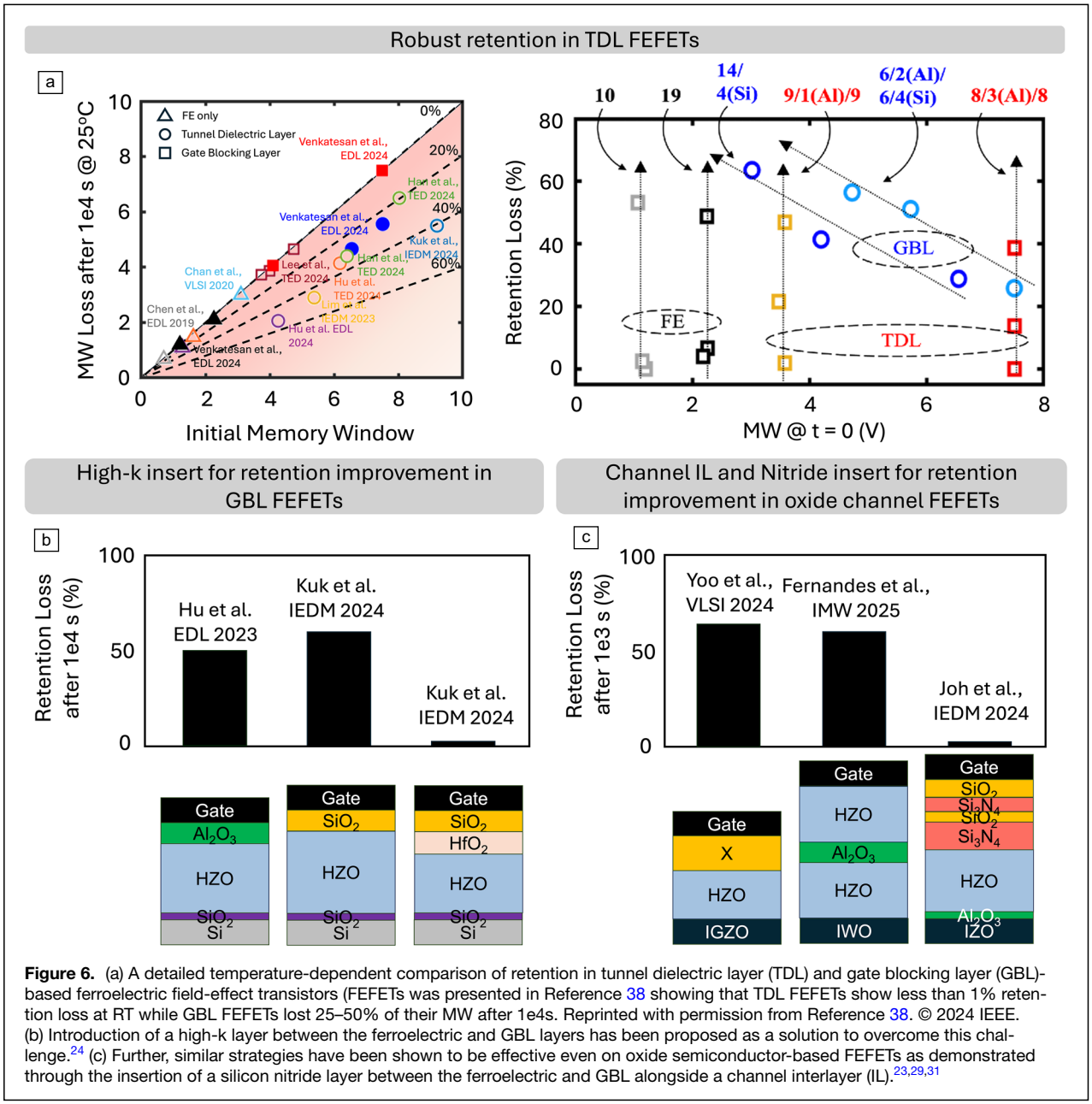

Figure 6. (a) A detailed temperature-dependent comparison of retention in tunnel dielectric layer (TDL) and gate blocking layer (GBL)-based ferroelectric field-effect transistors (FEFETs was presented in Reference 38 showing that TDL FEFETs show less than 1% retention loss at RT while GBL FEFETs lost 25–50% of their MW after 1e4s. Reprinted with permission from Reference 38. © 2024 IEEE. (b) Introduction of a high-k layer between the ferroelectric and GBL layers has been proposed as a solution to overcome this challenge.[24] (c) Further, similar strategies have been shown to be effective even on oxide semiconductor-based FEFETs as demonstrated through the insertion of a silicon nitride layer between the ferroelectric and GBL alongside a channel interlayer (IL).[23,29,31]

summarized in (Figure 6b).[24] Further, Joh et al. demonstrated a similar optimization of retention in FE-NAND devices with oxide semiconductor channels by inserting a nitride layer and a channel IL as summarized in (Figure 6c).[29] That said, the temperature-dependent variation of MW in GBL-based FEFETs remains a concern. Additionally, post-cycling retention in large MW FEFETs is yet to be investigated in detail.

Endurance

The strong interplay between trap dynamics and polarization switching in FEFETs has exacerbated endurance limitations. While write endurances lower than 10^{10} cycles would be a deal-breaker for DRAM and SRAM applications, traditional NAND storage is used for read-intensive applications and state-of-the-art NAND devices have write endurances around 100k cycles. Additionally, write endurance in conventional 3D NAND deteriorates significantly at high logic levels with QLC 3D NAND offering close to 1k cycles of write endurance. This results in a endurance-data density tradeoff impacting the application space of TLC and QLC 3D NAND.[3] In order to capture the tradeoff between the increasing data density and reducing write endurance, bytes written(BW) has been adopted as a performance metric by the industry.

While FEFETs, in general, achieve 10^5–10^6 write cycles endurance with record-high reports showing close to 10^{10} write

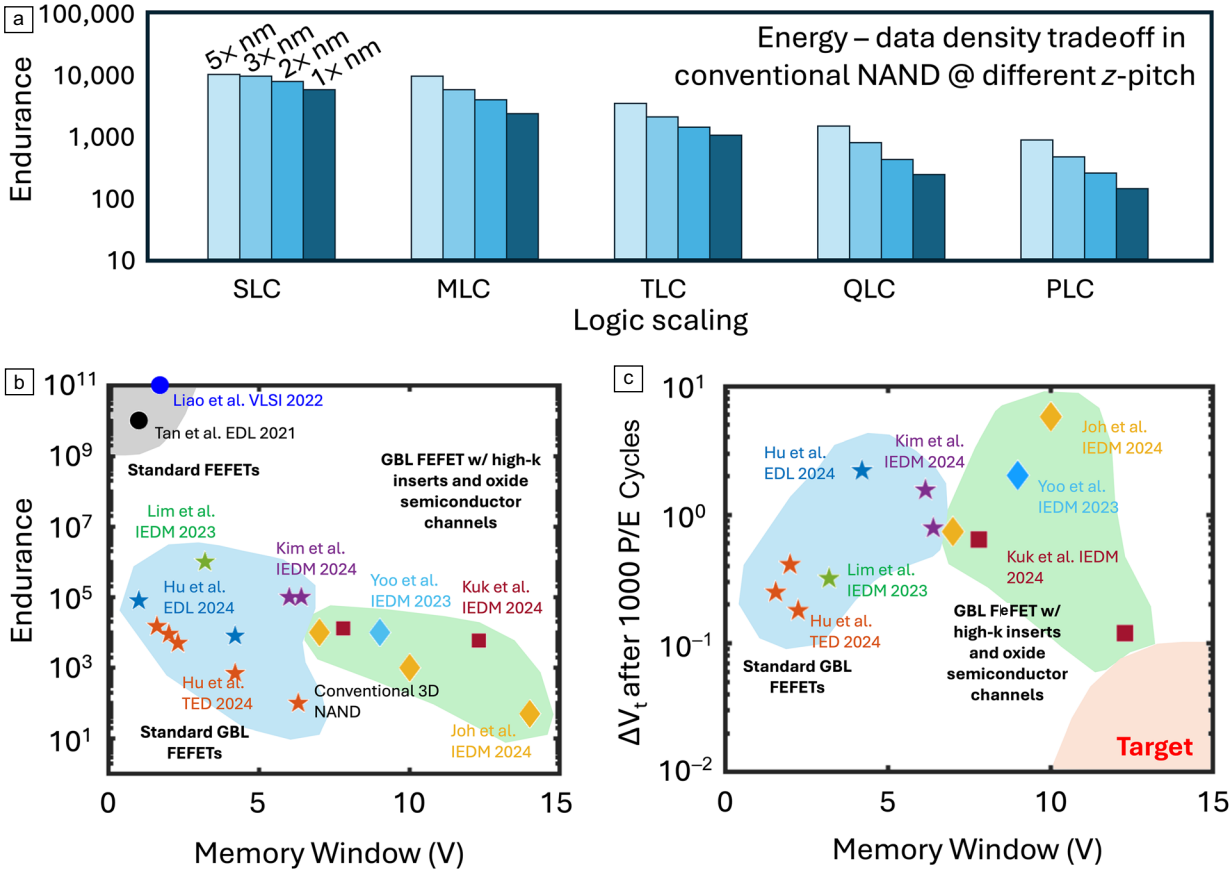

Figure 7. (a) While logic scaling and lower feature sizes have enabled exponential increase in data densities, conventional NAND suffers from rapidly degrading write endurance at higher logic level and lower feature sizes.[42] (b) Endurance in ferroelectric field-effect transistors (FEFETs) is largely governed by trapping at the FE-Channel interlayer (IL) interface leading to memory window (MW) closure. The less common form of MW degradation is a hard breakdown of the ferroelectric gate stack. However, the latter begins to dominate in FE-NAND devices with large MW and large write voltages. Usage of oxide semiconductors and inserting high-k layers between the FE and gate blocking layer (GBL) have enabled improved endurance even alongside MWs greater than 10 V. (c) However, the MW degrades during the program/erase (P/E) cycling before undergoing breakdown. This is undesirable especially in NAND devices that operate at high logic level (QLC, PLC, and higher).[18,20,21,23,24,29,40,41,43] QLC, quad-level cell; PLC, penta-level cell.

cycles, these devices undergo fatigue through their lifetime (i.e., V_T shifts), eventually leading to MW closure.[40,41] Further, the high voltage operation (closer to the breakdown voltage of the gate stack) compared to standard FEFETs has further degraded the endurance of NAND-compatible FEFETs. That said, significantly higher write endurance compared to conventional NAND has been achieved in large MW FE-NAND devices with Kuk et al. demonstrating ~6k cycles write endurance with a 12.3 V MW.[24] The cycles to breakdown for different large MW FEFETs has been summarized in **Figure** 7. Further engineering of the ferroelectric gate stack, channel interlayer and channel alongside novel write schemes is required to achieve degradation-free FE-NAND endurance for use in QLC and PLC compatible FE-NAND.

Alongside endurance, the interplay between trap dynamics and polarization switching leads to the requirement of a read-after-write delay for detrapping the trapped charges. This read-after-write delay worsens with P/E cycling due to the generation of deeper and slower traps in the channel IL.[44] However, Ma et al. demonstrated that leveraging gate-side injection by the insertion of a gate blocking layer could not only increase the memory window, but also enable immediate read-after-write operation.[45]

Ferroelectric-assisted CTF

As previously discussed, FEFETs offer a promising solution to overcome the challenges faced by incumbent CTF NAND. However, disturb, retention, and endurance concerns need to be resolved before FEFETs can replace CTF NAND. Ferroelectric-assisted CTF has been proposed as an intermediate solution.[46–50]

In FE-CTF devices, a ferroelectric layer is integrated adjacent to the charge-trapping nitride layer. This hybrid design enhances charge trapping via polarization-assisted carrier injection and stabilization, which can result in larger MWs and improved logic-level operation. These devices retain the familiar CTF program/erase scheme while leveraging ferroelectric effects to improve performance.

Recent studies have shown that incorporating ferroelectric layers improves not only the MW but also retention and program efficiency. For example, Breuil et al. and Higashi et al. reported enhanced retention and faster program speeds in FE-CTF devices compared to baseline CTF designs.[49,50]

Although FE-CTF devices may not fully match the scaling potential of FE-NAND, they could serve an intermediate solution offering incremental improvements in performance and reliability. To that end, FE-CTF represents a practical step toward bridging current CTF technology with emerging FE-NAND architectures.

Alternate ferroelectrics

While hafnia-based ferroelectrics currently dominate research for 3D NAND due to their CMOS compatibility, high coercive fields, and scalability, other material classes are also being explored to address specific performance or reliability gaps. Perovskite ferroelectrics such as $PbZr_xTi_{1-x}O_3$ and $SrBi_2Ta_2O_9$ offer inherently low coercive fields that enable highly energy-efficient single-bit operation, but this same property limits their suitability for multilevel storage. In addition, their lack of CMOS process compatibility and the integration challenges they pose severely restrict their use in vertical NAND process flows.[51–53]

Nitride ferroelectrics, including AlScN and AlBN, exhibit exceptionally high coercive fields (3–5 MV/cm) and could support large MW operation without the need for dielectric inserts.[54] With continued advances in materials engineering and process optimization, it could be possible to fine-tune the tradeoff between memory window and breakdown field-to-coercive field ratio, positioning these nitrides as candidates for specialized, high-performance NAND solutions.

By comparison, hafnia-based ferroelectrics provide the most balanced pathway forward—offering process compatibility, scalability, and a high coercive field. The incorporation of dielectric inserts further enhances their coercive voltage and, in turn, their memory window, making them particularly well suited to overcome the scaling and reliability challenges of next-generation 3D NAND.

Conclusion

Today, NAND flash memory stands as a cornerstone of modern data-storage solutions, powering everything from consumer electronics to enterprise storage systems. However, as AI applications continue to expand, the rising demand for high-capacity, low-latency memory is pushing traditional CTF technologies to their limits. The integration of ferroelectric materials into 3D NAND technology offers a compelling pathway to overcome reliability constraints and extend 3D NAND scaling. Ferroelectric NAND with engineered gate stacks promises multibit operation while offering enhanced reliability, low power consumption, and improved data density. This positions them as strong contenders for high-density, energy-efficient 3D NAND with a potential to enable penta-level operation with more than one thousand layers and data densities greater than 100 Gb/mm^2.

Author contributions

The manuscript was written by P.V. with contributions from all authors.

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Data availability

Not applicable.

Conflict of interest

On behalf of all authors, the corresponding author states that there is no conflict of interest.

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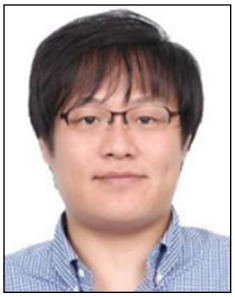

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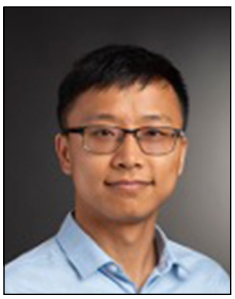

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