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An Approach to Control Multilevel Flying-Capacitor Converters Using Optimal Dynamic Programming Benchmark

Davide Tebaldi 

Department of Engineering Enzo Ferrari, University of Modena and Reggio Emilia, Via Pietro Vivarelli 10, 41125 Modena, Italy; davide.tebaldi@unimore.it

Abstract: The problem of balancing capacitor voltages is of utmost importance in multilevel converter topologies involving flying capacitors. In this study, a new minimum angular distance (MAD) algorithm is proposed to control the turning on and off of the switches, ensuring fast convergence of the capacitor voltages balancing problem in multilevel flying-capacitor converters. This algorithm was developed based on a preliminary analytical analysis of the capacitor voltage trajectories using the power-oriented model of the converter. Compared to other approaches, the proposed algorithm involves only simple and well-defined calculations, requires no training, and does not require any prediction of future values that the output current assumes. The proposed algorithm, implemented in the MATLAB/Simulink environment, is proven to give very good performance, verified against an optimal benchmark given by dynamic programming, in terms of capacitor voltages convergence time, efficiency, power loss, and total harmonic distortion.

Keywords: modeling; control applications; simulation; power systems; multilevel flying-capacitor converters; dynamic programming



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1. Introduction

Electrical power conversions find several applications, including power grids [1], the control [2] of electric machines [3], electric vehicles [4], and many others. Power converters can be mainly classified into DC/DC [4–6], AC/DC [7], DC/AC [8], and AC/AC converters [9–11]. Strong research interest resides in multilevel converters thanks to the many advantages they offer over two-level converters [12,13]. The multilevel converter topologies available in the literature include modular converters [14], H-bridge converters [15], and flying-capacitor converters [8].

In order to study the considered converter topology, the modeling step is the first to be addressed, as shown in [16] for switched systems. The modeling of cascaded H-bridge multilevel inverters is addressed in [15] using Kirchhoff's laws, whereas the modeling of modular multilevel converters is addressed in [17] using a state-space approach. In [18], the authors address the modeling of the considered DC microgrid by providing the differential equations describing it, whereas an effective approach for modeling multilevel flying-capacitor converters is proposed in [8] using the Power-Oriented Graphs modeling technique [19,20]. The next important step to be addressed is converter control [21], both for DC/DC and for AC/DC–DC/AC converters. The optimal control of buck converters is addressed in [22] with the objective of keeping the output voltage as close to the desired setpoint as possible. Weighted model predictive control is applied to modular multilevel converters in [23], whereas an approach for controlling multilevel flying-capacitor converters with varying numbers of output voltage levels is proposed in [8]. When working

with converter topologies involving floating capacitors, a particularly delicate aspect is the capacitor voltages balancing issue [24,25] in order to have a proper output voltage waveform. Different approaches are available in the literature to guarantee the balancing of capacitor voltages, which can vary from different modulation techniques [25–27] to the use of closed-loop techniques [28–31]. A new pulse width modulation (PWM) method was proposed in [25], while Phase Disposition PWM (PDPWM) is proposed in [26]. A modified version of Carrier-Redistribution PWM (CRPWM) was employed in [27] instead, allowing low voltage ripple and low harmonic content in the output voltage. On the other hand, closed-loop methods have the advantage of being more robust against undesired situations such as faults [8], for example. A closed-loop approach for capacitor voltages balancing is proposed in [28], introducing a dedicated control signal that modifies the duty cycle generated through modulation, while a deadband-based method is proposed in [29]. Other available closed-loop approaches can foresee the use of a proportional-integral controller [30] to achieve capacitor voltage balancing or a cost function to be minimized [31]. A common closed-loop approach for controlling power converters is model predictive control (MPC) [32]. As an example, in [33] the authors use an MPC variant to minimize a cost function using several criteria, including output voltage tracking and capacitor voltages balancing. However, this approach requires the prediction of the future values that the output current assumes. Furthermore, whenever a cost function needs to be minimized, the choice of weighting factors comes into play, which is generally not trivial. MPC is also used in [34] to minimize a cost function, involving output current tracking and capacitor voltages. Even in this case, however, output current prediction is required, and the weighting factors tuning problem was addressed by finding the proper weighting factors experimentally to minimize the total harmonic distortion. A switching control law is proposed in [35] instead, in order to achieve output voltage control and flying-capacitor voltages balancing in a four-level flying-capacitor converter. In [36], an artificial neural network was used to control a multilevel flying-capacitor inverter instead. The neural network was trained using data from the inverter controlled by MPC to achieve capacitor voltages balancing and output current tracking. However, the neural network training process is no easy task, as the input features need to be chosen. The use of neural networks is indeed becoming popular in several engineering applications, including power electronics [37] for applications such as capacitor voltages estimation [38] and converter control [36,39]. As an example, an artificial neural network is employed in [38] for capacitor voltages estimation, and a deep neural network is used in [39] to control multilevel flying-capacitor converters after a training phase from converter operations controlled using MPC. However, the difficulty in these approaches is represented by the training phase, where the right number of samples must be chosen in order to avoid, for example, underfitting or overfitting problems.

In the present paper, multilevel flying-capacitor converters (MFCCs) are the subject of study. A new control algorithm is proposed, handling the turning on and off of the switches to ensure fast convergence regarding the capacitor voltages balancing problem. The proposed control algorithm has the beneficial properties of being effective and simple to implement, as it is based on the calculation of the angular distance between vectors. Specifically, the work in [8] is extended with the following contributions with respect to the literature:

- (1) A detailed analysis of the converter dynamics, with specific emphasis on the IGBT (Insulated Gate Bipolar Transistor) signals' impact on the evolution of the capacitor voltage trajectories, with the objective of proposing the new algorithm at the next point;
- (2) a new minimum angular distance (MAD) control algorithm is proposed. The algorithm handles the turning on and off of the switches to ensure the fast balancing of capacitor voltages in multilevel flying-capacitor converters with a generic number n of capacitors.

The proposed MAD algorithm exhibits the following features: it involves very simple and well-defined calculations and does not require any training or prediction regarding future values that the output current assumes. The proposed algorithm is causal and implementable in real time. Furthermore, it can be applied to multilevel flying capacitor converters with a generic number n of capacitors, and it is proven to exhibit convergence times and performance in terms of efficiency, power loss, and total harmonic distortion (THD) which are very close to those provided by the considered optimal benchmark; (3) the statement and the description of the optimal control problem aiming at achieving balanced capacitor voltages condition. The optimal control sequence of the IGBTs states allowing the obtainment of such conditions, while generating the desired output voltage, is found using dynamic programming (DP) [40,41]. The latter approach requires a priori knowledge of the converter cycle, which makes it noncausal and not implementable in real time. However, DP represents an optimal benchmark candidate for evaluating the performance of the proposed MAD algorithm. Dynamic programming is used to generate the optimal benchmark because it is a well-established method to achieve the optimal solution given by Bellman’s Principle of Optimality [40]; (4) the evaluation of the good performance of the MAD algorithm by comparing the obtained results with those given by the DP optimal benchmark in terms of capacitors voltages convergence time, efficiency, power loss, and output voltage total harmonic distortion (THD).

The remainder of this paper is organized as follows. The converter modeling, voltage trajectories dynamic analysis, and converter control using the MAD algorithm are addressed in Section 2, Section 3, and Section 3.1, respectively. The optimal control problem is stated in Section 3.2, whereas a comparison of the results between the MAD algorithm and DP is addressed in Section 4. Finally, the conclusions are reported in Section 5.

2. Converter Modeling

The circuital representation of the n -dimensional multilevel flying-capacitor converter used for the proposed analysis is shown in Figure 1. This converter can be modeled as [8]:

$$\begin{cases} \mathbf{C}\dot{\mathbf{V}}_c = \mathbf{A}\mathbf{V}_c + \begin{bmatrix} \mathbf{B} & -\mathbf{S}_j^T \end{bmatrix} \mathbf{u}, \\ \mathbf{y} = \begin{bmatrix} -\mathbf{B}^T \\ \mathbf{S}_j \end{bmatrix} \mathbf{V}_c + \mathbf{D}\mathbf{u}, \end{cases} \quad \mathbf{C} = \begin{bmatrix} \mathbf{C}_1 & 0 & \cdots & 0 \\ 0 & \mathbf{C}_2 & \cdots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \cdots & \mathbf{C}_n \end{bmatrix}, \quad (1)$$

$$\mathbf{A} = \begin{bmatrix} \frac{-1}{R_{in}} & 0 & \cdots & 0 \\ 0 & 0 & \cdots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \cdots & 0 \end{bmatrix}, \quad \mathbf{V}_c = \begin{bmatrix} V_1 \\ V_2 \\ \vdots \\ V_n \end{bmatrix}, \quad \mathbf{S}_j^T = \begin{bmatrix} s_1 \\ s_2 \\ \vdots \\ s_n \end{bmatrix}, \quad \mathbf{B} = \begin{bmatrix} 1 \\ R_{in} \\ \vdots \\ 0 \end{bmatrix},$$

$$\mathbf{D} = \begin{bmatrix} \frac{1}{R_{in}} & 0 \\ 0 & 0 \end{bmatrix}, \quad \mathbf{y} = \begin{bmatrix} I_{in} \\ V_{out} \end{bmatrix}, \quad \mathbf{u} = \begin{bmatrix} V_{in} \\ I_{out} \end{bmatrix},$$

where \mathbf{C} and \mathbf{A} are the system energy matrix and the system power matrix, respectively, \mathbf{V}_c , \mathbf{u} , and \mathbf{y} are the system state, input and output vectors, respectively, and n is the number of capacitors in the converter. Vector $\mathbf{S}_j \in \mathbb{R}^{(1 \times n)}$ in (1) is called configuration vector. The state-space model (1) of the considered flying-capacitor multilevel converter can be equivalently represented using the Power-Oriented Graphs (POG) block scheme in Figure 2 [8]. The vertical dashed lines in the figure are named power sections and describe the power flows within the considered flying-capacitor multilevel converter. The first elaboration block in Figure 2 describes the input resistance, while the second elaboration block describes the capacitor dynamics. The first connection block in Figure 2 describes the

interaction between the resistive and capacitive parts of the converter, while the second connection block describes the interaction of the converter with the external world, that is, with the load. The horizontal arrows located at the top of each power section describe the positive direction of the power flows exchanged from one section to the next. When used as a DC/AC converter, $P_{in} > 0$, $P' = P'' > 0$ and $P''' = P_{out} > 0$ hold. Either the condition $P' = P'' > P''' = P_{out}$ or the condition $P' = P'' < P''' = P_{out}$ can be verified depending on the configuration vector \mathbf{S}_j , which will act to either recharge or discharge the capacitors C_1, \dots, C_n , as is further discussed in Section 3. Figure 2 shows that the power dissipation in the considered system takes place because of the input resistance R_{in} . Therefore, the system's average efficiency \bar{E} and average power loss \bar{P}_l can be defined as:

$$\bar{E} = \frac{\bar{P}'}{\bar{P}_{in}} \quad \text{and} \quad \bar{P}_l = \bar{P}_{in} - \bar{P}' \tag{2}$$

when the converter performs a DC/AC conversion, where $\bar{P}_{in} = \text{mean}(P_{in})$ and $\bar{P}' = \text{mean}(P')$.

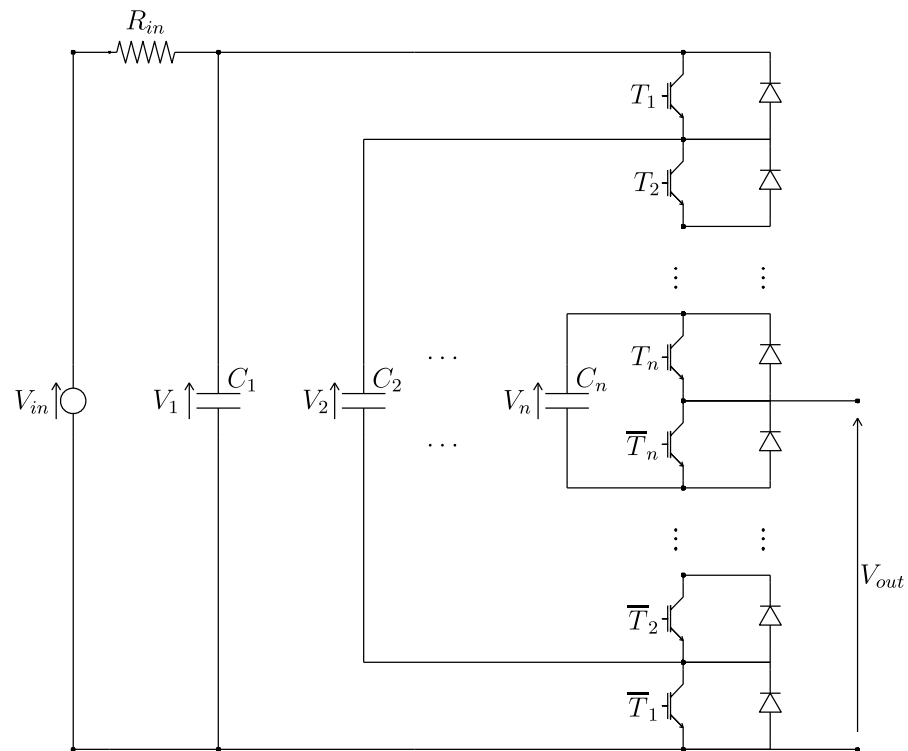


Figure 1. Circuitual representation of the considered n -dimensional MFCC.

Vector \mathbf{S}_j in (1) is in one-to-one correspondence with the IGBT signal vector \mathbf{T}_j through the following property [8]:

Property 1. The components $s_i \in \{-1, 0, 1\}$ of the configuration vector $\mathbf{S}_j = [s_1 \ s_2 \ \dots \ s_n]$ can be obtained from the components $T_i \in \{0, 1\}$ of the IGBT signal vector $\mathbf{T}_j = [T_1 \ T_2 \ \dots \ T_n]$ as follows:

$$s_i = \begin{cases} T_1 & \text{if } i = 1, \\ \bar{T}_{i-1} T_i - T_{i-1} \bar{T}_i & \text{if } i \in \{2, \dots, n\}. \end{cases} \tag{3}$$

The index $j \in \{0, 1, \dots, 2^n - 1\}$ identifies all the different 2^n combinations that the IGBT signals can assume. The study reported in [8] indicates that a different number $m = n + 1 \dots 2^n$ of output voltage levels can be obtained by properly choosing the desired

reference values for the capacitor voltages. In the case of $n = 3$, the converter operates in the so-called basic mode, generating $m = 4$ output voltage levels if the capacitors' voltages are controlled to the following desired reference values:

$$\mathbf{V}_{c_d} = [V_{1_d} \ V_{2_d} \ V_{3_d}]^T = [V_{in} \ \frac{2V_{in}}{3} \ \frac{V_{in}}{3}]^T, \tag{4}$$

where V_{in} is the DC input voltage, as shown in Figure 1. The resulting output voltage levels are shown in Table 1.

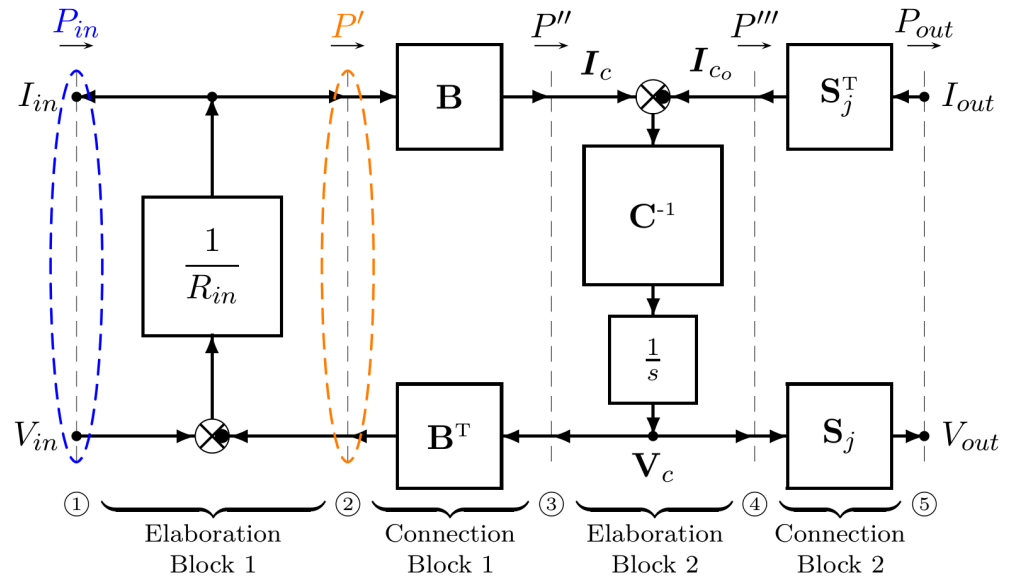


Figure 2. Power-Oriented Graphs block scheme of system (1).

Table 1. Switching table relating the IGBT signals to the values of the output voltage V_{out} when $n = 3$.

\mathbf{T}_j	T_1	T_2	T_3	V_{out} (if (4) holds)	Level
\mathbf{T}_0	0	0	0	0	L_0
\mathbf{T}_1	0	0	1	$V_3 = \frac{V_{in}}{3}$	L_1
\mathbf{T}_2	0	1	0	$V_2 - V_3 = \frac{V_{in}}{3}$	L_1
\mathbf{T}_3	0	1	1	$V_2 = \frac{2V_{in}}{3}$	L_2
\mathbf{T}_4	1	0	0	$V_1 - V_2 = \frac{V_{in}}{3}$	L_1
\mathbf{T}_5	1	0	1	$V_1 - V_2 + V_3 = \frac{2V_{in}}{3}$	L_2
\mathbf{T}_6	1	1	0	$V_1 - V_3 = \frac{2V_{in}}{3}$	L_2
\mathbf{T}_7	1	1	1	$V_1 = V_{in}$	L_3

Discrete-Time Model

The set of state transition equations in (1) can be rewritten as

$$\dot{\mathbf{V}}_c = \underbrace{\mathbf{C}^{-1}\mathbf{A}}_{\mathbf{A}} \mathbf{V}_c + \underbrace{\mathbf{C}^{-1}[\mathbf{B} \ -\mathbf{S}_j^T]}_{\mathbf{B}} \mathbf{u}, \tag{5}$$

where vectors $\mathbf{V}_c, \mathbf{B}, \mathbf{S}_j, \mathbf{u}$ and matrices \mathbf{A}, \mathbf{C} are defined in (1).

In the case of $n = 3$, matrices $\bar{\mathbf{A}}$ and $\bar{\mathbf{B}}$ in (5) assume the following form:

$$\bar{\mathbf{A}} = \begin{bmatrix} -\frac{1}{C_1 R_{in}} & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix}, \quad \bar{\mathbf{B}} = \begin{bmatrix} \frac{1}{C_1 R_{in}} & -\frac{s_1}{C_1} \\ 0 & -\frac{s_2}{C_2} \\ 0 & -\frac{s_3}{C_3} \end{bmatrix}, \quad (6)$$

and Equations (5) and (6) can be discretized into the following matrix difference equation:

$$V_c(k+1) = \mathbf{F}V_c(k) + \mathbf{G}u(k), \quad \mathbf{F} = e^{\bar{\mathbf{A}}T_s}, \quad \mathbf{G} = \int_0^{T_s} e^{\bar{\mathbf{A}}\sigma} \bar{\mathbf{B}} d\sigma,$$

$$\mathbf{F} = \begin{bmatrix} e^{-\frac{T_s}{C_1 R_{in}}} & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}, \quad \mathbf{G} = \begin{bmatrix} 1 - e^{-\frac{T_s}{C_1 R_{in}}} & -s_1 R_{in} \left(1 - e^{-\frac{T_s}{C_1 R_{in}}}\right) \\ 0 & -\frac{T_s s_2}{C_2} \\ 0 & -\frac{T_s s_3}{C_3} \end{bmatrix}, \quad (7)$$

where T_s is the sampling time.

3. Converter Control

The set of state transition equations in (1) can be rewritten as [8]:

$$\dot{V}_c = \mathbf{C}^{-1} \mathbf{A} V_c - \underbrace{\mathbf{C}^{-1} \mathbf{S}_j^T}_{\tilde{\mathbf{S}}_j^T} I_{out} + \mathbf{C}^{-1} \mathbf{B} V_{in}, \quad (8)$$

where $\tilde{\mathbf{S}}_j$ represents a new version of the configuration vector \mathbf{S}_j , in which the i -th component of \mathbf{S}_j has been normalized with respect to the i -th capacitance C_i . Since the value of the input resistance R_{in} is typically very low [8], from the first equation in (8) it can be evinced that $V_1 \simeq V_{in}$, meaning that the number of capacitor voltages to be controlled changes from n to $n - 1$. Therefore, a reduced version $\tilde{\mathbf{s}}_j$ of the configuration vector $\tilde{\mathbf{S}}_j$ can be introduced:

$$\tilde{\mathbf{s}}_j = [s_2/C_2 \cdots s_n/C_n]. \quad (9)$$

From the reduced vector $\tilde{\mathbf{s}}_j$, the reduced configuration vector \mathbf{s}_j can be defined as follows:

$$\mathbf{s}_j = \tilde{\mathbf{s}}_j / \|\tilde{\mathbf{s}}_j\|, \quad (10)$$

which will be called control vector \mathbf{s}_j hereafter. For the case of $n = 3$, all the possible control vectors \mathbf{s}_j that can be obtained from all the possible IGBT signal vectors \mathbf{T}_j in Table 1 can be found using (3), (9), and (10) as follows:

$$\begin{bmatrix} \mathbf{T}_0 \\ \mathbf{T}_1 \\ \mathbf{T}_2 \\ \mathbf{T}_3 \\ \mathbf{T}_4 \\ \mathbf{T}_5 \\ \mathbf{T}_6 \\ \mathbf{T}_7 \end{bmatrix} = \begin{bmatrix} 000 \\ 001 \\ 010 \\ 011 \\ 100 \\ 101 \\ 110 \\ 111 \end{bmatrix} \Leftrightarrow \begin{bmatrix} \mathbf{s}_0 \\ \mathbf{s}_1 \\ \mathbf{s}_2 \\ \mathbf{s}_3 \\ \mathbf{s}_4 \\ \mathbf{s}_5 \\ \mathbf{s}_6 \\ \mathbf{s}_7 \end{bmatrix} = \begin{bmatrix} 0 & 0 \\ 0 & 1 \\ \frac{1}{C_2 \|\tilde{\mathbf{s}}_2\|} & -\frac{1}{C_3 \|\tilde{\mathbf{s}}_2\|} \\ 1 & 0 \\ -1 & 0 \\ -\frac{1}{C_2 \|\tilde{\mathbf{s}}_5\|} & \frac{1}{C_3 \|\tilde{\mathbf{s}}_5\|} \\ 0 & -1 \\ 0 & 0 \end{bmatrix}. \quad (11)$$

Remark 1. From (8)–(10), and recalling that $V_1 \simeq V_{in}$, it can be observed that

$$\dot{V}_i = -\mathbf{s}_j \|\tilde{\mathbf{s}}_j\| I_{out}, \quad \text{for } i = 2, \dots, n, \quad (12)$$

meaning that the trajectory of the reduced voltage vector $\mathbf{v}_c = [V_2 \dots V_n]^T$ moves in the $n - 1$ dimensional state-space (V_2, \dots, V_n) in the direction specified by the control vector \mathbf{s}_j when $I_{out} < 0$, and it moves in the opposite direction when $I_{out} > 0$. The distance covered by the reduced voltage vector $\mathbf{v}_c = [V_2 \dots V_n]^T$ is given by $\|\tilde{\mathbf{s}}_j\| |I_{out}|$.

A graphical representation of the direction imposed on the trajectory of the reduced voltage vector $\mathbf{v}_c = [V_2 \ V_3]^T$ by the control vectors $\mathbf{s}_0, \mathbf{s}_1, \mathbf{s}_2, \mathbf{s}_3, \mathbf{s}_4, \mathbf{s}_5, \mathbf{s}_6$, and \mathbf{s}_7 in the state-space (V_2, V_3) for $n = 3$ is shown in Figure 3, assuming the following ratios between the capacitors values [8]:

$$C_1 = \frac{C_3}{3}, \quad C_2 = \frac{C_3}{2}, \quad C_3. \quad (13)$$

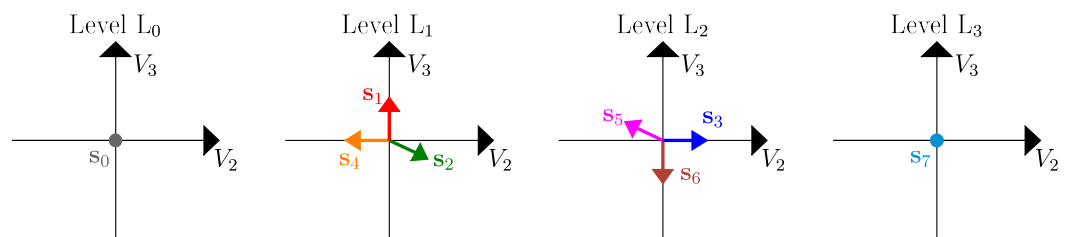


Figure 3. Control vectors \mathbf{s}_j for $j \in \{0, 1, \dots, 2^n - 1\}$ on the plane (V_2, V_3) in the case of $n = 3$.

From (11), (12), Table 1, and Figure 3, it can be observed that: (1) when the levels L_0 or L_3 need to be generated, the trajectory of the reduced voltage vector \mathbf{v}_c does not move since the control vectors \mathbf{s}_0 or \mathbf{s}_7 are null; (2) when the levels L_1 or L_2 need to be generated, the direction of (and the distance covered by) the trajectory of the reduced voltage vector \mathbf{v}_c depend on the control vector that is used: $\mathbf{s}_1, \mathbf{s}_2$, or \mathbf{s}_4 for level L_1 , and $\mathbf{s}_3, \mathbf{s}_5$, or \mathbf{s}_6 for level L_2 .

3.1. Proposed Minimum Angular Distance (MAD) Control

Let $V_{out,d}$ be the desired sinusoidal profile for the output voltage V_{out} indicated in Figure 1, let T_{PWM} be the pulse width modulation period, let δ be the duty cycle, and let t_k be the current time instant. Let V^- and V^+ be the two voltage values associated with the lower and upper levels L^- and L^+ , between which voltage $V_{out,d}$ falls within the T_{PWM} period. The desired output voltage level L within each T_{PWM} period is given by:

$$L = \begin{cases} L^- & \text{for } [t_k, t_k + \delta T_{PWM}) \\ L^+ & \text{for } [t_k + \delta T_{PWM}, t_k + T_{PWM}) \end{cases}. \quad (14)$$

Let $\mathbf{v}_{c,d} = [V_{2,d} \dots V_{n,d}]^T$ be the desired reference for the reduced voltage vector \mathbf{v}_c introduced in Remark 1, and let $\Delta_{\mathbf{v}_c} = \mathbf{v}_c - \mathbf{v}_{c,d}$ be the reduced voltage error vector, which will be called the error vector hereafter. The proposed MAD algorithm, reported in Algorithm 1 in a Matlab-like form, aims to select the best control vector \mathbf{s}_j to: (1) generate the desired output voltage level L given by (14); (2) keep the error vector $\Delta_{\mathbf{v}_c}$ as close as possible to zero:

$$\text{select } \mathbf{s}_j \text{ such that } \begin{cases} L_{\mathbf{s}_j} = L, \\ \|\Delta_{\mathbf{v}_c}\| \text{ is minimized,} \end{cases} \quad (15)$$

where L_{s_j} is the output voltage level generated by using the control versor s_j . The MAD algorithm is executed every switching period T_s , where T_s is a proper fraction of T_{PWM} and where $f_s = 1/T_s$ is the IGBT switching frequency. The MAD algorithm proposed in Algorithm 1 works for a generic n -dimensional multilevel flying-capacitor converter. The block diagram of the control architecture is shown in Figure 4.

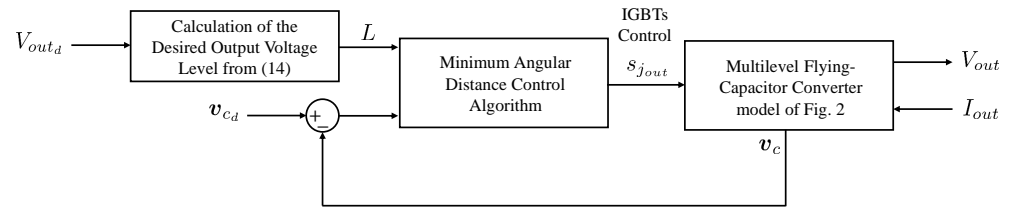


Figure 4. Block diagram of the control architecture.

Every switching period T_s , the function $s_{j,out} = \mathbf{MAD}(\Delta_{v_c}, I_{out}, L)$ in Algorithm 1 is called. The latter takes (as input) the current values of the error vector Δ_{v_c} , the load current I_{out} , and the desired output voltage level L . The control function produces (as output) the control versor $s_{j,out}$ to be engaged over the next switching period $[t_k, t_k + T_s)$. The control versor $s_{j,out}$ directly determines the IGBTs turn-on/off control signals through Property 1, (9), and (10); therefore, the MAD algorithm directly handles the turning on and off of the switches.

Algorithm 1 Matlab-like form of the minimum angular distance algorithm.

```

function  $s_{j,out} = \mathbf{MAD}(\Delta_{v_c}, I_{out}, L)$ 
1. if  $\|\Delta_{v_c}\| > 0$ 
2.    $\delta_{v_c} = \Delta_{v_c} / \|\Delta_{v_c}\|;$ 
3. else
4.    $\delta_{v_c} = \Delta_{v_c};$ 
5. end
6. if  $I_{out} < 0$ 
7.    $\delta_{v_c} = -\delta_{v_c};$ 
8. end
9.  $\varphi = \infty;$ 
10. for  $j = 0 : 2^n - 1$ 
11.   Determine the voltage level  $L_{s_j}$  generated
12.   by  $s_j$  using (12) and Table 1;
13.   if  $L_{s_j} == L$ 
14.      $\varphi_j = \arccos(s_j \cdot \delta_{v_c});$ 
15.     if  $\varphi_j < \varphi$ 
16.        $\varphi = \varphi_j;$ 
17.        $s_{j_o} = s_j;$ 
18.     end
19.   end
20. end

```

The MAD algorithm in Algorithm 1 works as described in the following. From line 1 to line 5, the error vector Δ_{v_c} is normalized into δ_{v_c} , which is called the error versor since it represents a versor in the state-space (V_2, \dots, V_n) . From line 6 to line 8, the sign of current I_{out} is checked. If $I_{out} < 0$, the sign of the error versor δ_{v_c} is changed because the direction imposed by the control versor s_j is reversed in this case, as shown in Remark 1. A cycle over all the control versors s_j is then performed from line 10 to line 20. Out of all the control versors s_j such that $L_{s_j} = L$, the one exhibiting the minimum angular distance φ_j from the error versor δ_{v_c} is picked, where the angular distance φ_j can be computed by recalling

the definition of the scalar product between two versors s_j and δ_{v_c} : $s_j \cdot \delta_{v_c} = \cos(\varphi_j)$. The reason for this choice can be understood by referring to the scenario depicted in Figure 5 in the case of $n = 3$, as an example. In this scenario, the trajectory of the reduced voltage vector $v_c = [V_2 \ V_3]^T$ moves in the state-space (V_2, V_3) . The desired output voltage level L from (14) is supposed to be level L_1 : the available control versors s_j that can be picked are, therefore, s_1 , s_2 , and s_4 ; see Figure 3. In the example of Figure 5, the current value of the error vector $\Delta_{v_c}(t_k)$ is supposed to be the one depicted by the black dashed line, whereas the corresponding current value of the error versor $\delta_{v_c}(t_k)$ is the one depicted by the yellow line. In this situation, it can be observed that the control versor s_j having the minimum angular distance φ_j from the error versor $\delta_{v_c}(t_k)$ is s_1 , exhibiting the angular distance φ_1 encircled in black in the figure, from the error versor $\delta_{v_c}(t_k)$. The reason why s_1 is the right choice can be understood from Remark 1. In fact, since $I_{out} > 0$ in this example, the trajectory of the reduced voltage vector v_c moves in a direction that is opposite to the one given by s_j . The same direction of movement holds as far as the error vector Δ_{v_c} is concerned. Assuming $\|\tilde{s}_1\| = \|\tilde{s}_2\| = \|\tilde{s}_4\| = 1$ only for the purpose of this explanation, the new position of the error vector $\Delta_{v_c}(t_k + T_s)$ after applying the control action can either be $\Delta_{v_{c1}}(t_k + T_s)$ (using the control versor s_1), $\Delta_{v_{c2}}(t_k + T_s)$ (using the control versor s_2), or $\Delta_{v_{c4}}(t_k + T_s)$ (using the control versor s_4) per unit of current I_{out} . From Figure 5, it can be observed that $\Delta_{v_{c1}}(t_k + T_s)$ is the closest one to the origin; therefore, s_1 is the right control versor to apply in order to minimize the norm of the error vector $\Delta_{v_c}(t_k + T_s)$.

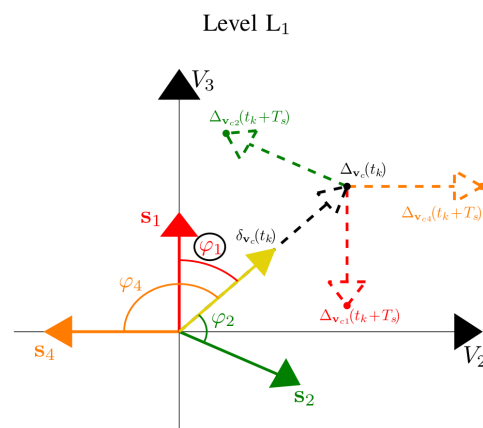


Figure 5. Example of the operation of the MAD algorithm in selecting s_j when the desired output voltage level L is equal to L_1 and $I_{out} > 0$.

The only mathematical calculations performed by the MAD algorithm in Algorithm 1 that require attention are: (1) the normalization at line 2 and (2) the calculation of the angular distance φ_j between the two versors s_j and δ_{v_c} at line 14. The aforementioned operation (1) is always well-defined, thanks to the check at line 1 on the norm $\|\Delta_{v_c}\|$ of vector Δ_{v_c} . The aforementioned operation (2) is always well-defined since:

$$0 \leq \varphi_j \leq \arccos(\mathbf{s}_p \mathbf{s}_{p+1}) = \frac{2\pi}{n} \text{ for } p \in \{1, \dots, n - 1\}.$$

From the latter, it follows that the angular distance φ_j is always lower than the angular distance $\frac{2\pi}{n}$ between two consecutive control versors s_p and s_{p+1} . Note that $\frac{2\pi}{n} \leq \pi$ since $n \geq 2$ must hold in order to have a number of output voltage levels $m \geq 3$, namely in order to have a multilevel converter. Therefore, the arccos characterizing the aforementioned operation (2) is always well-defined.

3.2. Optimal Solution Using Dynamic Programming

From Table 1 and from (11), in the case of $n = 3$, it can be noticed that some degrees of freedom are available when the desired output voltage level L from (14) is either equal to L_1 or L_2 :

$$\begin{aligned} \mathbf{T}_j &= \begin{cases} \mathbf{T}_1 \\ \mathbf{T}_2 \\ \mathbf{T}_4 \end{cases} \Leftrightarrow \mathbf{s}_j = \begin{cases} \mathbf{s}_1 \\ \mathbf{s}_2 \\ \mathbf{s}_4 \end{cases} \text{ if } L = L_1, \\ \mathbf{T}_j &= \begin{cases} \mathbf{T}_3 \\ \mathbf{T}_5 \\ \mathbf{T}_6 \end{cases} \Leftrightarrow \mathbf{s}_j = \begin{cases} \mathbf{s}_3 \\ \mathbf{s}_5 \\ \mathbf{s}_6 \end{cases} \text{ if } L = L_2. \end{aligned} \tag{16}$$

Let us consider a time interval $\mathbf{t} = [t_i, t_i + T_s, \dots, t_f - T_s, t_f]$ such that

$$(L(t_k) = L_1) \vee (L(t_k) = L_2), \quad \text{for any } t_k \in \mathbf{t}. \tag{17}$$

Based on (16), a discrete-time optimal control problem that is able to guarantee that the control objectives (15) are satisfied can be written:

- For all $t_k \in \mathbf{t}$ in (17),

$$\min_{\mathbf{s}_j} J(\mathbf{s}_j) \text{ s.t. } \begin{cases} \text{(a) } \dot{\mathbf{V}}_c(t_k + T_s) = \mathbf{F}\mathbf{V}_c(t_k) + \mathbf{G}\mathbf{u}(t_k), \\ \text{(b) } \mathbf{V}_c(t_i) = \mathbf{V}_{c_0}, \\ \text{(c) } \mathbf{T}_j(t_k), \mathbf{s}_j(t_k) \text{ from } L(t_k) \text{ as in (16),} \\ \text{(d) } \mathbf{S}_j(t_k) \text{ from } \mathbf{T}_j(t_k) \text{ as in (3),} \end{cases} \tag{18}$$

where the objective function $J(\mathbf{s}_j)$ is

$$J(\mathbf{s}_j) = \sum_0^N (V_2(t_k) - V_{2_d})^2 + (V_3(t_k) - V_{3_d})^2,$$

and N is the length of the horizon, meaning the number of time samples $t_k \in \mathbf{t}$ in (17). Points (a) and (b) in (18) describe the evolution of the capacitor voltage trajectories using the discrete-time system (7), starting from the given initial condition \mathbf{V}_{c_0} at $t = t_i$. Points (c) and (d) in (18) describe the calculation of the components of the control vector \mathbf{s}_j and of the configuration vector \mathbf{S}_j , affecting the capacitor voltage trajectories through the matrix \mathbf{G} in system (7). The optimal control problem (18) is subject to the constraints in (16) since the desired output voltage level L needs to be generated. The objective function $J(\mathbf{s}_j)$ in (18) to be minimized over the considered horizon N is composed of two criteria, which are the square distances of the two capacitor voltages V_2 and V_3 from the reference values V_{2_d} and V_{3_d} in (4). The k -th term of the objective function $J(\mathbf{s}_j)$ in (18) is the cost of applying the control vector $\mathbf{s}_j(t_k)$ at $t_k = kT_s$. When solving optimal control problems, an established way to find the optimal control sequence that minimizes an objective function is to use dynamic programming (DP), allowing to achieve the optimal solution given by Bellman’s Principle of Optimality [40]. The principle of dynamic programming is to find the optimal control sequence by proceeding backward, therefore making the whole process much more memory efficient since it is sufficient to evaluate the arc costs at each transition occurring from the final state all the way up to the initial state. This makes this approach noncausal and not implementable in real time since it requires a priori knowledge of the converter cycle. However, DP represents the optimal benchmark that can be used as a term of comparison to evaluate the performances of the proposed MAD algorithm described in Section 3.1. An effective way of solving discrete-time constrained optimal control problems using DP is to use the `dpm` Matlab function [41].

4. Results

This section deals with the simulation of the MFCC in the case of $n = 3$, in order to compare the results of the MAD algorithm with those of the DP optimal benchmark obtained by solving the optimal control problem in (16)–(18) using the dpm Matlab function [41]. The converter parameters used for the results of this section are shown in Table 2, together with the output load current that the converter is subject to and the desired output voltage waveform V_{out_d} , from which the desired output voltage levels L in (14) (to be provided to the MAD algorithm of Algorithm 1) can be obtained. The initial conditions of the capacitor voltages are assumed to be $\mathbf{V}_{c_0} = [100 \ 70 \ 40]^T$ V, where the initial values V_{2_0} and V_{3_0} of the capacitor voltages V_2 and V_3 have been intentionally chosen to be different from the desired values (V_{2_d} and V_{3_d}) given in (4); this is in order to verify the capability of the MAD control algorithm to take the reduced voltage vector $v_c = [V_2 \ V_3]^T$ back to the desired reference $v_{c_d} = [V_{2_d} \ V_{3_d}]^T$ as quickly as possible, as required in (15). The results are shown in Figures 6 and 7, and Table 3.

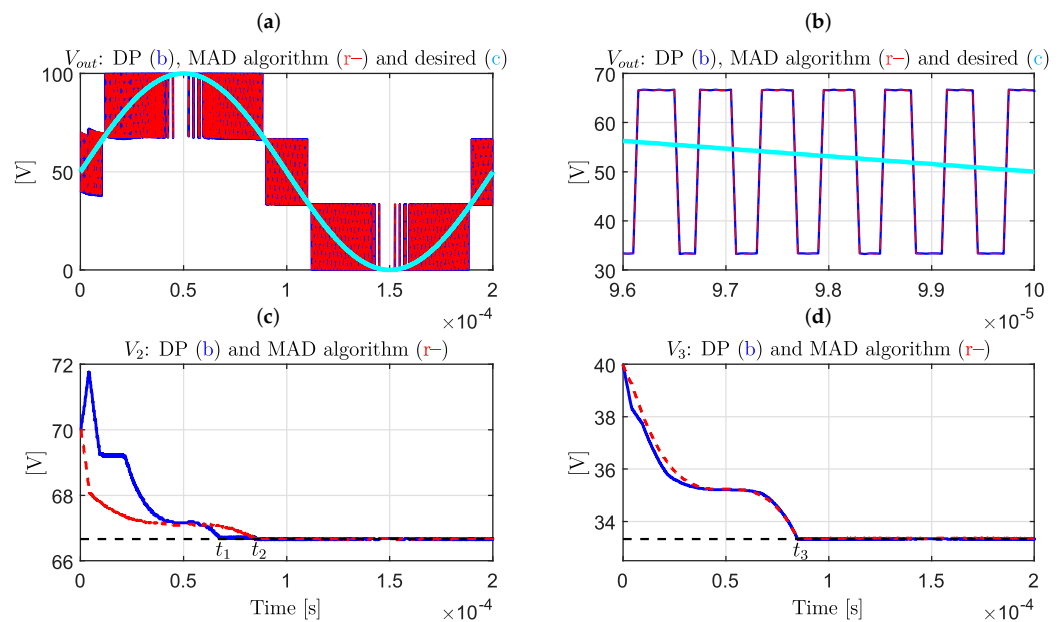


Figure 6. Comparison between the results given by the MAD algorithm and dynamic programming: (a,b) output voltage and (c,d) capacitor voltages.

Table 2. MFCC parameters and desired output voltage V_{out_d} .

$V_{in} = 100$ V, $R_{in} = 0.1$ Ω , $C_3 = 5$ μ F, $C_2 = \frac{C_3}{2}$, $I_{out} = 1$ A
$T_s = 50$ ns, $T_{PWM} = 0.6$ μ s, $V_{out_d} = \frac{V_{in}}{2} + \frac{V_{in}}{2} \sin(2\pi 5 \cdot 10^3 t)$

Figure 6a shows the desired output voltage profile V_{out_d} (cyan), the output voltage values generated by the converter when controlled using DP (blue), and the MAD algorithm (red dashed). Figure 6b zooms in on the time frame $[9.6 \ 10] \cdot 10^{-5}$ s. Figure 6c,d show the capacitor voltages V_2 and V_3 when the converter is controlled using DP (blue) and the MAD algorithm (red dashed). Regarding voltage V_2 , it can be observed that the red dashed plot reaches the reference value (black dashed) at $t = t_2$, that is only 0.0165 ms after the time instant $t = t_1$, at which the blue plot reaches the reference value. As for voltage V_3 , both plots reach the desired value at the same time: $t = t_3$. This proves the effectiveness of the proposed MAD algorithm, which gives convergence times that are very close or equal to those of the optimal benchmark solution while having the advantage

of being implementable in real time and being comprised of very standard mathematical calculations. The colored lines in Figure 7a,b show the directions imposed on the trajectory of the reduced voltage vector $v_c = [V_2 \ V_3]^T$ by the control versors reported in Figure 3, using the same color notation, when $I_{out} < 0$, as described in Remark 1. The dotted characteristics in Figure 7 show the evolution of the trajectory of the reduced voltage vector $v_c = [V_2 \ V_3]^T$ when the converter is controlled using the MAD algorithm (Figure 7a) and the DP optimal benchmark (Figure 7b). The color associated with each dot denotes the control versor s_j applied at the considered time instant t_k , in order to take the trajectory of the reduced voltage vector $v_c = [V_2 \ V_3]^T$ closer and closer to the desired reference v_{cd} . The control versors s_j used in the different parts of the piecewise linear voltage trajectories in Figure 7 are also denoted by the colored labels “ s_j ” reported in each part of the voltage trajectories. The grey dots describing the use of control versor s_0 are not visible in Figure 7 because level L_0 is only required when the voltages V_2 and V_3 reach the reference values of $V_{2,d}$ and $V_{3,d}$; see Figure 6. The grey dots, therefore, accumulate around the desired reference point v_{cd} . Figure 7 highlights that the MAD algorithm and DP impose different paths on the trajectory of the reduced voltage vector v_c , which, however, allow very similar and fast voltage convergence times, as shown in Figure 6c,d. Finally, Table 3 shows the very similar performances of the MAD algorithm and DP in terms of average efficiency \bar{E} and average power loss \bar{P}_l , computed as in (2), as well as their coincident performances in terms of total harmonic distortion (THD) in the generated output voltage V_{out} .

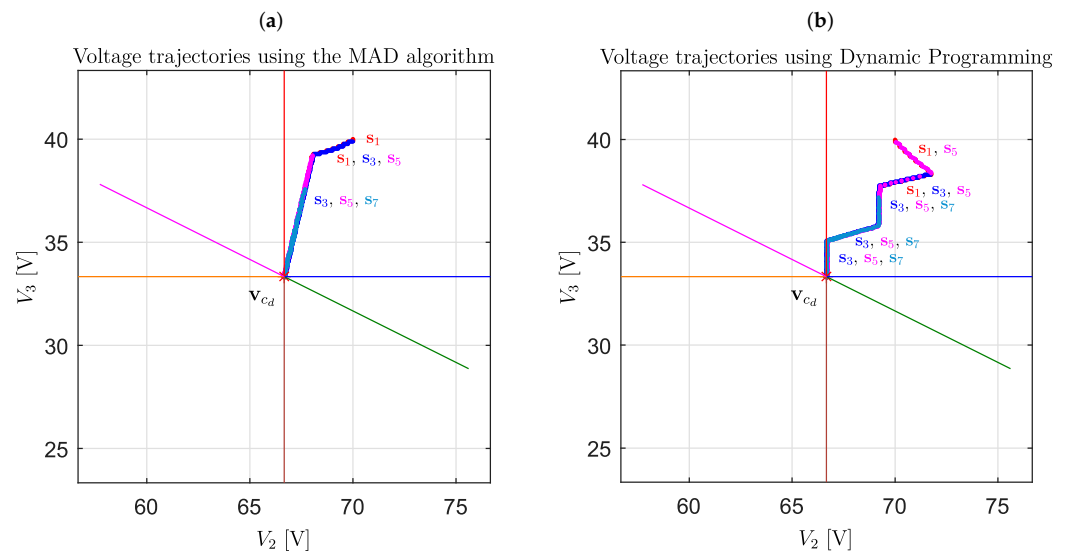


Figure 7. Comparison between the results given by the MAD algorithm (a) and dynamic programming (b): capacitor voltage trajectories.

Table 3. Average efficiency, power loss, and output voltage THD.

	Average Efficiency \bar{E}	Average Power Loss \bar{P}_l	THD
MAD	99.845 %	0.164 [W]	−5.903 [dBc]
DP	99.850 %	0.159 [W]	−5.903 [dBc]

In order to test the effectiveness of the MAD algorithm compared to DP in terms of capacitor voltages fast convergence, a new simulation starting from different initial capacitor voltages, lower than the desired value in this case, was performed. The results are shown in Figure 8, from which it can be seen that the convergence time t_4 is the same for voltages V_2 and V_3 , both when using the MAD algorithm and when using the DP optimal benchmark.

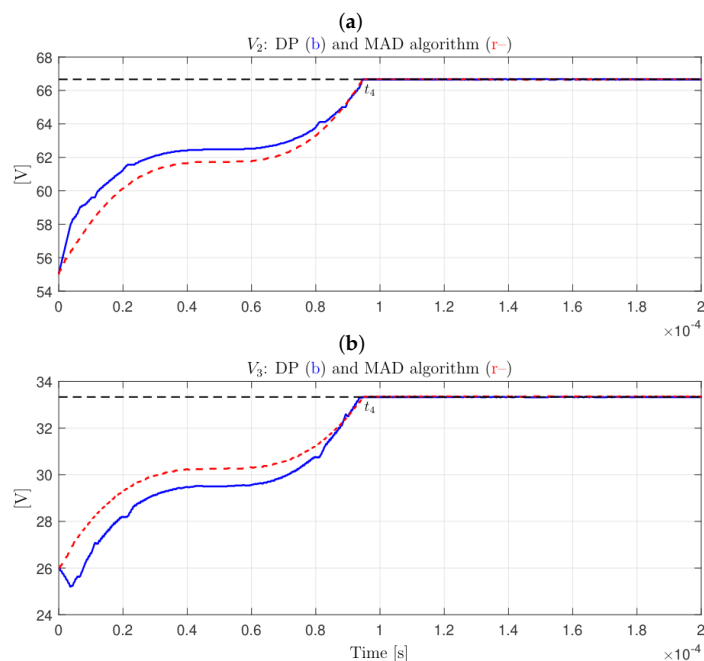


Figure 8. Comparison between the results given by the MAD algorithm and dynamic programming: (a,b) capacitor voltages.

5. Conclusions

In this paper, a detailed analysis of the evolution of the capacitor voltage trajectories as a function of the IGBT signals in multilevel flying-capacitor converters has led to the proposal of a new minimum angular distance algorithm. The proposed algorithm handles the turning on and off of the switches in order to achieve effective capacitor voltages balancing action while generating the desired output voltage. The proposed control algorithm is composed of very simple calculations and does not require any output current prediction. At the same time, the performance of the proposed algorithm has proven to be very good when compared with the optimal benchmark provided by dynamic programming. The future direction of this work should investigate the possible extension of the proposed algorithm to other multilevel converter topologies.

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