Impact of Process Variations on Back-Bias Effect in 100V p-GaN Gate AlGaN/GaN HEMTs

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***Abstract*—In this paper, we investigate the impact of Buffer resistivity and AlGaN barrier design on back-bias stress performed on 100 V p-GaN gate AlGaN/GaN HEMTs. To this end, we compare the results obtained in terms of (i) vertical leakage, (ii) back-bias stress on Transmission Line Measurements (TLM) structures and (iii) back-gating on real transistors. Concerning the latter, a novel test sequence is implemented to monitor the drain current evolution during the stress and evaluate the impact on V_{TH} and R_{ON} parameters after 1000 s stress with V_{SUB}=-50 V. Results indicate that high resistive buffer can significantly reduce the back-bias effect, but also the AlGaN barrier design can affect the parameters drift due to a different two-dimensional electron gas (2DEG) density.**

***Index Terms* - GaN HEMTs, Back-Effect, Vertical Leakage, 2-DEG density, R_{ON}-degradation, V_{TH} drift.**

I. INTRODUCTION

100V p-GaN gate AlGaN/GaN HEMTs are particularly important in power applications to realize both discrete and monolithic solutions. Concerning the latter, the monolithic integration of high-side and low-side transistor in a typical half-bridge configuration yields an important issue from the technological point of view [1]. Given the common substrate potential shared by high and low-side device (see Fig. 1), the high-side transistor experiences a voltage difference between its source and substrate terminal during on-state.

This so-called back-gating effect can be responsible for R_{ON}-degradation and V_{TH} drift, making it extremely important to evaluate this type of stress to understand the impact on performances in real applications.

Different approaches can be considered for this scope. In [2, 3], substrate ramping was used to investigate back bias effect, while in [4, 5] current transients on Transmission Line Measurement (TLM) structures were adopted. Even if both techniques are valid, they are commonly applied to TLM structures and not on the ultimate transistor. Goal of this work is to develop a simple technique able to capture the back-gating effect on the real transistor. Moreover, we aim to correlate the results obtained with measurements on simplified structures to process variations in order to understand the cause for the parameters degradation induced by this kind of stress. This is of paramount importance to provide useful feedback for improving device manufacturing.

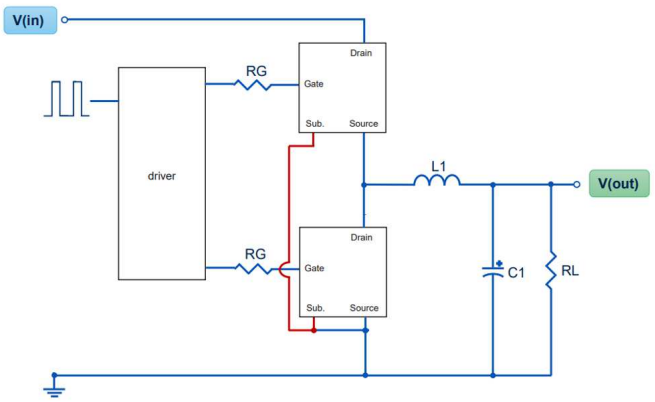

Figure 1. Schematic of a typical Half-Bridge configuration used in a Buck converter topology. In the monolithic integration of high-side and low-side transistors, both devices share the same substrate potential, yielding a voltage difference between source and substrate of the high-side transistor when it is turned on.

The paper is organized as follows: in Section II, we briefly describe the devices tested in this work, providing a first indication on the main differences shown by the samples considered. In Section III we report the preliminary characterization performed on simplified test structures, while in Section IV, back-bias stress/measurement is applied on real transistors to evaluate the different behavior shown by the samples. The correlations with the process variations and related discussion are reported in Section V, leading to the conclusion drawn in Section VI.

II. DEVICES DESCRIPTION

Devices tested in this work were AlGaN/GaN single heterojunction HEMTs grown on Silicon substrate. Four

different AlGaN barrier layer designs have been considered, namely #1, #2, #3 and #4. On the other hand, GaN buffer was Carbon (C) to obtain a semi-insulating layer [6]. Particularly, three different GaN Buffer designs have been tested, herby called Sample A, Sample B and Sample C. Devices gate length was < 1 µm while gate-source and gate-drain spacings were < 1 µm and < 2 µm, respectively. This geometry allows operation in the 0 V to 100 V voltage range. In Fig. 2 we reported the typical cross section of the devices under tests.

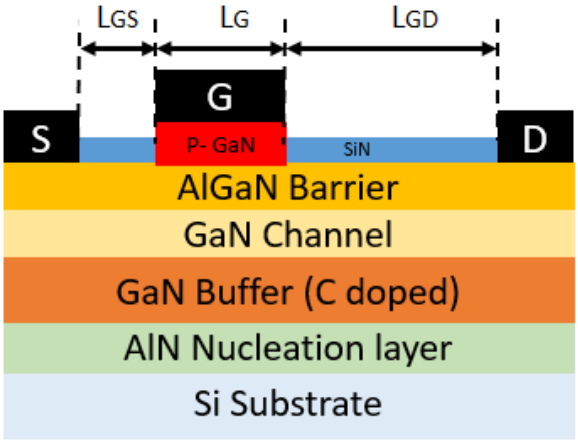

Figure 2. Schematic cross-section of the Device Under Test (DUT). DUTs presented a C-doped buffer layer grown on top of a Silicon (Si) substrate and Aluminum Nitride (AlN) nucleation layer. P-GaN gate is used to achieve normally-off operations, depleting the 2-Dimensional Electron Gas (2DEG) at the AlGaN/GaN heterojunction under the gate terminal even for V_{GS} = 0 V. Four different AlGaN barrier layer designs have been considered, namely #1, #2, #3 and #4. On the other hand, three different GaN Buffer designs have been tested, herby called Sample A, Sample B and Sample C.

The different AlGaN barrier layer designs could significantly impact the I_D-V_{GS} curves of the samples, yielding the differences in terms of triode current (i.e., R_{ON}) and pinch-off voltage shown in Fig. 3. Conversely, no significant differences were shown by samples A, B and C in terms of I_D-V_{GS} characteristics, since all the three samples showed the same AlGaN barrier as #3.

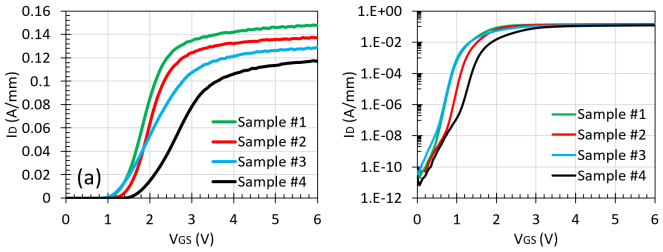

Figure 3. I_D-V_{GS} characteristics acquired on samples #1, #2, #3 and #4: (a) in linear scale, we can appreciate a significant difference in terms of triode current, while in (b) logarithmic scale, we can see a reduced pinch-off voltage for the devices presenting a higher conductivity. For a given AlGaN barrier design, no significant differences are observed by changing the buffer between A, B and C design.

In the following section, we introduce the structures and test conditions employed, along with the preliminary characterization performed.

III. Test Structures and Preliminary Characterization

The test structures used in this work are sketched in Fig. 4.

(i) We first analyze TLM structures (Fig. 4(a)) under Back-bias stress to see the impact of the stress on the 2DEG conductivity.

(ii) Then, to highlight the different resistivity of the three samples considered, vertical leakage measurements (I-V) were performed on the structure reported in Fig. 4(b).

(iii) Finally, tests were performed on real transistors (see Fig. 4(c)), presenting the features described in Section II.

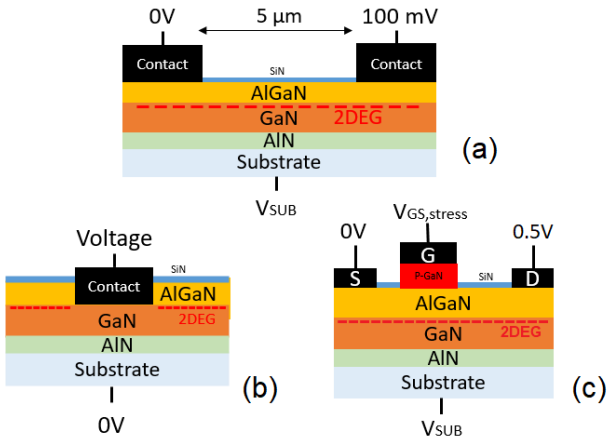

Figure 4. Tested Structures: (a) TLM structure used for back-bias stress; (b) vertical structure used for I-V vertical isolation measurement and (c) actual transistor used for back-bias stress in on-state to emulate high-side configuration in which the Source terminal faces a positive potential difference w.r.t. the substrate.

Concerning the tests performed on TLMs, we firstly measured the current between 5 µm separated pads, with a 100 mV potential applied between pads and V_{SUB}=0 V. This measurement allows to fix a reference fresh value (I_0) for evaluating the Back-Effect degradation. Afterward, the same potential is still applied between pads and the current is monitored for a stress time of 1000 s V_{SUB}=-50 V. The evolution of the current degradation over time (ΔI_{TLM}=I-I_0) is reported in Fig. 5(a) for the samples A, B and C.

On the same samples, vertical leakage measurements have been carried out on the test structure reported in Fig. 4(b). Particularly, four different voltages have been applied to the structure between the top pad and substrate (50 V, 100 V, 150 V and 200 V) yielding the results reported in Fig. 5(b).

As we can see, the Back-Effect degradation is reduced for samples showing a lower vertical leakage, suggesting that a higher vertical resistivity could help in reducing this issue.

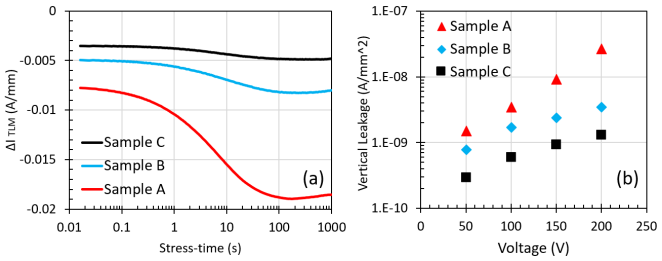

Figure 5. (a) ΔI_{TLM} ($I-I_0$) transients acquired on TLM structure with VSUB=-50V and (b) vertical leakage measurements performed on samples A, B and C. Samples with higher buffer resistivity (lower vertical leakage) are less sensitive to back-bias stress.

Even if this preliminary characterization performed on simplified structures already provides interesting results, it is important to investigate the impact of back-bias stress on the ultimate transistor to see if the trends observed are representative of the final device behavior.

IV. Experimental Results on Real Transistors

The tests on real transistors were carried out by applying the stress/measurement sequence depicted in Fig. 6.

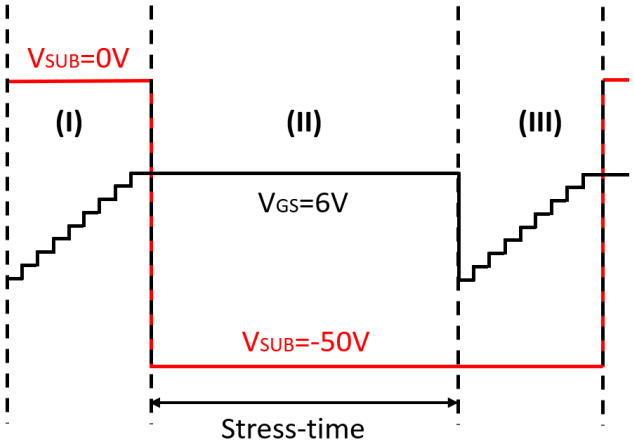

Figure 6. Waveforms employed for the stress/measurement sequence during back-bias stress in on-state. (I) Fresh I_D-V_{GS} is acquired; (II) Negative V_{SUB} (-50 V) is applied in on state (V_{GS}=6 V; V_{DS}=0.5 V) for 1000s; (III) post-stress I_D-V_{GS} is acquired with V_{SUB}=-50 V to reduce current recovery.

The test sequence proposed consists on three main steps.

(I) First, the Fresh I_D-V_{GS} is acquired to set a reference fresh point for the device's parameters.

(II) Then, a negative V_{SUB} (-50 V) is applied in on state (V_{GS}=6 V, V_{DS}=0.5 V) for 1000 s allowing the monitoring of the triode current over several time decades. Particularly, the stress time was set to observe the complete ionization of Buffer traps that have been reported to show time constants of several tens of seconds at room temperature [7].

(III) After the stress, the post-stress I_D-V_{GS} is acquired by still applying V_{SUB}=-50 V to reduce current recovery. The test is performed on devices presenting different buffer resistivity (samples A, B and C).

The results obtained on these three samples are reported in Fig. 7, Fig. 8 and Fig. 9 respectively.

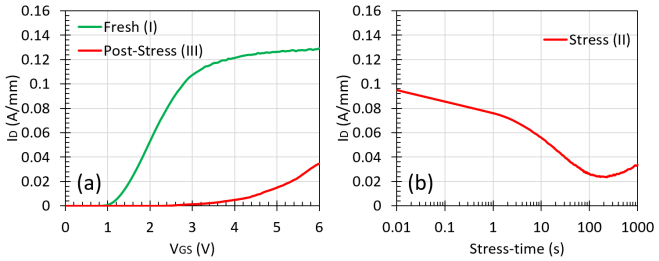

Figure 7. (a) I_D-V_{GS} acquired with the proposed method for Back-bias stress on DUT: Fresh curve (I) and post-stress curves (III) acquired on sample A after a 1000 s stress at V_{SUB}=-50V (II) during which the on-state current transient is monitored (b).

For sample A, we observed a large V_{TH} drift and R_{ON} degradation after the stress phase which is accompanied by a strong dynamic reduction of the triode current during the stress (Step II).

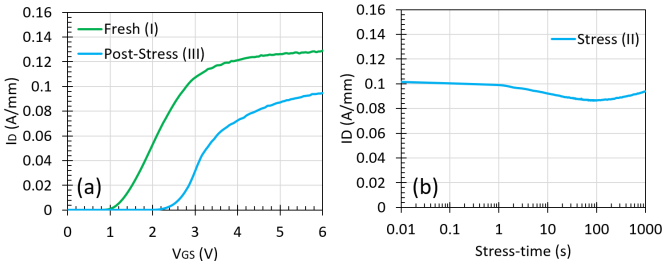

Figure 8. (a) I_D-V_{GS} acquired with the proposed method for Back-bias stress on DUT: Fresh curve (I) and post-stress curves (III) acquired on sample B after a 1000 s stress at V_{SUB}=-50V (II) during which the on-state current transient is monitored (b).

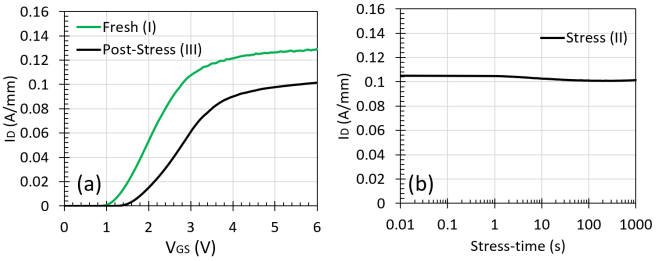

Figure 9. (a) I_D-V_{GS} acquired with the proposed method for Back-bias stress on DUT: Fresh curve (I) and post-stress curves (III) acquired on sample C after a 1000 s stress at V_{SUB}=-50V (II) during which the on-state current transient is monitored (b).

On sample B and Sample C, we observed a reduced degradation on both V_{TH} and R_{ON} parameters, as well as a reduced transient amplitude during the stress at V_{SUB}=-50 V. These results are totally aligned with those observed on TLM

for the corresponding samples. The fact that similar results were obtained on both TLM and real transistors (compare Fig. 5(a) and Fig. 7(b), 8(b) and 9(b)) is coherent with previous literature [8] and suggests that the p-GaN gate was not affecting the experiment. In fact, according to the applied stress, the dynamic reduction of the current over time could be associated to the 2DEG charge variation induced by Buffer traps [7, 9] and not associated to gate instabilities.

The same stress/measurement sequence was then applied on devices showing the same buffer design, but different AlGaN barrier. This yielded devices (#1, #2, #3 and #4) with different 2DEG density. The results are reported in Fig. 10 for which we compared the pre- and post-stress I_D-V_{GS}.

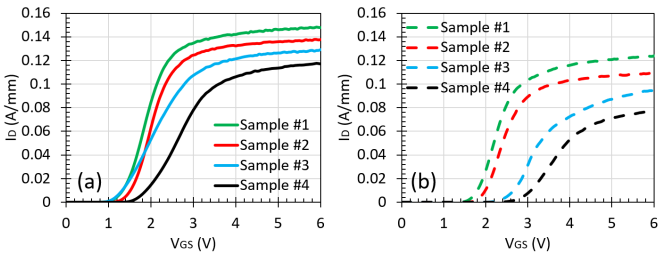

Figure 10. (a) Fresh I_D-V_{GS} curves measured on samples showing different AlGaN barrier (#1, #2, #3, #4) and (b) post-stress I_D-V_{GS} curves acquired after 1000 s back-bias stress in on-state with VSUB=-50 V. Samples presenting a higher fresh current level at V_{GS}=6 V present a reduced current degradation after 1000 s stress time, stemming for a higher carrier density in the 2DEG after the back-bias stress.

In general, a higher fresh current yielded a lower degradation after stress that is totally coherent with a higher carrier density that is less prone to be depleted. To assess the validity of this statement, we report in the following section the correlation observed between 2DEG density and R_{ON}-degradation.

V. Correlations and Discussion

In Fig. 11, we reported the correlation found between R_{ON}-degradation and 2DEG density.

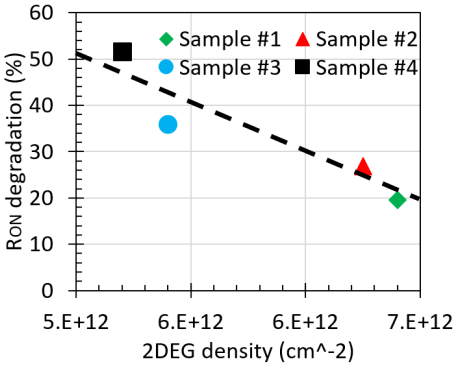

Figure 11. Correlation between 2DEG density (extracted from C-V measurements) and R_{ON} degradation after back-bias stress: samples with more populated 2DEG show a reduced degradation thanks to a higher carrier density that is difficultly depleted.

Essentially, the R_{ON} degradation decreases while increasing the 2DEG density. This is coherent with the fact that a larger carrier availability in the channel is less prone to be depleted, yielding a more conductive channel after the stress and thus a lower R_{ON} degradation.

However, this is just a part of the story. In fact, we have previously observed a strong impact of the Buffer resistivity on the back-bias effect. This is better highlighted in Fig. 12, in which we correlated the R_{ON} degradation with the vertical leakage current.

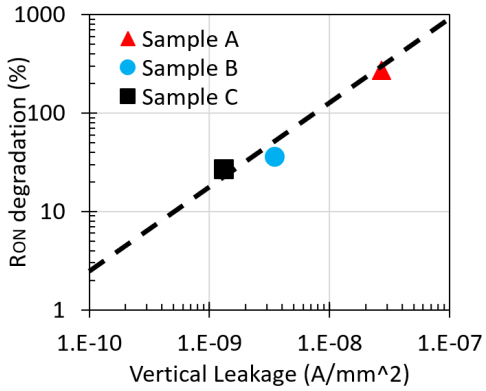

Figure 12. Correlation between vertical leakage and R_{ON} degradation (%) after back-bias stress: samples with more insulating Buffer show a reduced degradation.

As we can see, the degradation increases significantly while increasing the vertical leakage current, suggesting that a poor vertical isolation (i.e., less resistive Buffer) is more likely to cause a strong back-bias effect on the ultimate transistor. Conversely, a higher Buffer resistivity can reduce the degradation and, in principle, prevent the back-bias issue.

VI. Conclusions

In this work we proposed a novel technique to evaluate the back-bias effect on 100V p-GaN gate AlGaN/GaN HEMTs. Thanks to the method proposed, we evaluated the impact of Buffer resistivity and 2DEG density on the R_{ON}-degradation induced by means of back-bias stress. Essentially, an increase in the 2DEG density or in the buffer resistivity can contribute to prevent back-gating effect, thus allowing the realization of half-bridge topology by through monolithic GaN integration.

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