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Review

Low-Power Silicon-Based Frequency Dividers: An Overview

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Abstract: Frequency divider circuits divide the frequency of an input signal by a specified ratio. They are critical components in analog, digital, and mixed-signal microelectronics. In power-constrained environments, such as cryogenic electronics or implanted biomedical devices, minimizing power consumption is crucial. This paper reviews operational principles, benefits, trade-offs, and circuit solutions of three main typologies of frequency divider: Current Mode Logic (CML), Injection-Locking (IL), and True Single-Phase Clock (TSPC). Distinct trade-offs between operation speed, power efficiency, complexity, and integration make each of them suitable for specific applications. Nevertheless, hybrid circuit solutions combining different typologies could potentially balance performance and energy efficiency. This paper thus also reports and discusses examples of hybrid frequency dividers. Examples of frequency dividers implemented in emerging technologies, such as the FinFETs CMOS, are addressed, as well. The purpose of this paper is to guide designers in selecting frequency divider solutions that best meet the design-specific requirements.

Keywords: frequency divider; low power consumption; current mode logic; injection-locking; true single-phase clock; latch; register; CMOS; BiCMOS; FinFET

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1. Introduction

Frequency dividers are fundamental auxiliary components in analog, digital, and mixed-signal microelectronic circuits, used in applications such as frequency synthesis, clock recovery, quadrature generation, and signal processing.

In applications where the thermal budget and/or the available energy limit power consumption, it is crucial for the frequency divider to dissipate as little power as possible. Frequency dividers as a part of cryogenic control electronics for qubits [1,2] or of biomedical implanted/wearable electronic devices are significant examples [3,4].

A frequency divider can be designed by adopting different typologies, including Current Mode Logic (CML), Injection-Locking (IL), and True Single-Phase Clock (TSPC). Each of them offers unique trade-offs in terms of power consumption, speed, complexity, and robustness. Furthermore, their operational principles differ: the IL approach is purely analog, TSPC is purely digital, and CML is mixed-signal.

Each typology excels in distinct application areas. CML circuits can operate at very high speeds, making them suitable for high-frequency communication systems, such as transceivers [5], high-speed data links [6], and 5G wireless networks [7], with the future challenge of shifting toward 6G [8].

In particular, CML frequency dividers are adopted in Phase-Locked Loops (PLLs) [9] and RF/microwave systems [10].

On the other hand, Injection-Locked Frequency Dividers (ILFDs) generate frequency-stable signals while consuming very low power. Thus, they are commonly used in low-power biomedical devices, such as implantable devices [3], where energy efficiency is critical to prolong battery life. They are also used for low-power wireless communication applications [11], such as CML frequency dividers.

Finally, TSPC frequency dividers are easy to integrate, occupy a small silicon area, and consume low power. They are used in digital signal processing systems, including radar [12] and image and sound transmission systems [13]. Additionally, they are key components in high-performance computing systems, such as CPUs, GPUs, and FPGAs [14]. Furthermore, TSPC frequency dividers are employed in high-frequency communication systems, such as PLLs for RF circuits [15].

Nevertheless, hybrid approaches exploiting the strengths of each circuit topology are possible, as demonstrated by [16], with a radiometer that incorporates a static CML frequency divider alongside a dynamic clocked CMOS one, and by [17], with a PLL incorporating IL and CML frequency dividers.

This paper succinctly captures the working principle of the main typologies of frequency dividers (CML, IL, and TSPC), and it also reports, with examples, the circuit improvements claimed in the literature. For each family of frequency dividers, the paper reviews their strengths and limitations, focusing in particular on speed, complexity, power consumption, and occupied silicon surface.

The purpose of this article is to guide designers in selecting a frequency divider circuit solution that best meets their specific requirements.

This paper is organized as follows: Section 2 addresses the CML frequency dividers; Section 3 details the IL Frequency Dividers (ILFDs); Section 4 discusses TSPC frequency dividers. These three sections address their functioning principles and report examples from the literature. Afterwards, Section 5 provides an overview of frequency dividers in relation to advancements, such as sub-30 nm CMOS and FinFETs. Section 6 compares the different circuit solutions and, finally, Section 7 draws some conclusions and explores some future applications.

2. Current Mode Logic (CML) Frequency Dividers

Figure 1 depicts the master–slave architecture of a register, obtained by arranging two latches in a negative feedback loop [18]. This circuit implements a Current Mode Logic (CML) divide-by-2 frequency divider, but it can also be used to generate in-phase (I) and quadrature (Q) differential signals, as each single-ended output signal undergoes a phase shift equivalent to the full angle divided by the number of output signals [19], which are four in this case. As a general rule, when n latches with $2n$ outputs are arranged in cascade, with negative feedback between the last and the first latches, each output undergoes a phase shift equal to the full angle divided by $2n$, i.e., π/n.

As depicted in Figure 2, each latch is composed of three pairs of transistors: a clocked pair (M_1, M_2), an input differential pair (M_3, M_4), and a latch pair (M_5, M_6). The load, formed by the resistors R_D and the capacitors C_D, is shared between the differential pair and the latch pair. The output voltages at the nodes Q and $\overline{Q}$ swing between V_{DD} and $V_{DD} - I_0 R_D$.

The clock CLK splits the circuit operation into two phases: amplification and latching. In the amplification (latching) phase, the CLK is high (low), M_1 (M_2) is on, and M_2 (M_1) is off; the input (latch) pair is activated while the latch (input) pair is deactivated. When the CLK is high, the transistors M_3 and M_4 therefore amplify the differential voltage between the input nodes D and $\overline{D}$. On the other hand, when the clock CLK is low, the circuit reduces to the schematic in Figure 3a. The positive feedback, involving M_5 and M_6, regeneratively

amplifies the difference between Q and $\overline{Q}$. The amplification continues until one transistor of the pair (M_5 or M_6) turns off.

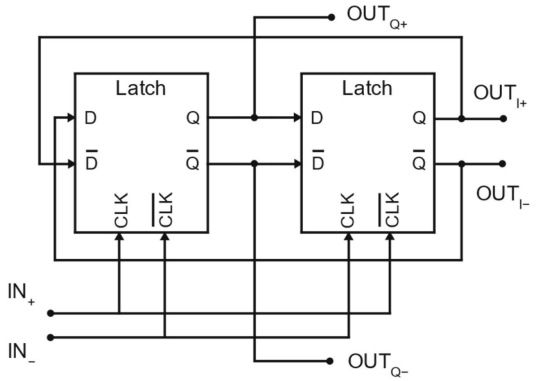


Figure 1. Register as a master–slave arrangement of two latches. IN_+/IN_- are the differential input signals, while OUT_{I+}/OUT_{I-} and OUT_{Q+}/OUT_{Q-} are the two quadrature differential output signals.

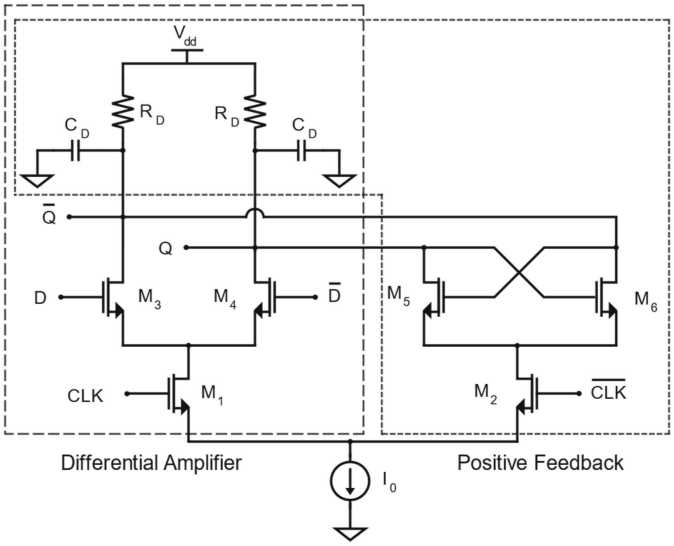
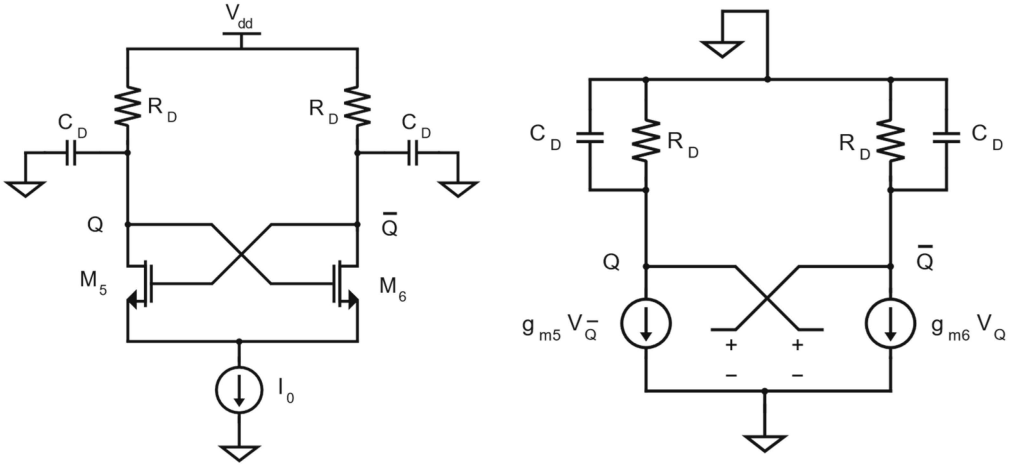


Figure 2. CML latch schematic. C_D are the load capacitors, R_D are the load resistors, and I_0 is the tail current that biases both the differential amplifier and the latch branch.



(**a**) (**b**)

Figure 3. (**a**) CML latch circuit when the clock is low and the latch pair is active; (**b**) small-signal equivalent circuit of the CML latch.

Let us suppose that the initial voltage difference between the voltages at the nodes Q and $\overline{Q}$, denoted as V_{d0}, is small. Therefore, M_5 and M_6 are near equilibrium [20], and we can depict the small-signal equivalent circuit as in Figure 3b.

Applying Kirchhoff's Current Law at both Q and $\overline{Q}$ nodes, and defining $g_m = g_{m5} = g_{m6}$ as the transconductance of M_5 and M_6 transistors, we obtain the following equations:

$$\frac{V_Q}{R_D} + C_D \frac{dV_Q}{dt} + g_m V_{\overline{Q}} = 0, \tag{1}$$

$$\frac{V_{\overline{Q}}}{R_D} + C_D \frac{dV_{\overline{Q}}}{dt} + g_m V_Q = 0. \tag{2}$$

Then, let us subtract Equation (2) from Equation (1), substitute $V_{d0} = V_Q - V_{\overline{Q}}$, and separate the variables. We obtain the following:

$$\frac{dV_d}{V_d} = \left(\frac{g_m R_D - 1}{R_D C_D} \right) dt. \tag{3}$$

By solving the differential equation with the initial condition $V_d(t = 0) = V_{d0}$, we obtain the expression for the regenerative amplification:

$$V_d = V_{d0} \exp\left(\frac{g_m R_D - 1}{R_D C_D} t \right), \tag{4}$$

from which we can define the regeneration time constant:

$$\tau_{reg} = \frac{R_D C_D}{g_m R_D - 1}, \tag{5}$$

which is positive, since we assume that $g_m R_D > 1$. Afterwards, when V_d is high enough, one of the two transistors of the latch pair is switched off, and its g_m reaches zero [20]. In this way, the latch pair solves, in a digital form, the sign of the differential signal previously amplified by the input pair. Equation (4) shows that the solving time decreases as the value of V_{d0} increases. Since this initial condition represents the V_d voltage at the end of the amplification phase, Equation (4) points out that the role of the input differential pair is speeding up the decision-making process of the latch pair. This amplification, provided by the differential pair, together with the positive feedback, intrinsic in the latch pair, ensures the high sensitivity and rapid propagation of even small voltage variations throughout the circuit, allowing high-speed operations.

Now, let us consider the frequency divider, depicted in Figure 1. When the input is not applied to the clock ports of the latches, only the bias voltage is applied to the gate of the transistors M_1 and M_2, and the frequency divider works as a CML ring oscillator, with a self-oscillation frequency f_{SO}. This phenomenon is due to the negative feedback of the master–slave arrangement.

In the case of n latches, with n even, f_{SO} can be expressed as follows [21]:

$$f_{SO} = \frac{1}{2\pi} \frac{\sin \frac{\pi}{n}}{\cos \frac{\pi}{n} + \frac{|I_{LSO}|}{|I_{DSO}|}} \frac{1}{R_D C_D}, \tag{6}$$

where $|I_{DSO}|$ and $|I_{LSO}|$ are the oscillation amplitudes of the currents flowing under the self-oscillation conditions, through the differential pair and latching pair transistors, respectively.

On the other hand, when the input clock is applied, the frequency divider operates as an injection-locked oscillator.

The frequency f_{SO} is the output frequency produced by the divide-by-2 frequency divider when the clock signal has zero amplitude. The minimum clock voltage amplitude $V_{CLK,min}$ required to lock the circuit is when $f_{CLK} = 2f_{SO}$, where f_{CLK} represents the clock frequency. The amplitude $V_{CLK,min}$ increases as the frequency offset $\Delta f = |2f_{SO} - f_{CLK}|$ grows. The graph of $V_{CLK,min}$ as a function of f_{CLK}, known as the sensitivity curve, thus forms a V-shape centered around $2f_{SO}$.

The sensitivity curve is approximately described in [22] as follows:

$$V_{CLK,min} = K_{inj} \frac{\left| \frac{f_{CLK}}{2f_{SO}} - 1 \right|}{\sqrt{1 + \left(\frac{f_{CLK}}{2f_{SO}} \right)^2}}, \quad (7)$$

where K_{inj} is a parameter relating to the current injected by the clock signal and the static current. Equation (7) shows that $V_{CLK,min}$ approaches K_{inj} when f_{CLK} approaches zero or infinity. However, it adequately describes the sensitivity curves only when the ratio $\frac{\Delta f}{2f_{SO}}$ is small, that is, for f_{CLK} close to $2f_{SO}$, or for f_{SO} sufficiently larger than Δf, as in [22].

The CML latch in Figure 2 is used, for example, in [23–28], where it is implemented in classical CMOS technology. A frequency divider-by-2 with 17.7 mW power consumption with a 1.8 V supply and a frequency range of 61.5 GHz–84 GHz is reported in [24]. It consumes more than the divide-by-2 presented in [25], which consumes 0.88 mW, with a maximum frequency of 26 GHz and a voltage supply of 1 V.

On the other hand, some works, such as [29–33], implement this latch using SiGe BiCMOS technology, which makes available SiGe HBTs (Heterojunction Bipolar Transistors) and CMOS FETs in the same fabrication process [34]. Since HBTs outperform MOSFET by offering higher transconductance [33], Equation (4) suggests that HBT CML dividers may offer higher operation frequency.

For instance, Ref. [29] implements a divide-by-4 frequency divider in 130 nm SiGe BiCMOS technology, which can reach a high maximum frequency of 133 GHz for a power consumption of 210 mW. Likewise, the authors of [30], still utilizing a 130 nm SiGe BiCMOS, reach 164 GHz, consuming 134.3 mW. Again, a 55 nm SiGe BiCMOS design achieves frequencies of 63 GHz as in [31], and a 180 nm SiGe BiCMOS design reaches 12.2 GHz with just 74.4 µW of power consumption as in [32].

A Partially or Fully Depleted Silicon On Insulator (PDSOI or FDSOI) may improve performance [35].

A particular solution is proposed in [33]. It is a frequency divider-by-2 designed in a 45 nm PDSOI BiCMOS technology. Inductive peaking with PMOS switches is used for band selection and bandwidth extension. The divider achieves a frequency range from 15 GHz to 185 GHz, consuming 12 mW with a 1.6 V supply. Another example is [32], in which they implement a frequency divider-by-2 using 180 nm SiGe BiCMOS technology, with a frequency range between 30 GHz and 100 GHz. It dissipates 66 mW with a 3.3 V supply. A further solution using HBTs is presented by the authors in [36], where they add an auxiliary transistor to increase current through the amplification pair, implementing a technique called the keep-alive bias technique. In this way, they can precisely control the eventual asymmetry of the two branches by tuning the gate voltage of the auxiliary transistor.

The authors in [37] adopt an interesting, modified version of the CML divider, using a 28 nm FDSOI CMOS process. This work implements Folded MOS Current Mode Logic (FMCML). As depicted in Figure 4, FMCML exploits the complementary nature of CMOS technology, using a PMOS differential pair for the lower level of the stack and a current mirror to connect it to the upper-level NMOS differential pairs. Therefore, this topology

stacks three layers of transistors, instead of four, reducing the minimum supply voltage and the power consumption consequently.

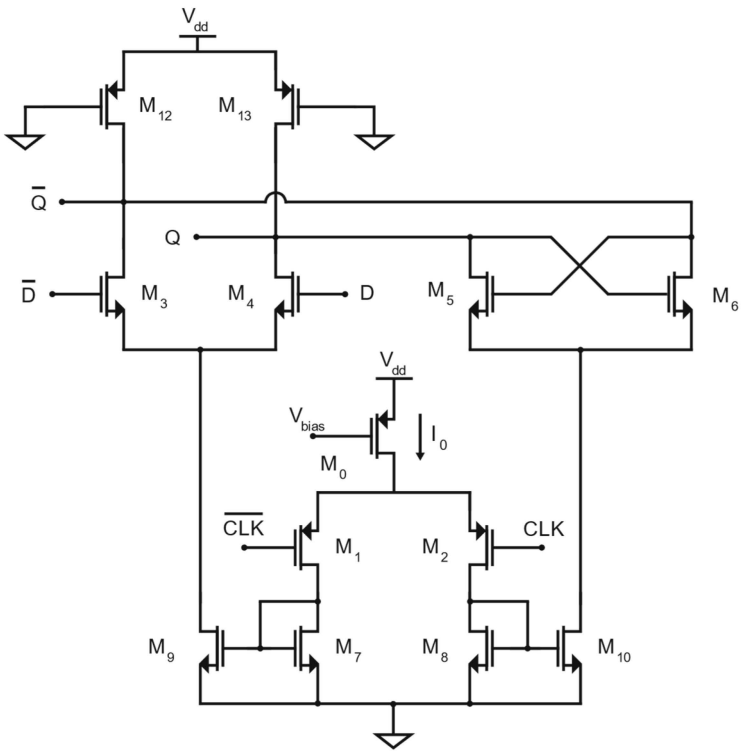


Figure 4. FMCML latch, nType. The pType is complementary. V_{bias} is the bias voltage and I_0 is the tail current.

Each register is composed of two latches. This design is based on alternating FMCML registers with complementary PMOS or NMOS input differential pairs, since common-mode problems arise using only one type of FMCML register.

This circuit manages to obtain a divide-by-16 frequency divider with power consumption equal to 74.4 µW, which is the lowest value among the CML circuit solutions considered, with a maximum frequency of 12.2 GHz, for a voltage supply of 0.8 V.

Another example is [38], which implements an in-phase/quadrature CML divider-by-2 in a 22 nm CMOS FDSOI process for 5G applications. It operates from 21.3 to 30.6 GHz, with a voltage supply of 0.86 V, a power dissipation equal to 11 mW, and an occupied silicon area of 800 μm^2.

A slight variation of the classical schematic is presented in [39]. They realize a divide-by-4/5 frequency divider, adding some logic to the classic CML topology. They obtain a frequency range from 2 GHz to 13 GHz and a power consumption of 19.5 mW.

So far, all the circuits addressed above are static solutions. However, CML latches in a dynamic solution are also possible [10]. Dynamic solutions are advantageous because they do not draw a constant current during the hold phase. Therefore, for the same budget of total dissipated power, the dynamic latch is allowed to consume more current in the reading mode and to adopt lower load resistances, consequently. The time constant thus decreases with improvements to the operation frequency of the latch [10].

Figure 5 depicts an example of such a solution [10]. This circuit makes use of a differential pair, as for the static CML latch. On the other hand, a time-dependent load is peculiar to this circuit. A complementary clock drives both the tail current source (M_0) and the PMOS load (M_3, M_4). The output voltage signal is the exact input replica, just delayed by a 1/2 clock period. A cascade of an even number n of latches closed in a feedback loop can realize a frequency divider-by-n.

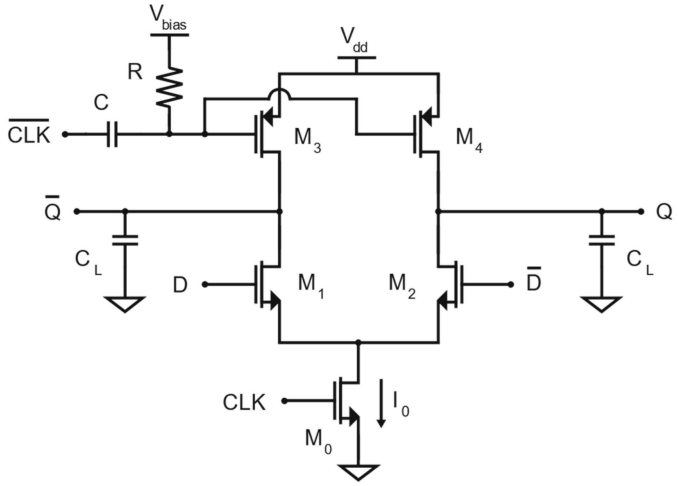


Figure 5. Dynamic CML latch with modulated loads. C_L are the load capacitors, while the resistor R and the capacitor C form an RC bias-tee.

The operation of the circuit can be divided into two parts: read mode, when the clock is high, and hold mode, when the clock is low. During read mode, the differential pair charges the load capacitors C_L. During hold mode, on the other hand, the tail current source is switched off and the parasitic capacitors C_L at the output are discharged through the load constituted by the PMOS equivalent resistance.

Figure 5 shows that the PMOS load transistors are off in hold mode so that the information is held, in terms of stored charge, in the capacitors C_L.

In this way, the load modulation allows for a reduction in the read time with respect to the static solution and guarantees, at the same time, that the output is correctly kept constant during hold mode.

This dynamic topology is implemented in [10], which designs a divide-by-4 frequency divider with an operating frequency range from 14 GHz to 70 GHz, with 4.8 mW as its power consumption and 1 V as its supply voltage. The solution is also used in [40], where they obtain a divide-by-4 frequency divider with a frequency range from 25 GHz to 102 GHz with a maximum power consumption of 5.64 mW for a 0.9 V voltage supply.

Static CML frequency dividers exhibit wide locking ranges and high operation speeds, but they are power-hungry. It is worth remembering that the locking range is defined as the frequency range between the minimum and maximum input frequencies within which the divider correctly operates. Other drawbacks are their larger circuit size due to the adoption of differential structures and additional components.

Furthermore, CML circuits dissipate static power, as they rely on a constant flow of current through the circuit, even during idle states. Another limitation is the necessity for differential input signals, which can complicate their integration with systems that primarily use single-ended signals. Lastly, CML frequency dividers require tail current biasing, which increases the design complexity and necessitates careful calibration.

In conclusion, CML frequency dividers offer good performance at high frequencies, while also being power efficient. However, their larger size, static power dissipation, and reliance on differential inputs and tail current biasing can represent a limit. Nevertheless, when designing systems with stringent performance requirements, CML frequency dividers are an excellent choice, if designed carefully.

3. Injection-Locked Frequency Dividers (ILFDs)

Some classes of frequency dividers are based on oscillators. One example is the regenerative frequency divider, also known as the Miller divider. This type of divider

comprises three main components: a mixer, a filter, and a buffer. The buffer's output is fed back as input to the mixer, enabling the frequency division process. Figure 6 illustrates its block diagram.

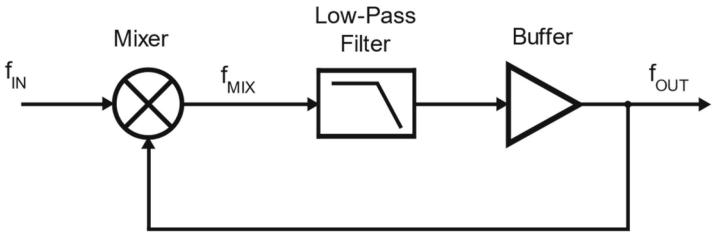


Figure 6. Regenerative frequency divider block scheme.

In this circuit, we can derive the relationship between the output frequency f_{OUT} and the input frequency f_{IN} as follows. By focusing on the second-order intermodulation products only, the mixer behaves like a multiplier, and it generates the output frequencies $f_{MIX} = f_{IN} \pm f_{OUT}$. The low-pass filter selects the lower frequency so that you write $f_{OUT} = f_{IN} - f_{OUT}$, from which $f_{OUT} = f_{IN}/2$.

Injection-Locked Frequency Dividers (ILFDs) represent another class of frequency dividers based on oscillators, with a working principle similar to the one described above. However, regenerative dividers differ from ILFDs, because they can oscillate even without an input signal, whereas ILFDs cannot [20].

An ILFD operates using a nonlinear oscillator that runs at sub-harmonic frequencies of the input signal, corresponding to the frequency to be divided. The oscillator's nonlinearity is exploited to achieve a specific locking frequency range [41].

Figure 7 illustrates the simplest Injection-Locking circuit for realizing a frequency divider-by-2 [42]. Because of the negative transconductance provided by the cross-coupled pair of transistors, the circuit can oscillate. Since the transistors operate in counter-phase, they split the period in two, and node S oscillates at a frequency twice that of the oscillation frequency f_{OUT} of the output nodes.

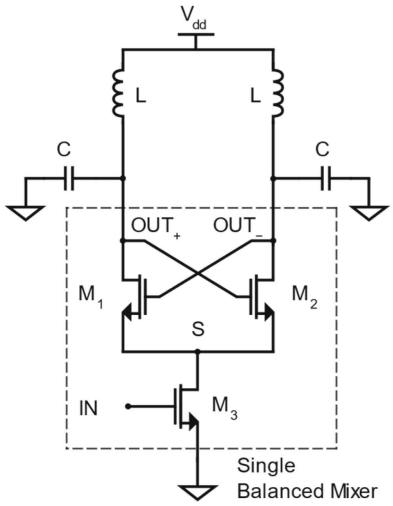


Figure 7. Traditional tail ILFD circuit schematic. The inductors L and the capacitors C form an LC tank to filter the signal.

If the frequency f_{IN} of the input signal is close enough to the resonance frequency, the input signal is able to force $f_{IN} = 2f_{OUT}$, so that you achieve $f_{OUT} = f_{IN}/2$ and the circuit behaves like a divide-by-2 frequency divider. Under these conditions, the circuit operates like a self-oscillating mixer, in which the undesired harmonics are filtered out by the LC circuit [43]. Due to the intrinsic nonlinear nature of the oscillator, f_{OUT} can be

forced, within the limit of the locking range, to be different from the resonance frequency. To some extent, the higher the amplitude of the input signal, the wider the locking range becomes. It is worth pointing out that the LC filtering allows for excellent residual phase noise performance. This feature makes ILFDs ideal for RF communication systems.

The classic tail ILFD inefficiently injects current through the tail coupling transistor M_3, which must be large. In contrast, in the solution in Figure 8, the coupling transistor M_3 operates with higher efficiency because it injects current directly into the LC tank [44]. The transistor M_3 can therefore be designed smaller. It is worth noticing that in the solution in Figure 7, the injection function and the bias function are in charge of the same transistor because M_3 is on the path of the DC tail current. This constrains the degrees of freedom in tailoring the size of M_3, while this is not the case for the solution in Figure 8. In addition, the transistor M_3 in the circuit in Figure 7 should be n-channel, while it can be an NMOS transistor, a PMOS transistor, or be replaced by a pass-gate [44].

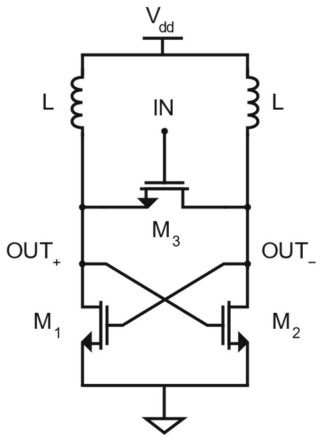


Figure 8. Traditional direct ILFD circuit schematic.

The ILFD frequency dividers offer low power dissipation but involve trade-offs, such as a larger area requirement due to the inductor and a narrower locking range due to the LC resonator.

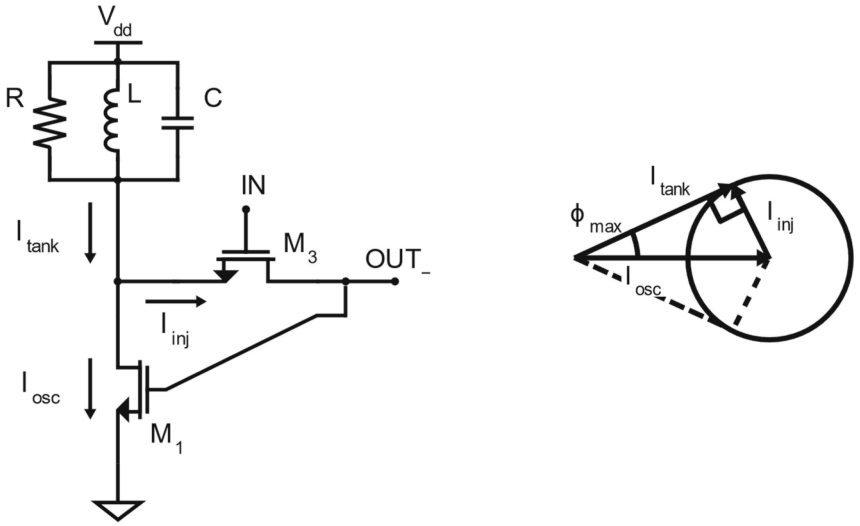
Figure 9a illustrates the half-equivalent schematic of a traditional ILFD. According to the phasor diagram in Figure 9b, for the ILFD to oscillate, the phase difference Φ between $I_{osc}(\omega)$ and $I_{tank}(\omega)$ should increase to match the shift introduced by the LC tank. This phase difference reaches the maximum when the phase difference between $I_{inj}(\omega)$ and $I_{tank}(\omega)$ is equal to 90° [45]. Consequently, the following phase condition holds:

$$\sin \Phi_{max} = \frac{I_{inj}(\omega)}{I_{tank}(\omega)}. \tag{8}$$

The locking range, which is the range of ω_{inj} where Injection-Locking occurs, is given as follows [45]:

$$\omega_L = \frac{\omega_0}{2Q} \frac{I_{inj}(\omega)}{I_{tank}(\omega)}. \tag{9}$$

Here, ω_0 and Q represent the resonance frequency and the quality factor of the LC tank, respectively. Therefore, if the quality factor Q of the LC resonator decreases, the locking range increases. Furthermore, to ensure the ILFD oscillates, the loop gain must exceed one (gain condition) [46].



(**a**) (**b**)

Figure 9. (**a**) Half-equivalent schematic of traditional tail ILFD; (**b**) phasor diagram of the ILFD.

Several ILFD topologies are reported in the literature, most of which are based on the solution in Figure 8. The simplest approach to increasing the locking range is demonstrated in [47], where an ILFD is designed with a low-quality-factor LC tank.

For example, Refs. [48–51] introduce peaking inductors to increase the locking range. Inductive peaking consists of inserting inductors in series with the coupling transistor (M_3) to boost the voltage swing at its drain and source nodes, without reducing the output gain. As a result, the locking range can be enlarged even with low injection power.

Some authors implement circuit solutions by utilizing coupled transformers [52,53], while others combine transformer-based resonators with inductive peaking techniques [46,54,55]. A particularly intriguing approach is employing a transformer-based resonator of an order higher than 2, as it can fulfill the phase condition of Equation (8) over a broad frequency range. This is because, with a higher order, the phase response of the resonator impedance becomes more uniform; the phase curve of a 2*n*-order impedance exhibits a plateau around the central frequency, which can effectively enhance the locking range [46,55,56].

For instance, by employing a 4th-order transformer-based resonator along with inductive peaking, Ref. [46] achieves a frequency range spanning from 27.9 GHz to 53.5 GHz with a supply voltage of 1 V, leading to a power consumption of 5.8 mW. In contrast, Ref. [55] utilizes an 8th-order resonator.

Also, inductorless solutions are possible [57–60]. For instance, in [57], the author adopts an inductorless technique to realize a divide-by-3 frequency divider through a Ring-type Injection-Locking Frequency Divider (RILFD) to overcome the issue of the large area occupied by inductors. The frequency range spans from 100.8 GHz to 110.4 GHz, and the RILFD consumes 4.5 mW at a supply voltage of 1 V. Finally, authors in [61] implement harmonic termination to reduce power consumption.

It is also possible to use both tail and direct injectors driven by the same input signal [59]. In that paper, the authors report on an inductorless multi-injection divide-by-5 frequency divider. Multi-injection significantly broadens the locking range without increasing power dissipation. This divider operates between 8 GHz and 101.6 GHz, consuming 5.6 mW with a 0.9 V supply voltage.

Another technique to enlarge the locking range without increasing static power consumption is the forward-body bias technique [48]. It exploits the body effect to enhance the injection efficiency of the injection transistor (M_3) by reducing its threshold voltage.

Using both inductive peaking and body bias, the authors in [48] demonstrate a frequency divider-by-2 that consumes 2.4 mW with a voltage supply of 0.6 V and operates over a frequency range between 12 GHz and 32 GHz.

On the other hand, Ref. [62] enhances signal injection efficiency by employing a circuit with input and interstage matching, while incorporating shunt peaking inductors to mitigate parasitic capacitances. Ref. [63] broadens the locking range through supplementary current injections. Meanwhile, other works, such as [64,65], suggest the use of distributed LC tanks to extend the locking range by reducing parasitic capacitance; however, this approach necessitates additional inductors, inevitably resulting in a larger chip area.

Another approach for increasing the locking range while keeping low power consumption is the transformer-feedback topology, which implements the oscillator shown in Figure 10.

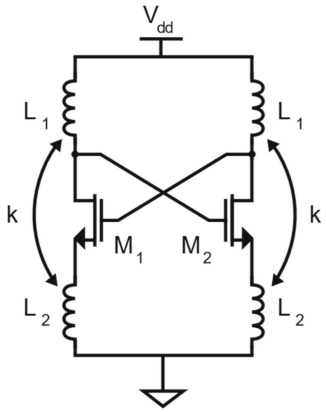


Figure 10. Transformer-feedback oscillator schematic. Here, k is the coupling factor between the inductors L_1 and L_2.

To ensure an ILFD meets the gain condition and minimizes injection–saturation issues with low power consumption, a large cross-coupled pair is required to provide sufficient negative transconductance. However, this increases parasitic capacitance, which dominates the LC tank at high frequencies and reduces the locking range. Conventional ILFDs may struggle therefore in the case of low input power. To address these issues, a secondary transformer (L_2) can be connected to the source terminal of the cross-coupled pair. The added inductors are magnetically coupled to the standard inductors (L_1). When the gate voltage of the cross-coupled pair increases, the source voltage decreases. This out-of-phase relationship between the gate and source voltages provides additional voltage headroom and larger negative transconductance, which improves the gain condition and allows the ILFD to operate with a small bias current at a low voltage supply.

Transformer-feedback ILFDs achieve a wider locking range with lower input power due to reduced cross-coupled pair currents. The transformer serves dual roles: reducing power consumption and redistributing parasitic capacitance, further increasing the locking range [52]. Using this technique, Ref. [52] presents a low-power divide-by-2 frequency divider with a power consumption of 440 µW at a 0.85 V supply, operating over a frequency range from 60.9 GHz to 62.6 GHz. Another example is found in [66].

Using multiple frequency dividers-by-2, it is also possible to obtain higher division factors, as with dividers-by-4 using two ILFDs [67,68]. In particular, they use two frequency dividers with non-coincident, just overlapped locking range to achieve a wide band locking range.

Finally, Ref. [60] presents an ILFD with a frequency range between 26.2 GHz and 35 GHz, and a power consumption of 366 µW at a 1.2 V supply. A technique called the

body injection technique is employed on the PMOS to achieve better control over the threshold voltage of the transistors.

ILFDs can also be implemented in SiGe BiCMOS technology; some examples are in [69–71] with the 350 nm SiGe 3P3M BiCMOS technology and in [72], using the TSMC 180 nm SiGe BiCMOS process.

Ref. [69] realizes a divide-by-3 frequency divider with a frequency range between 3.58 GHz and 6.2 GHz, with a power dissipation of 8.96 mW at a supply of 1.4 V. The die area is 651 μm^2. Ref. [70] shows a divide-by-2/(-4) frequency divider with an operation range from 4.2 to 6.7/(9.06 to 11.96) GHz, with a power consumption of 2.6 mW and a 1.1 V voltage supply. Ref. [72] presents a divide-by-4 frequency divider with a supply voltage of 1.5 V and a frequency from 14.5 to 16.8 GHz, with a core power consumption of 1.5 mW and silicon area equal to 147 μm^2.

In summary, the key advantages offered by ILFDs are excellent noise figures, low power consumption, and quite high operation frequencies.

Despite these advantages, ILFDs face several limitations. A notable drawback is their smaller locking range, which is restricted by the LC tank circuit. Another issue is the presence of unwanted harmonics, which can degrade the quality of the output signal. These harmonics arise from the nonlinear nature of the Injection-Locking process and may require additional filtering stages to suppress, making the circuit more complex. Furthermore, the LC tank circuit occupies a large silicon area due to the physical size of the inductors and capacitors.

ILFDs also face challenges in providing multiple phases or achieving a large divisor number within a single LC oscillator stage. Scaling the division ratio or implementing multi-phase outputs may require additional stages or circuitry, increasing the chip area and the complexity of the circuit solution. For instance, achieving an odd division ratio using the traditional ILFD circuit necessitates a balun [73]. Additionally, the complexity of injecting a high-quality signal increases the design effort. As such, ILFDs are best suited for niche applications where their strengths, such as noise filtering and frequency scalability, outweigh the drawbacks.

4. True Single-Phase Clock (TSPC) Frequency Dividers

The True Single-Phase Clock (TSPC) frequency divider is a widely used architecture in modern CMOS design due to its simplicity, efficiency, and compatibility with digital circuits. In particular, the TSPC circuitry avoids clock skew issues, because it uses a single clock signal.

Figure 11 shows that a TSPC latch can be implemented using six transistors in two different versions—positive or negative—depending on the type of the MOS transistors controlled by the clock signal.

Figure 12 demonstrates that a divide-by-2 frequency divider can be implemented by arranging two TSPC latches in series. In this configuration, the output signal is inverted and fed back as the input signal to form a register [74]. There are four possible architectures. When the latches are of the same type, an inverter is required to generate the counter-phased clock. Therefore, the architectures in Figure 12a,b cost 16 transistors, while the ones in Figure 12c,d cost 14 transistors.

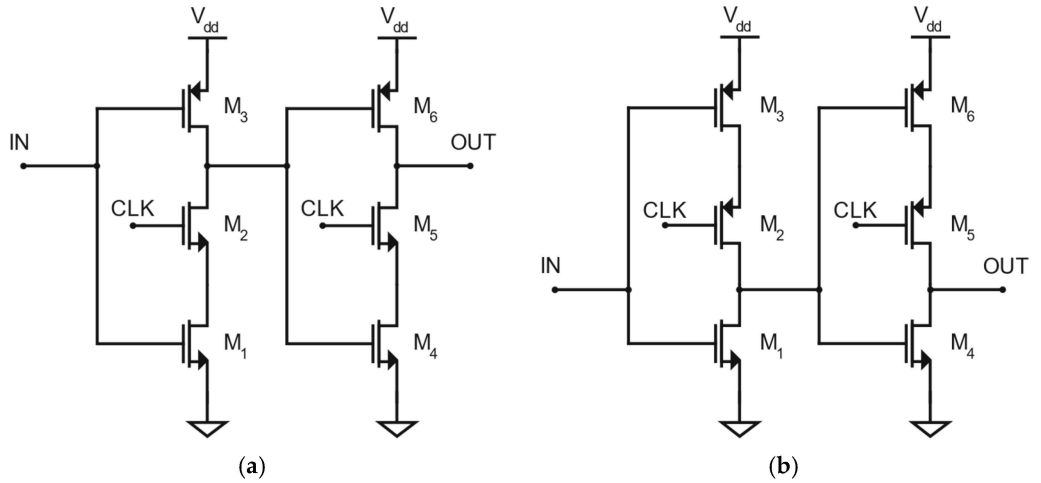


Figure 11. (**a**) Positive TSPC latch; (**b**) negative TSPC latch. The clock signal CLK works as an enable signal for the inverters.

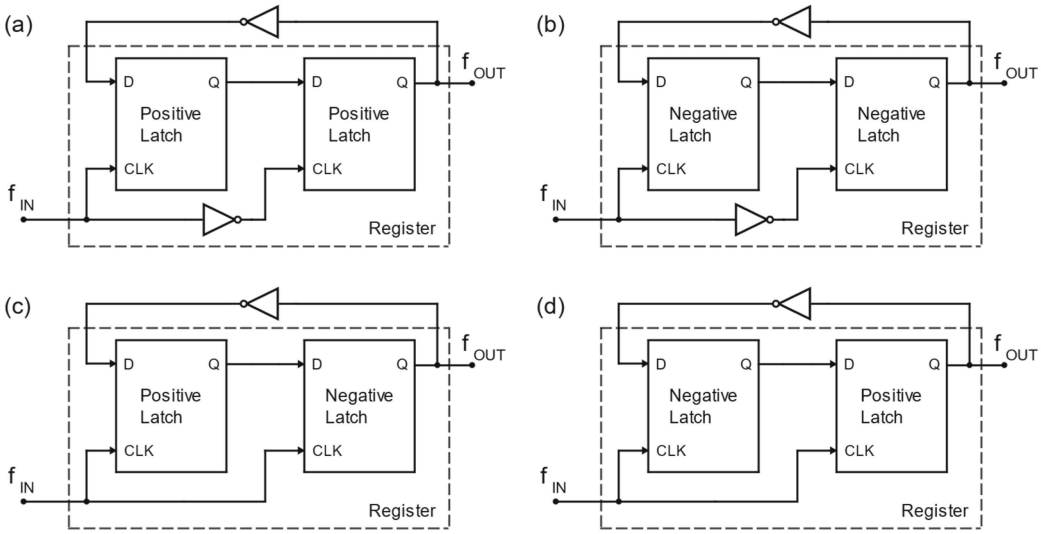


Figure 12. Divide-by-2 TSPC frequency dividers possible master–slave architectures. (**a**) Register with two positive latches; (**b**) register with two negative latches; (**c**) register with a positive latch as master and a negative latch as slave; (**d**) register with a negative latch as master and a negative latch as slave.

While TSPC dividers are composed of two latches, like Current Mode Logic (CML) frequency dividers, they cannot generate quadrature signals directly. This limitation arises because an additional stage is required to evaluate the output state, typically represented by an inverter (as shown in Figure 12). In this regard, Ref. [75] addresses this problem by adopting a hybrid approach that combines a TSPC frequency divider in cascade with a CML frequency divider to generate quadrature signals.

Figure 13 depicts a less expensive solution for a divide-by-2 TSPC frequency divider [74]. The nine transistors M_1–M_9 form a TSPC register, which can be broken down into three main sub-circuits. The transistors M_1-M_3 form a half-positive TSPC latch, the transistors M_4–M_6 form a dynamic inverter with M_5 being the pull-up network, and, finally, the transistors M_7–M_9 form a half-negative TSPC latch. It is worth noticing that a half-TSPC latch is equivalent to a clocked CMOS static inverter, which is active if the clock is high (low) in the case of a half-positive (negative) TSPC latch.

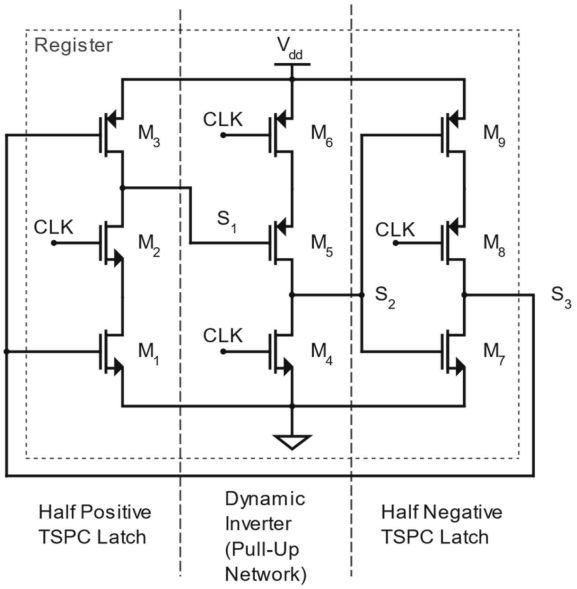


Figure 13. TSPC divide-by-2 frequency divider.

The register operation can be described by assuming that the input signal, on the gates of M_1 and M_3, is high.

If the clock signal CLK is high (low), the input clocked inverter is active (inactive), and, thus, the signal S_1 is low (kept at the previous value, because M_2 and M_3 are both off). Concerning the dynamic inverter in the middle, the high (low) CLK sets it in the pre-discharge (evaluation) phase, so that the signal S_2 is forced low by M_4 (is the logic negation of the S_1 value). Regarding the output clocked inverter, it is inactive (active), because the CLK is high (low), with M_8 being a p-channel MOSFET, and the output, therefore, assumes the previous value (the value of S_1).

On the CLK falling (rising) edge, the input clocked inverter is deactivated (activated), and, therefore, the signal S_1 remains (reaches) a low value because the input signal is high. After the falling (rising) edge, the CLK signal is low (high), the dynamic inverter enters the evaluation (pre-discharge) phase, and the output clocked inverter is active (inactive), and, thus, S_2 goes high (low), and the output becomes zero (remains at the pre-edge value of S_1).

The output therefore assumes the negated logic value of the input in correspondence with the CLK falling edge. On the other hand, it remains unchanged on the CLK rising edge. It is straightforward to verify that similar conclusions hold in the case where the input signal is low. Therefore, following the main idea behind the master–slave architecture in Figure 12, closing the feedback from the output to the input leads to a divide-by-2 frequency divider, as depicted in Figure 11. Nevertheless, the dividers in Figure 12 cost between 14 and 16 transistors, while the divider in Figure 13 costs 9 transistors only.

Some works that implement TSPC topologies are reported in [76,77]. The authors in [76] describe frequency dividers for 8/9 prescalers, with a frequency range between 0.5 GHz and 14.5 GHz, a voltage supply of 1.2 V, and a power consumption of 821 µW. The authors in [77] report on frequency dividers for 4/5 and 8/9 prescalers. The former has a maximum working frequency of 6.8 GHz, with a power consumption of 960 µW, while the latter has a maximum frequency of 8.5 GHz and a power consumption of 1.16 mW. Both have a minimum working frequency of 500 MHz and use a voltage supply of 1.2 V.

Extended True Single-Phase Clock (ETSPC) logic can be used to design a frequency divider with improved operation frequency, as in [74]. This technique increases the operation speed because it eliminates the RC delay of these stages. Figure 14 reports the schematic of an ETSPC divide-by-2 frequency divider, whose operation principle is similar to the circuit

in Figure 13, but at the cost of six transistors only. The core of the circuit is the cascade of three inverters, whose load is modulated by the clock signal.

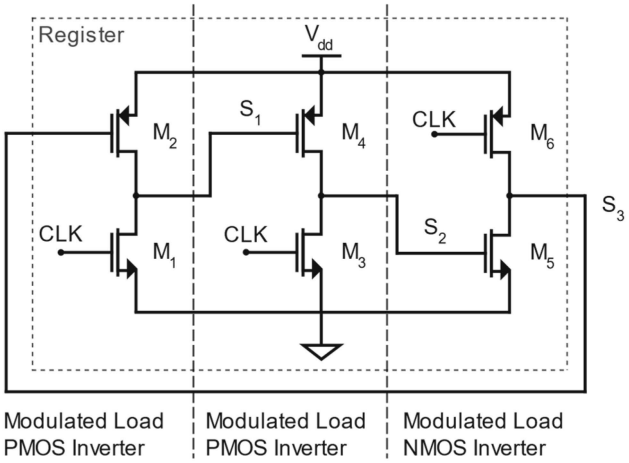


Figure 14. ETSPC divide-by-2 frequency divider.

For an ETSPC register, the transistor form factors are of paramount importance. Specifically, some states are undefined unless one transistor dominates the other. In particular, the form factor of M_2 should be larger than that of M_1; the form factor of M_3 should be larger than that of M_4; and the form factor of M_5 should be larger than that of M_6.

For addressing the working principle of the ETSPC register, let us assume that the CLK signal is high, making M_1 and M_3 on, while M_6 is off. If the input signal, on the gate of M_2, is high (low), S_1 is low (high), because M_2 is off (on, with a larger aspect ratio than M_1), and, thus, M_4 is on (off) and S_2 is low, because M_3 is on with a larger aspect ratio than M_4. S_2 being low makes M_5 off. The output therefore remains at its previous value because M_6 is also off, as remarked above.

On the CLK falling edge, M_1 switches off and, if the input signal is high (low), S_1 remains low (high) because M_2 is off (on); thus, S_2 goes high (remains low), because M_3 also switches off on the edge, and, therefore, the output signal is low (high) because M_5 is on with an aspect ratio higher than M_6.

On the other hand, in the case of the CLK rising edge, M_3 is on and M_6 is off after the edge since the CLK signal is high. This forces S_2 low and, thus, M_5 off. The output therefore remains at its previous value, because both M_5 and M_6 are off.

We can thus conclude that the output signal can change, taking the logic negation value of the input signal, only in correspondence with the CLK falling edge. Also, for the ETSPC register, a divide-by-2 frequency divider can be obtained by closing the feedback from the output to the input, as depicted in Figure 14.

By exploiting the ETSPC technique, the authors in [74] designed a divide-by-8 frequency divider that exhibits a maximum frequency equal to 12 GHz, and it consumes 748 µW from a 1.1 V voltage supply.

Also, the authors in [15] adopted the ETSPC technique. They obtained a divide-by-4 frequency divider exhibiting a frequency range between 16 GHz and 70 GHz and a power consumption of 350 µW from a 0.8 V supply.

The authors in [78] demonstrated a low-power divide-by-2 (divide-by-3) ETSPC frequency divider, draining just 4.35 µW (4.61 µW) from a 0.6 V supply, but at the cost of a low maximum operation frequency, equal to 531 MHz (525 MHz), which uses a pass transistor as control logic. However, it can reach up to 2.98 GHz as maximum frequency by increasing the voltage supply to 0.9 V.

The power consumption of a CMOS digital circuit is mainly determined by switching power, which results from the charging and discharging of capacitive loads during transitions. However, when both the PMOS and NMOS transistors are simultaneously turned on, short-circuit power is also introduced [79].

The load capacitance of the TSPC register is greater than that of the ETSPC register, resulting in higher switching power consumption for the TSPC register, as switching power is directly influenced by the output load capacitance. As noted in [80], reduced load capacitance leads to lower short-circuit power. In a 2/3 prescaler, the ETSPC register consumes less switching power (due to charging and discharging of load capacitances when transistors switch states) but exhibits significantly higher short-circuit power, which occurs when the ETSPC operates as a divide-by-2 circuit [79]. This short-circuit power is influenced by transistor sizing, making it more prominent in ETSPC designs.

Moreover, ETSPC circuits require a larger clock signal amplitude but support higher operating frequencies, while TSPC designs are more power-efficient and better suited for ultra-low-power applications. However, it is possible to combine TSPC and ETSPC dividers to use their strengths: TSPC minimizes power consumption in low-frequency operations, while ETSPC excels at high-frequency tasks. This hybrid approach balances power efficiency and speed, making it ideal for applications requiring both performance and low energy consumption. This hybrid solution combining both TSPC and ETSPC circuits to realize a divide-by-2/3 frequency divider is used in various works [81–83].

The circuit reported in [81] obtains a 2/3 prescaler exhibiting a frequency range from 3 GHz to 24 GHz and a power dissipation of 56 μW (divide-by-2) and 74 μW (divide-by-3) from a voltage supply of 1 V.

Notably, in [82], the approach leads to a 2/3 prescaler operating in the frequency range from 4 GHz to 8 GHz, with a voltage supply of 1.8 V. The divider-by-2 consumes 50 μW, while the divider-by-3 consumes 680 μW. The circuit in [83] exhibits a high maximum operation frequency in the 6 GHz to 17.1 GHz frequency range. It dissipates 471 μW (divide-by-2) and 444 μW (divide-by-3) from a 1.2 V voltage supply.

FDSOI brings advances for both TSPC and ETSPC frequency dividers. The authors in [84] propose a TSPC divide-by-5 fabricated in a 22 nm FDSOI CMOS technology. The maximum frequency is 35 GHz, with a power consumption of 1.35 mW. The divider core occupies a silicon surface equal to about 34 μm^2.

On the other hand, an ETSPC divide-by-4 frequency divider implemented in a 22 nm FDSOI CMOS technology, in [15], achieves a frequency range from 16 to 70 GHz, with a power consumption of 350 μW, a voltage supply of 0.8 V, and an area of 3.4 μm^2.

One of the advantages of the TSPC typology is its ability to achieve reasonably high speeds, making it ideal for applications in digital and mixed-signal circuits that require rapid frequency division. Additionally, TSPC circuits occupy a small silicon area since they are composed of just transistors.

Furthermore, TSPC dividers do not consume static power. Indeed, unlike Current Mode Logic (CML) designs, which drain a constant flow of current even when the circuit is in idle states, TSPC circuits operate solely on dynamic switching, leading to substantial power savings. Moreover, the TSPC approach requires only a single-phase clock, which simplifies the clock distribution network and reduces the design complexity associated with generating and synchronizing multiple clock phases. This simplification not only improves efficiency but also reduces power overhead and potential clock skew issues.

However, the TSPC typology also suffers from drawbacks. One notable limitation is the propagation delay introduced by the circuit. For every input cycle, the signal must pass through three gates, which adds latency and limits the maximum operating frequency of

the circuit. Another limitation is the requirement for full-swing CMOS input signals, which means that the voltage levels must be well defined and not degraded.

Additionally, not only are TSPC designs slower than CML circuits but it is also not possible to obtain quadrature outputs with them, as is the case for the CML frequency dividers. Furthermore, the reliance on dynamic registers in TSPC dividers introduces potential challenges at low operating frequencies, since charge leakage can happen over time. Therefore, if the clock period is too long, TSPC circuits can fail [85].

Technology scaling improves device density and reduces power consumption by lowering power supply levels but also increases the leakage current due to reduced transistor threshold voltage [86]. The major components of leakage are gate oxide leakage and subthreshold leakage [87]. NMOS transistors typically experience higher gate oxide leakage than PMOS transistors of similar dimensions because of the higher probability of electron tunneling [87].

Subthreshold leakage causes current flow between the source and drain. This current varies exponentially with threshold voltage reduction [87]. While gate oxide leakage dominates in idle mode or at low temperatures, subthreshold leakage is the primary contributor at high temperatures or during active mode.

Circuit design techniques address leakage issues. Transistor stacking reduces leakage significantly; for instance, a two-transistor stack exhibits an order-of-magnitude lower leakage than a single transistor [88], a principle applied in TSPC frequency dividers [87]. Multi-Threshold CMOS (MTCMOS) integrates high-threshold transistors to suppress subthreshold leakage while using low-threshold transistors for high performance. Variable-Threshold CMOS (VTMOS) employs body biasing to control threshold voltage, applying a deeper reverse bias in standby mode to cut leakage currents [89]. Similarly, Dynamic-Threshold CMOS (DTCMOS) ties the gate and body together, allowing real-time frequency adjustments through back-gate biasing [90,91]. Additionally, supply voltage scaling reduces switching power, but also decreases leakage power, as subthreshold leakage reduces with lower supply voltage [89].

Effective TSPC designs must address both gate oxide and subthreshold leakage across varying modes and temperatures to optimize performance and minimize power loss [87].

In summary, the TSPC frequency divider offers a compelling combination of speed, compactness, and power efficiency, making it an interesting choice for digital circuit design. Its ability to operate with a single-phase clock and the elimination of static power consumption make it a preferred typology for low-power applications. However, they present some limitations, including propagation delays, input signal requirements, and leakage issues at low frequencies.

5. Future Outlooks: 28 nm Process Technology, FinFETs, 3D Integration, AI-Based Optimization

As the semiconductor industry moves toward smaller technology nodes and explores beyond-CMOS solutions, innovations in process technologies such as FinFETs (Fin Field-Effect Transistors) and 3D integration are applied to frequency dividers to achieve higher speed, lower power consumption, and smaller occupied silicon area.

Just scaling the channel length may lead to improvements. For example, considering CML frequency dividers, a 28 nm CMOS implementation achieves a low power consumption of 880 μW [25], while the authors in [40], also using 28 nm CMOS, obtain a maximum frequency of 102 GHz.

ILFDs also benefit from scaling technologies to achieve high frequencies. For example, a frequency divider-by-6, implemented in 28 nm CMOS technology, operates in a frequency range from 1 to 55 GHz, with a power consumption of 2.7 mW [58]. The authors in [59]

propose another ILFD design implemented in the same technology that achieves frequencies from 8 to 101.6 GHz, with a power consumption of 5.6 mW, demonstrating the potential for high-frequency performance using advanced technological nodes.

To further scale the channel length of the transistors, an interesting solution is to use FinFETs. A FinFET uses 3D transistor architecture designed to address the limitations of planar MOSFETs, particularly in advanced nodes below 28 nm. Unlike traditional planar transistors, FinFETs use a thin, vertical fin structure to form the channel. This design enables higher performance, lower power consumption, and improved scalability [92]. On one hand, FinFET devices enable high-frequency operations due to their high drive currents and offer reduced power consumption thanks to lower leakage currents. On the other hand, their 3D structures introduce greater layout complexity and increased parasitics.

Frequency divider circuits could benefit from implementation in FinFETs. In this regard, the authors in [93] implement a frequency divider in a 5 nm FinFET CMOS process. The divider uses static latches in master–slave architecture. It was measured for a frequency up to 10 GHz, it consumes 720 μW, and it occupies a silicon area of 79 μm^2. Also, the authors in [94] implement a transceiver in a 22 nm FinFET CMOS process, which contains a CML quadrature frequency divider working at a frequency of 53.6 GHz.

Another example is reported in [95], where an ILFD together with an injection-locked oscillator is used to design a frequency doubler in 10 nm FinFET technology. The proposed frequency doubler consumes 12 mW with a 0.8 V supply, with a frequency range from 23.9 to 29.4 GHz, and it occupies 0.035 mm^2. Additionally, the authors in [96] demonstrate that TSPC circuits can benefit from being implemented in FinFET technology. In this work, the author uses the 18 nm FinFET process to design a TSPC frequency divider and demonstrates that realizing a circuit with FinFET transistors reduces the number of devices used compared to classic CMOS transistors.

Frequency dividers realized as latches in a register with negative feedback have been implemented in FinFET technology in a few papers. The authors in [97–99] use frequency dividers as part of a PLL implemented in 5 nm, 14 nm, and 6 nm FinFET processes, respectively. Similarly, the authors in [100] present a transmitter in 10 nm FinFET technology, which also incorporates frequency dividers.

Besides FinFET technology, an alternative approach to implementing frequency dividers is offered using 3D integrated layouts [101,102]. One notable example is a frequency divider implemented as a master–slave register specifically designed for 3D integration, as presented in [103]. Furthermore, a 3D integrated static latch that could be used as part of a frequency divider is presented in [104]. By exploiting 3D integrated circuits, designers can achieve lower costs, higher device packing density, and reduced connectivity latency [103]. Indeed, interconnect lengths are shortened by stacking circuits vertically, which minimizes parasitic capacitance and improves signal integrity.

Above, we have discussed technologies that can improve frequency divider circuits. However, circuit performance can also be enhanced using Artificial Intelligence (AI) in the design process. Indeed, AI-based algorithms can automate circuit sizing optimization and improve performance models [105]. In integrated circuit design, AI optimizes sizing, placement, power consumption, and overall efficiency, enabling faster, more reliable, and energy-efficient circuits, while also reducing design time and effort. For example, the authors in [11] apply the seeker optimization algorithm [106] to design an ILFD circuit.

6. Discussion

The following three tables compare the above-investigated typologies of frequency dividers in terms of process technology, operation frequency, voltage supply, division factor,

dissipated power, and silicon area. Table 1 is focused on the CML implementation, Table 2 on the ILFD, and Table 3 on the TSPC.

Table 1. CML frequency dividers comparison table.

CML Paper	Year	Technology	f_{min} (GHz)	f_{max} (GHz)	Voltage Supply (V)	Division Factor	Power (mW)	Silicon Area (μm^2)
[23]	2008	65 nm CMOS	64.7	94.4	2.4	2	129.8	4000
[24]	2008	65 nm CMOS	61.5	84	1.8	2	17.7	6075
[29]	2010	130 nm SiGe BiCMOS	6	87	3	4	14	278,400 *
[29]	2010	130 nm SiGe BiCMOS	6	105	3.6	4	51	278,400 *
[29]	2010	130 nm SiGe BiCMOS	6	133	5.8	4	210	278,400 *
[10]	2013	32 nm CMOS	14	70	1	4	4.8	990
[25]	2014	28 nm CMOS	0	26	1	2	0.88	250
[40]	2015	28 nm CMOS	25	102	0.9	4	5.64	635
[39]	2017	130 nm CMOS	2	13	1.5	4/5	19.5	2240
[36]	2017	130 nm SiGe BiCMOS	2	92.5	1.5	2	37	24,300
[26]	2018	180 nm CMOS	1	8	1.8	4	12.6	610,000 *
[38]	2019	22 nm FDSOI CMOS	21.3	30	0.86	2	11	800
[31]	2020	55 nm SiGe BiCMOS	40	63	3	2	23.7	3900
[37]	2021	28 nm FDSOI CMOS	0	10.5	0.8	16	0.0528	83
[37]	2021	28 nm FDSOI CMOS	0	12.2	0.8	16	0.0744	166
[30]	2022	130 nm SiGe BiCMOS	145	163	3.3	16	396	27,000
[32]	2023	180 nm SiGe BiCMOS	30	100	3.3	2	66	8800
[27]	2023	180 nm CMOS	4.96	5.88	1.8	4	4.59	19,152 *
[33]	2024	45 nm PDSOI BiCMOS	15	185	1.6	2	12	240,000 *
[28]	2024	110 nm CMOS	5	29	1.35	2	5.47	1350

* Bond pads included.

Table 2. ILFDs comparison table.

ILFD Paper	Year	Technology	f_{min} (GHz)	f_{max} (GHz)	Voltage Supply (V)	Division Factor	Power (mW)	Silicon Area (μm^2)
[62]	2006	130 nm CMOS	58.4	63	1.2	2	8.8	127,200
[51]	2007	180 nm CMOS	37.5	49.8	1	2	6	428,400 *
[57]	2009	65 nm CMOS	100.8	110.4	1	3	4.5	92
[47]	2009	130 nm CMOS	48.7	55.8	1.1	2	2	317,000
[64]	2009	65 nm CMOS	128.24	137	1.1	2	5.5	51,200
[69]	2009	350 nm SiGe BiCMOS	10.5	18.8	1.4	3	8.96	651,000
[70]	2009	350 nm SiGe BiCMOS	4.2	6.7	1.1	2	2.6	55,000
[70]	2009	350 nm SiGe BiCMOS	9.06	11.96	1.1	4	2.6	55,000
[71]	2010	350 nm SiGe BiCMOS	6.3	15.3	1.25	2	3.54	519,000
[50]	2010	65 nm CMOS	48.5	62.9	1.2	2	1.65	15,700
[61]	2011	90 nm CMOS	4.1	60	0.6	5	3.75	503,000 *

Table 2. *Cont.*

ILFD Paper	Year	Technology	f_{min} (GHz)	f_{max} (GHz)	Voltage Supply (V)	Division Factor	Power (mW)	Silicon Area (μm^2)
[63]	2011	90 nm CMOS	52.7	64.8	1.2	2	8.6	82,800
[72]	2012	130 nm SiGe BiCMOS	14.5	16.8	1.5	4	1.5	147,400 *
[52]	2013	65 nm CMOS	60.9	62.6	0.85	2	0.44	13,000
[67]	2017	180 nm CMOS	13	19	0.8	4	7.09	1,191,500 *
[46]	2017	65 nm CMOS	27.9	53.5	1	2	5.8	180,000
[48]	2017	90 nm CMOS	12	32	0.6	2	2.4	450,000 *
[65]	2017	130 nm SiGe BiCMOS	35	59.5	1.2	2	3.8	56,700
[53]	2018	90 nm CMOS	75.1	99	0.7	2	2.45	26,000
[56]	2018	65 nm CMOS	27.9	53.5	1	2	5.8	180,000
[56]	2018	65 nm CMOS	32.4	61.9	0.42	2	1.2	70,000
[68]	2019	180 nm CMOS	11.4	17.1	1.6	4	9.93	584,800
[54]	2019	65 nm CMOS	53.2	63	1.2	2	3.7	28,800
[66]	2020	65 nm CMOS	73.9	82.5	1	2	7.88	220,000
[58]	2021	28 nm CMOS	1	55	0.95	6	2.7	100
[55]	2021	40 nm CMOS	28.8	91.9	0.9	2	5.8	20,000
[59]	2022	28 nm CMOS	8	101.6	0.9	5	5.6	1300
[49]	2022	65 nm CMOS	23.3	31.02	0.6	3	5.18	490,000 *
[60]	2024	90 nm CMOS	26.2	35	1.2	3	0.366	18

* Bond pads included.

Table 3. TSPC frequency dividers comparison table.

TSPC Paper	Year	Technology	f_{min} (GHz)	f_{max} (GHz)	Voltage Supply (V)	Division Factor	Power (mW)	Silicon Area (μm^2)
[74]	2011	130 nm CMOS	-	12	1.1	8	0.748	1120
[78]	2012	180 nm CMOS	-	0.531	0.6	2	0.00435	72
[78]	2012	180 nm CMOS	-	0.525	0.6	3	0.00461	72
[82]	2012	180 nm CMOS	4	8	1.8	2	0.05	329
[82]	2012	180 nm CMOS	4	8	1.8	3	0.68	329
[107]	2013	90 nm CMOS	-	6	1.1	8	0.144	-
[83]	2013	130 nm CMOS	6	17.1	1.2	2	0.471	70
[83]	2013	130 nm CMOS	6	17.1	1.2	3	0.444	70
[108]	2016	130 nm CMOS	-	2.5	0.6	2	0.018	70
[81]	2019	45 nm CMOS	3	24	1	2	0.056	-
[81]	2019	45 nm CMOS	3	24	1	3	0.074	-
[76]	2021	65 nm CMOS	0.5	14.5	1.2	8/9	0.821	-
[15]	2022	22 nm FDSOI CMOS	16	70	0.8	4	0.35	3.4
[77]	2023	130 nm CMOS	0.5	6.8	1.2	4/5	0.96	12,410
[77]	2023	130 nm CMOS	0.5	8.5	1.2	8/9	1.16	12,410
[84]	2023	22 nm FDSOI CMOS	6.5	35	0.875	5	1.35	34

Comparing the silicon area is challenging because some papers report the size of the core only, while others report the area of the entire chip, bond pads included. For the latter case, the tables have asterisks next to the area values. The data reported in these tables allow for the following considerations.

CML frequency dividers are fast and can achieve high maximum frequencies, as shown in [29,33]. It is also worth remembering that they can generate quadrature output signals from the input signals. However, they tend to dissipate more power than other circuit solutions. Furthermore, they may occupy a large area.

ILFD circuits can reach frequencies equal to or higher than 100 GHz, with a power consumption of around 5 mW [55,57,59,64]. Despite their low power consumption, they occupy a large area due to the presence of inductors. Additionally, the presence of the LC tank makes the circuit intrinsically narrowband.

Finally, TSPC frequency dividers can consume less than 1 mW and occupy small areas, since they consist just of transistors, which exhibit lower footprints than passive devices. Their limitation is that they can only achieve modest maximum frequencies, although there are some exceptions [15]. Moreover, since the signals must pass through multiple logic stages, TSPC circuits can face delays and synchronization issues, particularly in high-speed designs.

Table 4 briefly summarizes all these considerations.

Table 4. Advantages and limitations of different types of frequency dividers.

Type	Principles	Advantages	Limitations
CML	Differential amplifiers and latches	High frequency Quadrature generation	High power dissipation
ILFD	Nonlinearities and LC tank	Low power dissipation High frequency	Small frequency range Large area (inductors)
TSPC	Clocked CMOS logic latches	Low power dissipation Small area	Limited by clock frequency Delay and synchronization

Figure 15 depicts another interesting comparison by plotting the maximum operation frequency against power dissipation for the frequency dividers reported in the tables above. The figure reveals that each frequency divider topology describes a distinct area on the plot, with only partial overlap between them. The overall trend aligns with expectations: higher operating speeds require greater power dissipation. This indicates that there is not a clear best option for designing a frequency divider, but the choice of typology depends on the specific requirements of the application.

Nevertheless, it can be remarked that the CML frequency dividers cover the entire frequency range, even at the cost of higher power dissipation. This makes them highly versatile and suitable for a wide range of applications, provided the power consumption is acceptable. On the other hand, TSPC frequency dividers excel in applications where minimizing power dissipation is a priority, because they stand out for their low power consumption, provided their lower operation frequencies are adequate for the application. Eventually, the ILFDs may be considered as a choice of compromise between high operating frequency and low power dissipation, making them an attractive choice when chip area is not a limiting factor.

As a possible remark, the application of Figure 15 to the CMOS cryogenic qubit controller described in [2] suggests that the X-band frequency divider, which offers several advantages to the architecture but at the cost of consuming nearly the entire dissipated power of about 100 mW (a value consistent with Figure 15), could be redesigned by adopting a TSPC topology. Figure 15 indicates that such a redesign could potentially reduce

power consumption by at least two orders of magnitude. Of course, in this case, synchronization and delay concerns associated with TSPC circuits would need to be carefully investigated at cryogenic temperatures.

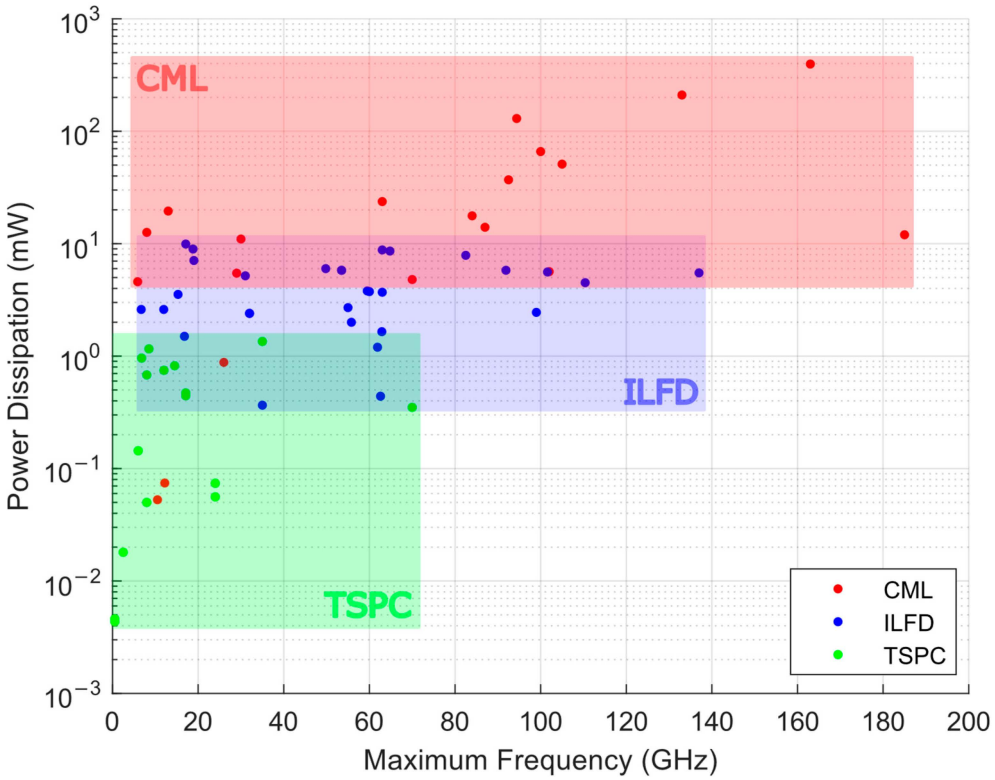


Figure 15. Maximum frequency against power dissipation for different topologies of frequency dividers reported in Tables 1–3.

The CML frequency divider presented in [2] is implemented using a 130 nm SiGe BiCMOS technology. Therefore, it may also be possible to scale the technology to reduce power consumption. For instance, the authors in [109] implement a cryo-CMOS receiver for scalable multiplexed qubit readout in a 40 nm CMOS technology. It incorporates a Phase-Locked Loop (PLL) that uses three divide-by-2 CML frequency dividers. The self-oscillation frequency of one of these dividers is approximately 14 GHz. Considering a maximum input clock amplitude of 0.4 V, the divider operates within a frequency range of 6.2 GHz to 20 GHz and consumes approximately 6 mW of power.

Another example of a frequency divider implemented in a circuit for cryogenic applications in quantum computing can be found in [110]. The circuit is implemented in 40 nm CMOS technology, and it utilizes a divide-by-2 solution based on two latches that form a register in negative feedback, which generates in-phase/quadrature differential phases. The latches are simple clocked CMOS types. Similarly, the authors in [111] use the same type of frequency divider as part of a cryogenic RF arbitrary waveform generator in 14 nm FinFET technology for qubit control.

Extending the frequency dividers comparison in Tables 1–3, Figure 16 plots process technology against the occupied silicon area. The figure demonstrates that all the divider topologies benefit from process advancements. However, as noted earlier, ILFDs occupy a larger area compared to other techniques, due to passive inductors and capacitors. Conversely, TSPC circuits are the most compact solution, while CML dividers fall in between. Therefore, TSPC topologies are the best in terms of area efficiency and scalability but lack the design flexibility of CML circuits. Indeed, TSPC frequency dividers operate

at a lower frequency than CML and cannot be biased or controlled to optimize their performance. In contrast, ILFDs are the least scalable and the most area-consuming.

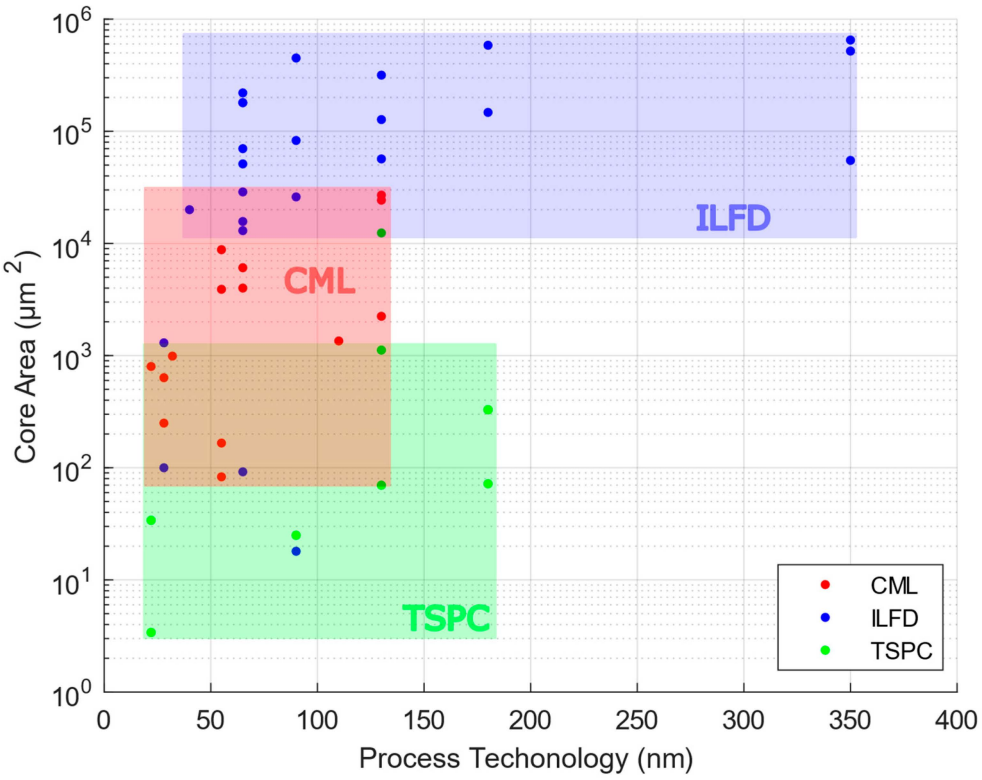


Figure 16. Process technology against silicon area for different topologies of frequency dividers reported in Tables 1–3.

Regarding process variations, CML dividers are the least sensitive to them, since they are biased and operate with constant current [112]. On the other hand, ILFDs are the least robust, as their performance heavily depends on passive inductors and capacitors, making them highly susceptible to fabrication processes. Finally, TSPC dividers stand in the middle and are moderately affected by process variations since they rely on digital logic and lack biasing control for compensation.

Another parameter for comparing frequency dividers is the residual phase noise. However, measuring it is challenging, as the phase noise of the input signal must be canceled out. To address this, an interferometric approach is used [113]. Two dividers are driven by the same input signal, and the phase of one of the outputs is shifted by 90°. Then, the two outputs are summed, and the resulting signal is measured using a phase detector. This value is divided by 2 to obtain the phase noise of a single divider.

Thanks to this technique, the authors in [114] measured the noise floor of a CML frequency divider obtaining −163 dBc/Hz for a carrier frequency of 78 GHz. Note that the noise floor is the value of phase noise in correspondence with the plateau region for a high frequency offset from the carrier frequency.

In addition, the authors in [115] performed this measurement on a CML frequency divider, achieving a noise floor of −155 dBc/Hz for a 5.5 GHz input carrier frequency. The authors in [116] detail the techniques to reduce the phase noise in CML dividers, primarily focusing on minimizing load capacitance, increasing current, reducing the size of load resistors, and enhancing input voltage swings. They measured a −160 dBc/Hz noise floor at an input frequency of 10 GHz.

TSPC dividers present similar values of phase noise, as shown in [117], which measures the noise floor of a TSPC circuit obtaining −163 dBc/Hz for a 1.5 GHz carrier frequency.

The authors in [118] investigate the phase noise behavior of ILFDs, measuring two dividers and obtaining noise floors equal to −133 dBc/Hz and −140 dBc/Hz at 9.8 GHz carrier frequency. This suggests that ILFDs exhibit worse phase noise performance compared to other divider typologies.

Since scaling down the technology node over the years is intrinsic to microelectronics; Figure 17 plots the amount of frequency dividers implemented in a given technology node versus the corresponding year interval. The dot diameter is proportional to the number of implemented circuits. The data are from Tables 1–3. The figure shows that the 55 nm, 45 nm, and, especially, 22 nm technology nodes exhibit the most promising trend for the future design of low-power frequency dividers. Meanwhile, the use of the 180 nm, 130 nm, 90 nm, and 65 nm technology nodes appears consolidated.

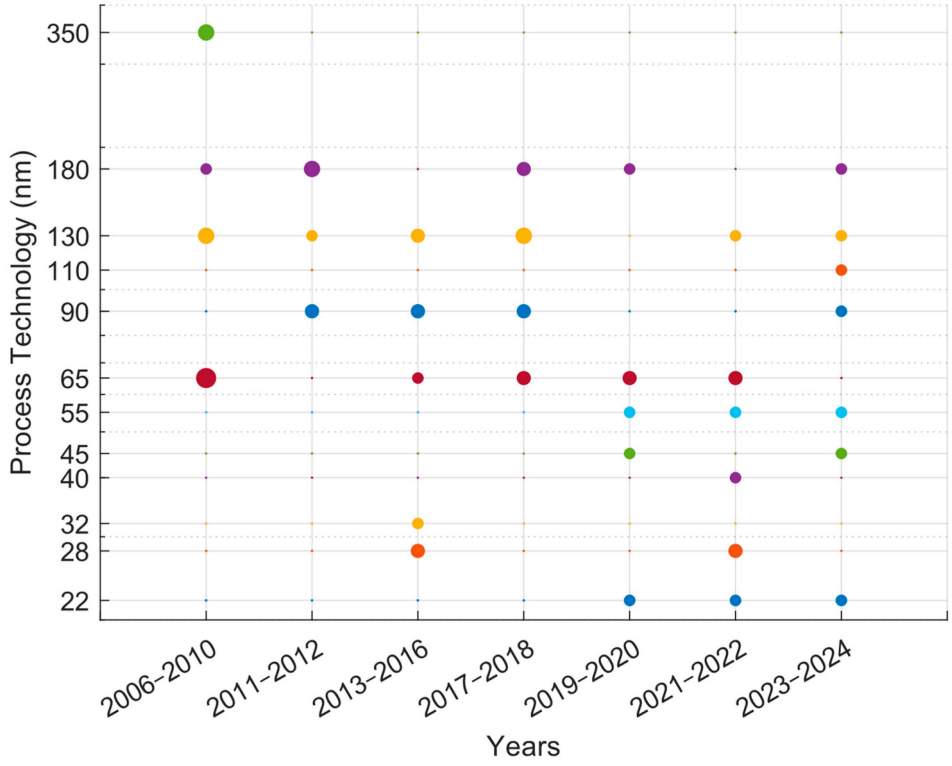


Figure 17. Process technologies adopted during the years for the frequency dividers reported in Tables 1–3. The different colors of the dots represent different process technologies.

7. Conclusions

This paper has reviewed three frequency divider types, Current Mode Logic (CML), Injection-Locking (IL), and True Single-Phase Clock (TSPC), with the aim of providing guidelines to help designers in selecting the most suitable solution.

The comparison of these frequency divider typologies highlights their trade-offs in speed, power consumption, and silicon area. CML dividers are fast and versatile but consume more power than the other types. ILFDs achieve high frequencies with low power but require large chip areas due to inductors. TSPC dividers are compact and energy-efficient but limited in speed. Process advancements improve all types, though ILFDs remain the least scalable. CML dividers are robust to process variations, while ILFDs are the most sensitive. A phase noise analysis shows ILFDs perform worse than CML and TSPC. Recent trends favor 22 nm and smaller technology nodes for low-power frequency divider designs.

Future research in low-power frequency dividers could focus on optimizing hybrid architectures that combine the advantages of multiple design techniques, such as TSPC,

ETSPC, and CML, to achieve better energy efficiency and higher operating frequencies. Advances in materials and transistor technologies, such as FinFETs [93], 3D integrated circuits [101,102], and nanosheets [119], could be further explored to reduce leakage currents and improve power efficiency further, leading to circuit solutions for ultra-low-power applications, like biomedical sensors [3,4].

Another application will be in 6G communication systems [8]. In particular, since 6G will cover the frequency band of 7–24 GHz [120], it could be interesting to design low-power frequency dividers for PLLs that cover this range. For instance, the authors of [121] present a 24 GHz integrated Phase-Locked Loop fabricated in 65 nm CMOS technology. It contains a 24 GHz CML divider-by-2 and an 8/9 prescaler, which is composed of three CML frequency dividers and one TSPC divider. This hybrid approach can be justified since, at higher frequencies, the CML solution is more suitable, while after that the frequency is divided and becomes lower, a TSPC can be used to further divide the signal, in accordance with Figure 15.

Also, research into alternative clocking methods, such as asynchronous [122] or adiabatic clocking [123], may also pave new ways for power savings in frequency divider designs. In addition, AI-based optimization techniques could help to automate the design process, enabling more efficient trade-offs between power, speed, and area [105,106]. Furthermore, it could be interesting to design low-power frequency dividers for THz applications [124], as current designs cover frequencies up to hundreds of GHz, but with relatively high power consumption [125,126].

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