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Off-State Breakdown Characteristics of AlGaN/GaN MIS-HEMTs for Switching Power Applications

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***Abstract*— A consistent description of breakdown characteristics in ohmic-to-ohmic, ohmic-to-substrate and HEMT structures has been achieved by means of device simulations for a depletion-mode AlGaN/GaN MIS-HEMT technology on Si substrate suited for power switching applications. For relatively short gate-drain distances or ohmic-to-ohmic spacings, source-drain punch-through is suggested to be the limiting breakdown mechanism in either HEMTs under off-state conditions or ohmic-to-ohmic isolation test structures, respectively. The mechanism ultimately limiting the HEMT off-state voltage blocking capability is instead the vertical drain-to-substrate breakdown for long gate-drain spacings. The latter phenomenon is induced, in HEMTs on a low-resistivity p-type substrate like those considered here, by the triggering of a high-field carrier generation mechanism rather than by carrier injection.**

***Index Terms*—Gallium nitride, high-electron mobility transistor, breakdown, device simulation.**

I. Introduction

Understanding the physical mechanisms limiting the off-state breakdown voltage in AlGaN/GaN HEMTs is of great importance for the application of these devices to switching power converters. However, it is far from being an easy task owing to structure and technology complexities, like the presence of field plates and back-barrier layers, and the possible role played by intrinsic defects and/or extrinsic impurities used for compensating the unintentional GaN conductivity. Correlating the HEMT breakdown characteristics with the high-voltage behavior of more simple, lateral and vertical test structures, as well as adopting device simulation as an interpretative tool can be useful in view of a more rapid and effective technology optimization.

In [1] and [2], we have analyzed the trap effects in AlGaN/GaN power MIS-HEMTs, pointing out the possible impact of buffer Carbon (C) doping on current collapse and threshold-voltage instabilities. In this paper, we address the off-state breakdown behavior of devices of the same technology by comparing measurements and device simulations, with the aim of further extending the capabilities of the device-to-system "virtual prototyping" approach to GaN technology modeling proposed in [3].

II. Test Devices and Numerical Models

The depletion-mode AlGaN/GaN MIS-HEMT technology adopted for this work features: low-resistivity p-type Si substrate, GaN buffer intentionally doped with C, 300-nm undoped GaN channel, $Al_{0.22}Ga_{0.78}N$ barrier, insulated gate, double field-plate structure.

Device simulations are carried out with the Sentaurus Device code by Synopsys Inc. C doping is modeled by means of acceptor- and donor-like traps associated to C_N and C_{Ga} states, respectively [4, 5]. In a previous work, trap-related dispersion effects and threshold-voltage instabilities have been associated in the devices under study to a dominant acceptor-like behavior of C doping related to C_N states [2], whereas negligible trapping effects have been found in devices where C doping resulted in the formation of perfectly self-compensating C_{Ga}-C_N states [1]. In the simulations of lateral ohmic-to-ohmic structures, the Ar isolation implant is modeled by following [6].

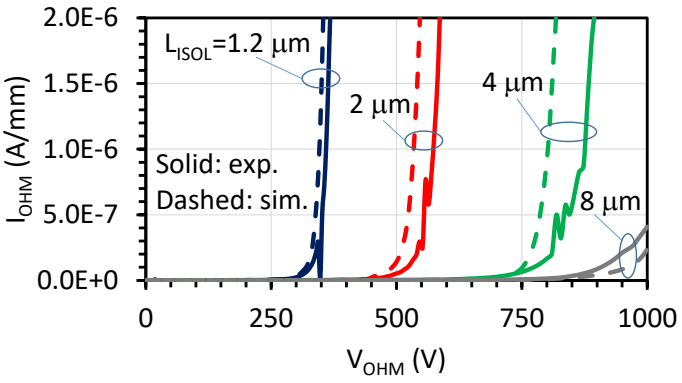


Fig. 1. Room-temperature experimental (solid) and simulated (dashed) IV curves in lateral, ohmic-to-ohmic isolation structures for different isolation implant lengths (L_{ISOL}). One of the ohmic contact and the substrate contact are grounded while a positive voltage V_{OHM} is applied to the other ohmic contact.

III. Lateral Isolation Structures

Room-temperature experimental and simulated breakdown characteristics of lateral isolation test structures are illustrated by Fig. 1, where one of the ohmic contact and the substrate contact are grounded while a positive voltage V_{OHM} is applied to the other ohmic contact. Lateral isolation structures having different isolation implant lengths (L_{ISOL}) and therefore different ohmic-to-ohmic distances are considered. As can be noted, simulations are able to reproduce correctly the breakdown-voltage scaling with L_{ISOL}.

Same satisfactory agreement is achieved at different temperatures, as shown in Fig. 2 for the two smallest L_{ISOL} values. As can be noted, increasing the temperature leads to an increase in the pre-breakdown leakage current level and to a decrease in the breakdown voltage.

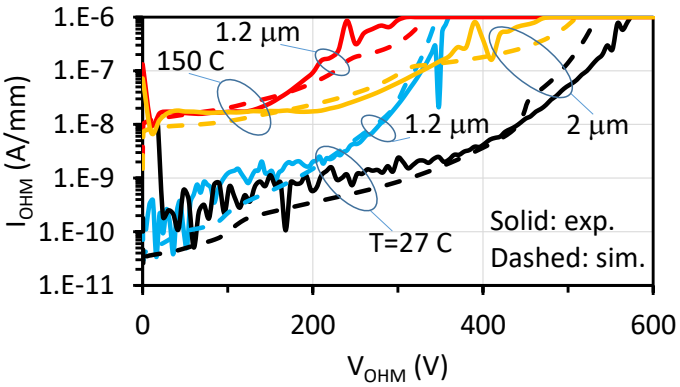


Fig. 2. Experimental (solid) and simulated (dashed) IV curves in lateral, ohmic-to-ohmic isolation structures for two different isolation implant lengths (L_{ISOL}) and two different temperatures. Same setup as for Fig. 1.

Simulations suggest that the physical mechanisms underlying breakdown in these lateral isolation structures are as follows: (i) lateral, ohmic-to-ohmic punch-through for $L_{ISOL} \leq 4$ µm and (ii) vertical, ohmic-to-substrate breakdown for $L_{ISOL} \geq 8$ µm.

The lateral ohmic-to-ohmic punch-through effect is illustrated by Fig. 3, showing the simulated electron current density distribution at different V_{OHM} voltages in a lateral isolation structure with L_{ISOL}=1.2 µm and a gap of 1.4 µm between the isolation implant and the ohmic contact (d_{ISOL}) on both sides. As the breakdown regime is reached (bottom plot in Fig. 3), a punch-through conductive path connects the positively-biased, ohmic contact (right contact in Fig. 3) to the 2DEG on the opposite side of the isolation implant. As a result, the total punch-through region length is $\approx L_{ISOL}+d_{ISOL}$.

It is worth emphasizing that the detailed description of trap states in the GaN channel and buffer layers resulting from our previous analysis of trap-related effects in this technology [2] turned out to be instrumental to achieving a "quantitative" breakdown prediction like that shown in Figs. 1 and 2. As a matter of fact, channel and buffer traps (along with the isolation implant) impact the pre-breakdown leakage current level as well as have an influence on the electric field under the ohmic contacts and, as a consequence of this, on their carrier injection properties in the breakdown regime.

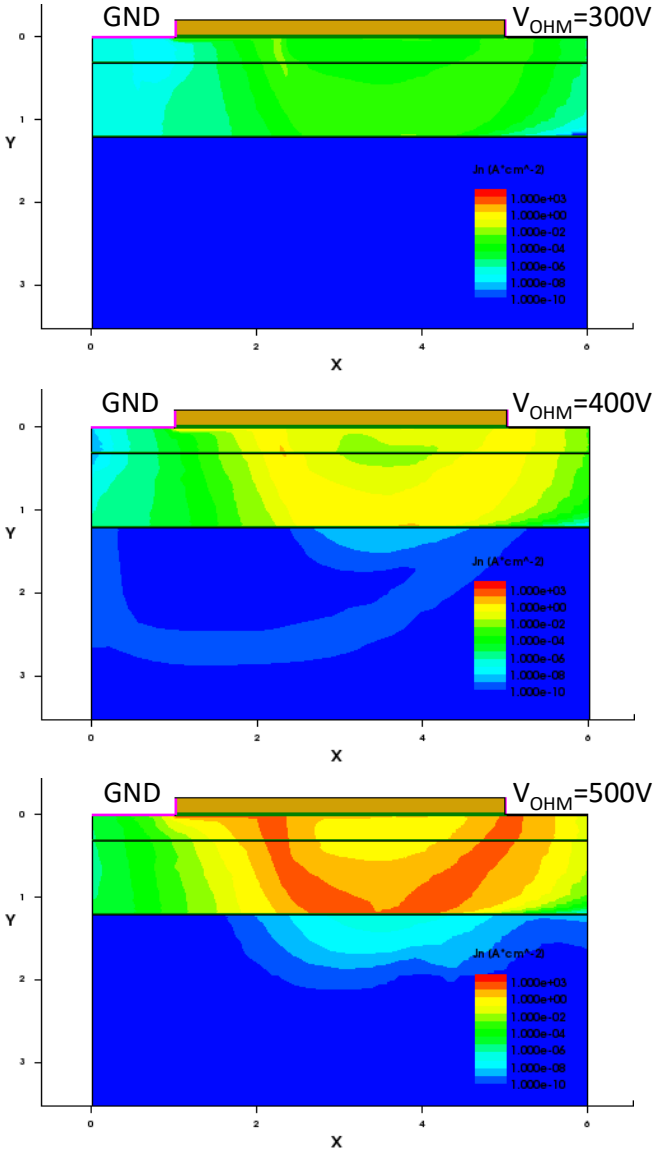


Fig. 3. Simulated electron current density plots in a lateral isolation structure with L_{ISOL}=1.2 µm and a gap of 1.4 µm between the isolation implant and the ohmic contacts on both sides. The left ohmic contact and the substrate contact (not shown in these enlarged plots) are grounded, while different positive voltages are applied to the right ohmic contact.

IV. Vertical Structures

The analysis of vertical, ohmic-to-substrate structures is illustrated by Figs. 4 and 5 for the case when a positive voltage is applied to the top ohmic contact (V_{TOP}) and to the substrate (V_{SUB}), respectively. A good agreement between measurements and simulations is achieved also for these structures. Apparent discrepancies in the pre-breakdown regime are related to measurement noise masking the actual leakage current level in the experimental curves. As can be noted, vertical breakdown

experimentally takes place at ≈950 V and ≈850 V for positive V_{TOP} and V_{SUB}, respectively (assuming a 10^{-5} A/mm^2 breakdown definition). Underlying breakdown mechanisms suggested by simulations are as follows.

When the positive voltage is applied to the top ohmic contact, high-field carrier generation in the GaN buffer layers where the electric field tends to accumulate at high voltages has a crucial role, electron injection from the substrate being inhibited by the low-resistivity p-type doping. In our simulations, we used band-to-band tunneling as high-field carrier generation mechanism in order to reproduce the experimental breakdown curves shown in Fig. 4.

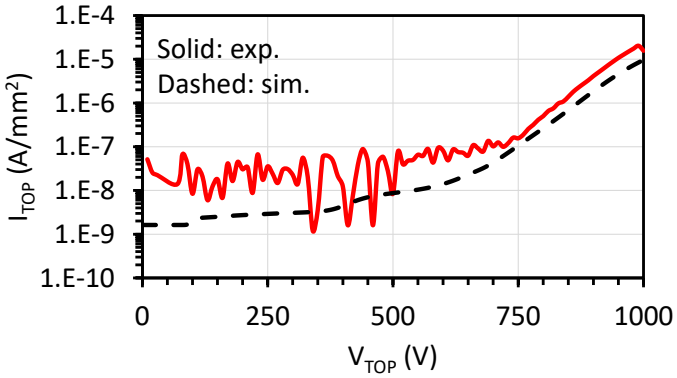


Fig. 4. Room-temperature experimental (solid) and simulated (dashed) IV curves in a vertical, ohmic-to-substrate structure with the positive voltage V_{TOP} applied to the top ohmic contact and the substrate grounded.

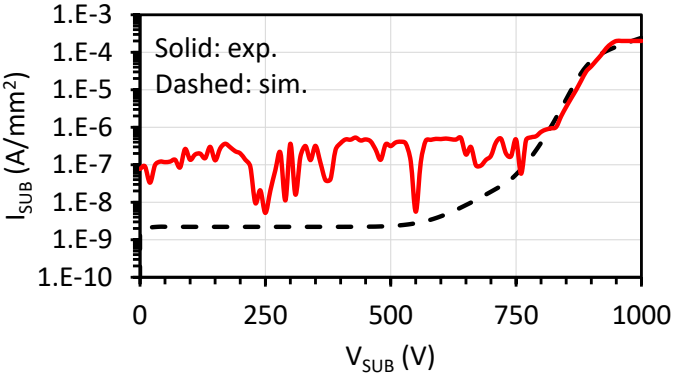


Fig. 5. Room-temperature experimental (solid) and simulated (dashed) IV curves in a vertical, ohmic-to-substrate structure with the positive voltage V_{SUB} applied to the substrate and the ohmic contact grounded.

When the positive voltage is applied to the substrate contact, breakdown is governed by a combination of electron injection from the top ohmic contact and high-field carrier generation in the buffer layer where most of the applied voltage drops.

V. HEMT OFF-STATE BREAKDOWN

Analyzed HEMT devices have a gate length (L_G) of 3 μm, a gate field plate of 1 μm and source-connected field plate of 3 μm.

The physical mechanisms leading to three-terminal, off-state breakdown in HEMT devices is suggested by simulations to be the same as in lateral, ohmic-to-ohmic isolation structures, i.e.: (i) lateral, source-drain punch-through for "short" gate-to-drain spacings (L_{GD}) and (ii) vertical, drain-to-substrate breakdown for "long" L_{GD} devices.

The source-drain punch-through effect is illustrated by Fig. 6, showing the simulated electron current density distribution for different drain-source voltages in a HEMT with L_{GD}=4 μm under off-state conditions (gate-source voltage of -10 V).

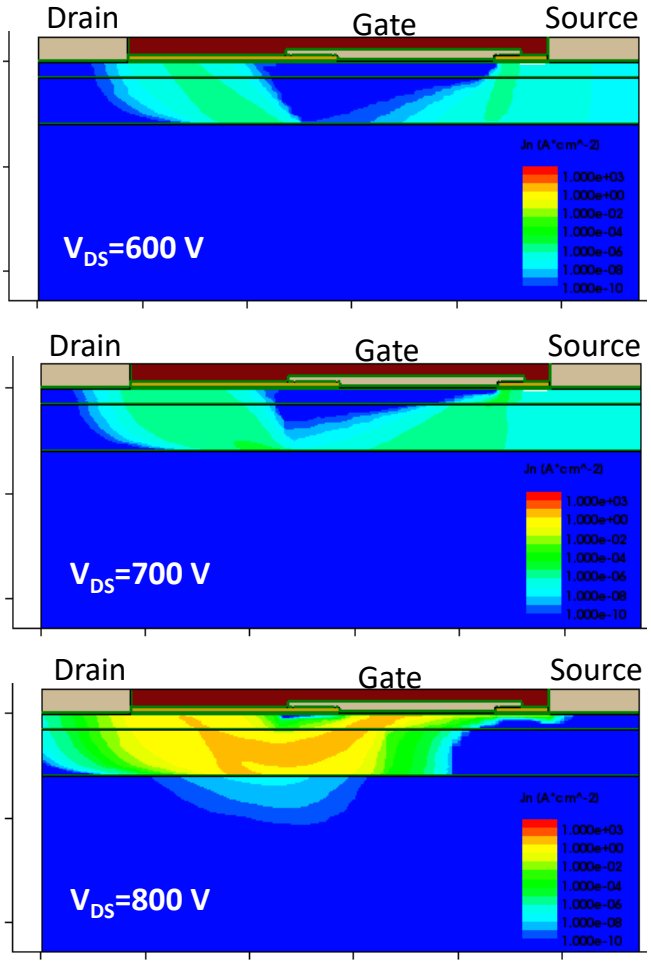


Fig. 6. Contour plot of the electron current density distribution in a HEMT with L_{GD}=4 μm for different drain-source voltages under off-state conditions (V_{GS}=-10 V).

Simulations show that, in lateral isolation structures, the applied ohmic-to-ohmic voltage drops over a total length of L_{ISOL}+d_{ISOL} (see Section III). In HEMTs, the critical length for breakdown, i.e. the distance over which the applied voltage drops laterally, is instead L_{GD} plus a fraction of the gate length

L_G. The breakdown voltage (V_{BD}) dependence on the critical length (L_{crit}) is illustrated by Fig. 7. For lateral isolation structures, L_{crit} is defined as $L_{crit}=L_{ISOL}+d_{ISOL}$, whereas for HEMTs the following two cases are considered: $L_{crit}=L_{GD}$ and $L_{crit}=L_{GD}+L_G/2$. As can be noted, similar V_{BD} scaling with L_{crit} is achieved in isolation and HEMT structures when the HEMT critical length is defined as $L_{crit}=L_{GD}+L_G/2$.

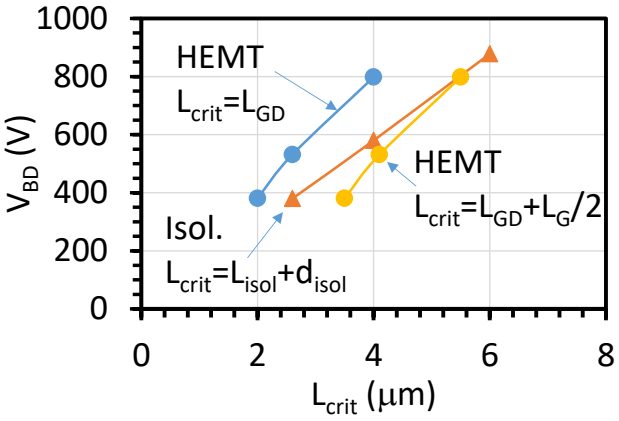


Fig. 7. Simulated breakdown voltages in HEMTs and ohmic-to-ohmic isolation structures as a function of the length (L_{crit}) over which the applied voltage mainly drops. Breakdown voltage is defined as the voltage at which the current equals the 10^{-5} A/mm level.

VI. Conclusions

In conclusion, a consistent description of breakdown characteristics in ohmic-to-ohmic, ohmic-to-substrate and HEMT structures has been achieved by means of numerical device simulations for a depletion-mode AlGaN/GaN MIS-HEMT technology on Si substrates suited for power switching applications. These results complement the capability of the GaN device-to-system virtual prototyping approach introduced in [3], while providing useful insights into breakdown mechanisms in GaN HEMT technologies.

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