University of Modena and Reggio Emilia

PhD in Industrial Innovation Engineering

XXXII Cycle

Current Source Inverter Solutions for Renewable Energies Sources and Electric Drives for Aerospace Applications

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Sommario della Tesi

In questo lavoro di tesi è stata analizzata una particolare architettura di convertitore elettronico di potenza DC/AC denominata CSI ("Current Source inverter"). Storicamente, questa topologia è stata largamente impiegata per l'azionamento di macchine elettriche in media tensione. Il CSI, rispetto ai più diffusi Voltage Source Inverter (VSI) è caratterizzato da maggiori perdite di conduzione dei propri transistor ma è in grado di garantire un'affidabilità più elevata, siccome il corto-circuito di un qualunque mezzo-ponte (gamba dell'inverter) non determina una rottura (come nelle comuni architetture VSI), ma bensì è una normale condizione operativa all'interno di un periodo di commutazione della modulazione PWM. Una peculiarità importante di questa topologia è il suo funzionamento intrinseco come step-up nel caso la sorgente in ingresso al convertitore sia costituita da una sorgente di tensione continua seguita da un induttore. In questo lavoro si sono investigate modifiche topologiche rispetto all'architettura classica del CSI, nuove strategie di controllo e modulazioni PWM al fine di incrementare l'efficienza di conversione, ridurre il contenuto armonico indesiderato delle proprie correnti di uscita e limitare le correnti di modo comune. Cercando cosi, di rendere la topologia competitiva in applicazioni Industriali. Differenti soluzioni topologiche e di controllo del CSI sono state studiate per due differenti applicazioni: convertitori DC/AC grid-connected senza isolamento galvanico per sistemi fotovoltaici e per azionamenti elettrici per applicazioni aerospaziali. Nell'ambito dei convertitori DC/AC

grid-connected sono state proposte soluzioni sia per sistemi trifase, sia per sistemi monofase. In particolare grazie all'aggiunta di uno o più transistor e a modulazioni PWM dedicate è stato possibile ridurre le perdite di conduzione, il contenuto armonico delle correnti iniettate in rete e la corrente di dispersione verso terra. Nella seconda applicazione come azionamento elettrico, si è investigato l'impatto della topologia nel mondo aerospaziale, proponendo una nuova strategia di controllo che permette di controllare la macchina elettrica unicamente attraverso un'architettura tradizionale CSI con sorgente di tensione continua e induttore serie, senza l'ausilio di un ulteriore convertitore DC-DC che regola la corrente in ingresso al CSI. Sfruttando la caratteristica intrinseca di innalzamento della tensione d'uscita dell'azionamento, sono stati progettati dei motori elettrici che potendo lavorare a tensioni più elevate e con basso contenuto armonico grazie al filtro d'uscita intrinseco del CSI, è possibile realizzare delle macchine con densità di potenza elevata, aspetto molto interessante in ambito aerospaziale.

Summary of the Thesis

In this thesis work, a particular DC / AC power converter architecture called CSI ("Current Source inverter") was analyzed. Historically, this topology has been widely used for driving medium voltage electrical machines. The CSI, compared to the more widespread Voltage Source Inverter (VSI) is characterized by higher semiconductor conduction losses but is able to guarantee a higher reliability as the short-circuit of any half-bridge (inverter leg) does not cause a break (as in VSI architectures), but rather it is a normal operating condition within the pattern of PWM modulation. An important peculiarity of this topology is its intrinsic operation as voltage step-up when the input source of the converter consists in a DC voltage with an inductor in series. In this work, some topological variations respect to the classical CSI architecture were investigated along with new control strategies and Space Vector Modulation(SVM) in order to increase the conversion efficiency, to reduce the undesired harmonic component of output currents, and to mitigate the common mode current. Different CSI topologies and control strategies have been designed for two different applications: DC / AC grid-connected converters without galvanic isolation for photovoltaic applications and electric drives for aerospace applications. In Grid-connected applications, DC / AC converter solutions have been proposed for three-phase and single-phase systems. In particular, thanks to the addition of one or more transistors and dedicated SVM, it was possible to reduce conduction losses, the harmonic component

in the injected currents into the grid and the ground leakage current. In the second application, the impact of the CSI topology in the aerospace environment was investigated. The proposed control strategy allows to control the electric machine using only the traditional CSI architecture with a DC Voltage source and with an inductor in series, without the aid of an additional DC-DC converter that regulates the input current of the CSI. Taking advantage of the intrinsic step-up voltage characteristic and very low high frequency harmonic content of the output phase voltages (thanks to the intrinsic CSI output filter), electric motors can be designed for higher voltages allowing higher power density, very interesting aspect in the aerospace field.

Introduction

It is well-known and widely accepted that today the world of power electronics is dominated by the Voltage Source Inverter (VSI). Its success is probably due to its simplicity, the general availability of voltage sources and the high efficiency that it can achieve. This popularity has in turn also influenced how the semiconductor industry has developed, where a focus on devices tailored for VSI usage has been the norm in the last years. Thus, products such as depletion devices (normally off) and without reverse voltage blocking capability have seen widespread marketing and use. On the other hand, the current source inverter (CSI), while never very popular, has in the last two decades, been pushed even more into obscurity. Based on the common, pre- wide bandgap era technologies and topologies, then applications and scenarios where CSIs would give an inherent advantage are few and far between. This trend is today however changing. The quest for higher efficiencies and power density, combined with new technological developments is 'opening' up the playing field to CSIs. The CSI's inherent characteristics of intrinsic voltage boost, a low output voltage THD and the absence of electrolytic capacitors are all extremely important benefits, can result in a resurrection of the CSI in the very near future. It is perceived that certain niche applications can benefit greatly from the development and implementation of CSIs. For example, any high-speed drive that is limited with a low voltage source, e.g. for transport applications, will be an ideal breeding ground for the next generation of CSI

converters. Small-scale photovoltaic system as well would benefit from the intrinsic voltage boost capability.

This thesis presents a study, whose main aim is to investigate and define the real potential of CSI-based power converters for renewable energy exploitation and transportation technologies. In the first chapter the classic CSI topology is presented with an ideal DC input current source and with a DC input voltage source followed by a DC inductor. The main peculiarities of CSIs along with its dedicated Space Vector Modulation is described. After this short recall of CSI operation principles the thesis is divided in two parts related to transformerless grid-connected converters for renewable energy sources and electric drives for aerospace applications.

The second chapter analysed different CSI topologies for three-phase and single phase grid-connected systems for photovoltaic applications. The new topologies are evaluated in terms of output current distortion, ground leakage currents and semiconductors power losses.

The third deal with the use of CSIs in aerospace applications in order to increase reliability and power density of the electric machine for particular applications as cabine pressurization in which the machine works most of the time at high speed. In this framework the fourth chapter proposes an alternative DC Link current control strategy that allows to avoid the use of the DC-DC Front-End converter when the machine operates at high speed, i.e. when the line-to-line machine voltages are higher than the DC input voltage source. This allows to reduce power losses and to increase power density. All the topologies, proposed controls and SVM strategies are simulated in Matlab-Plecs environment and validated experimentally. The last two chapters are the result of a collaboration with University of Nottingham (UK) and University of Nottingham-Ningbo China. The author has been for five mounts as visiting student at the University of Nottingham-Ningbo China.

During the PhD course, the author investigated other research topics related to power electronics and electric drives about resonant DC-DC Converter, Wireless Power Transfer and electric drives for PM machines and piezoelectric actuators. These research activities are not reported in this thesis in the interests of clarity and conciseness. In the following Publications section it is possible to see the research products of these activities.

Publications

Journal papers

1. C.M. Verrelli, P. Tomei, E. Lorenzani, G. Migliazza, F. Immovilli, "Nonlinear tracking control for sensorless permanent magnet synchronous motors with uncertainties", Control Engineering Practice, Volume 60, 2017, Pages 157-170, ISSN 0967-0661.

2. E. Lorenzani, F. Immovilli, G. Migliazza, M. Frigieri, C. Bianchini and M. Davoli, "CSI7: A Modified Three-Phase Current-Source Inverter for Modular Photovoltaic Applications," in IEEE Transactions on Industrial Electronics, vol. 64, no. 7, pp. 5449-5459, July 2017.

3. E. Lorenzani, G. Migliazza, F. Immovilli and G. Buticchi, "CSI and CSI7 current source inverters for modular transformerless PV inverters," in Chinese Journal of Electrical Engineering, vol. 5, no. 2, pp. 32-42, June 2019.

4. E. Lorenzani, G. Migliazza, F. Immovilli, C. Gerada, H. Zhang and G. Buticchi, "Internal Current Return Path for Ground Leakage Current Mitigation in Current Source Inverters," in IEEE Access, vol. 7, pp. 96540-96548, 2019.

5. Madonna V., Migliazza G., Buticchi G., Giangrande P., Lorenzani E. and Galea M." The rebirth of the Current Source Inverter: advantages for aerospace motor design." IEEE Industrial Electronics Magazine

6. V. Madonna, P. Giangrande, G. Migliazza, G. Buticchi and M. Galea, "A Time-Saving Approach for the Thermal Lifetime Evaluation of Low Voltage Electrical Machines" in IEEE Transactions on Industrial Electronics TIE.2019.2956378, December 2019

Conference papers

7. G. Migliazza, E. Lorenzani, F. Immovilli and C. Bianchini, "Ground leakage current reduction in single-phase current source inverter topologies," IECON 2016 - 42nd Annual Conference of the IEEE Industrial Electronics Society, Florence, 2016, pp. 2325-2330.

8. E. Lorenzani, G. Migliazza, F. Immovilli, C. Bianchini and G. Buticchi, "Ground leakage current in PV three-phase current source inverter topologies," IECON 2017 - 43rd Annual Conference of the IEEE Industrial Electronics Society, Beijing, 2017, pp. 4221-4226.

9. A. Reatti, F. Corti, L. Pugi, M. K. Kazimierczuk, G. Migliazza and E. Lorenzani, "Control Strategies for Class-E Resonant Inverter with Wide Load Variation," 2018 IEEE International Conference on Environment and Electrical Engineering and 2018 IEEE Industrial and Commercial Power Systems Europe (EEEIC / I and CPS Europe), Palermo, 2018, pp. 1-6.

10. E. Lorenzani, G. Migliazza and F. Immovilli, "Ground Leakage Current Mitigation for Three-Phase Current Source Inverters," 2018 IEEE Energy Conversion Congress and Exposition (ECCE), Portland, OR, 2018, pp. 3694-3699.

11. R. Fornari, G. Migliazza, E. Lorenzani and F. Immovilli, "Critical Aspects of Hybrid PFM-PWM Operation in LLC Converters For Electric Vehicles," 2018 IEEE International Conference on Electrical Systems for Aircraft, Railway, Ship Propulsion and Road Vehicles and International Transportation Electrification Conference (ESARS-ITEC), Nottingham, 2018, pp. 1-6.

12. V. Madonna, P. Giangrande, G. Migliazza, G. Buticchi and M. Galea,

"On the Thermal Insulation Qualification of Low Voltage Electrical Machines," IECON 2019 - 45th Annual Conference of the IEEE Industrial Electronics Society, Lisbon, Portugal, 2019, pp. 7115-7120.

13. D. Benatti, G. Migliazza, R. Fornari, E. Lorenzani and G. Buticchi, "Analytical Equivalent Circuit Model for Series-Compensated Wireless Power Transfer Systems," IECON 2019 - 45th Annual Conference of the IEEE Industrial Electronics Society, Lisbon, Portugal, 2019, pp. 4177-4182.

Patents

14. Migliazza Giovanni ; Lorenzani Emilio ; Larcher Luca, "Amplificatore per il pilotaggio di un carico capacitivo", hdl.handle.net/11380/1152336

Chapter 1

Current source Inverter for Grid-Connected Photovoltaic Systems

In this chapter modified topologies based on traditional CSI are presented and analysed with the use of different figures of merit: Total Harmonic Distortion (THD) of injected output currents, ground leakage currents due to parasitic capacitances of Photovoltaic panels and semiconductor power losses.The first section shows the operation principles of the CSI. In the second section a modified CSI topology, named CSI7, is analysed in detail together with different SVM strategies. In the third section the performance of the CSI7 topology is compared to the traditional CSI. The fourth section shows an additional modification of CSI7 topology allowing to mitigate the ground leakage current. The last section shows a CSI solution dedicated to single phase grids, named CSI5, able to strongly reduce the ground leakage current respect to a basic single phase CSI.

1.1 Operation principles of Current Source Inverter

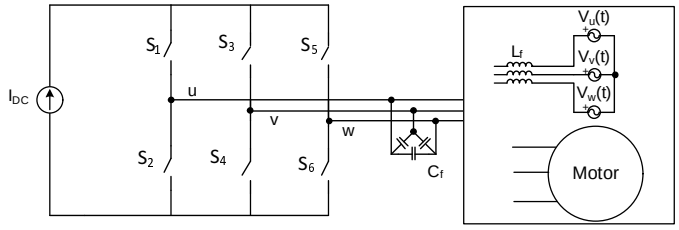


Figure 1.1. Ideal Three-phase CSI topology

The "Current Source Inverter" (CSI) as the name suggests, is a power electronics converter whose input is a current source. It allows to converts the input direct current into an alternate current. Figure 1.1 shows two possible applications of the CSI as grid-connected converter and electric drive. With an ideal DC current input the output voltage of the inverter is independent from the load because the inverter controls the output current [4]. The classic CSI topology, needs six reverse blocking power switches, that can be obtained by the series connection of a no reverse-blocking transistors + diode, resulting in higher conduction losses.

Since in practical applications the DC input source is a voltage source a DC inductor has to be inserted in series, as shown in Figure 1.2. The electrostatic energy storage provided by electrolytic capacitors in VSIs is replaced by this magnetic energy storage. This could allow to increase the lifetime of the power converter. Since the short-throw of a leg of the power converter is not a failure condition but an admissible switching state (as shown in the next section) also the reliability of power system could significantly increase.

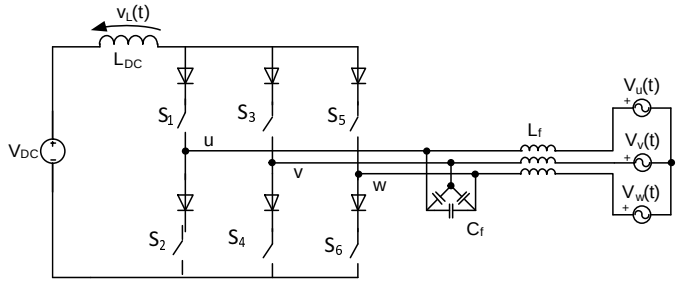


Figure 1.2. Three-phase CSI topology with DC Voltage Bus

1.1.1 Space Vector Modulation in CSI

The traditional Current Source Inverter has nine possible switching states which impose to the load nine current vectors, that can be classified as Null vectors and Active vectors, as listed in Tab 1.1 [4]. During the six Active vectors, for example during the vector I_6 the switch $S1$ and $S4$ are on, and the current I_{DC} flow on $S1$ and $S4$ and then back to the DC source resulting $i_u = I_{DC}$ and $i_v = -I_{DC}$. There are three Null switching vectors defined $I_{0,1}$, $I_{0,2}$, and $I_{0,3}$ which correspond to the short-circuit of one CSI leg. For example the Null vector $I_{0,1}$ means that switches $S1$ and $S2$ are in on state and the other four switches of the inverter are off, leading to $i_u = i_v = i_w = 0$. During the application of a Null vector, in case of a DC voltage Source, there is an increase of energy stored in the DC inductor.

Table 1.1. Space Vector Modulation

Type	Space Vector	On-vector Switch	Inverter PWM Current		
			i_u	i_v	i_w
Null vector	$I_{0,1}$	$S1, S2$	0	0	0
	$I_{0,2}$	$S3, S4$			
	$I_{0,3}$	$S5, S6$			
Active vector	I_1	$S1, S6$	I_{DC}	0	$-I_{DC}$
	I_2	$S3, S6$	0	I_{DC}	$-I_{DC}$
	I_3	$S3, S2$	$-I_{DC}$	I_{DC}	0
	I_4	$S2, S5$	$-I_{DC}$	0	I_{DC}
	I_5	$S5, S4$	0	$-I_{DC}$	I_{DC}
	I_6	$S1, S4$	I_{DC}	$-I_{DC}$	0

Active current vectors, corresponding to the values of Tab.1.1, are illustrated in Figure 1.3. The desired current vector applied to the load, I_{ref}, has to be inside the circle inscribed in the hexagon. The desired vector can be obtained as a linear combination of the permissible Active and Null vectors showed in Tab. 1.2.

Table 1.2. Space Vector Modulation

Space Vector	Current Space Vector
$I_{0,1}$	$\bar{i} = 0$
$I_{0,2}$	$\bar{i} = 0$
$I_{0,3}$	$\bar{i} = 0$
I_1	$\bar{i} = (2/\sqrt{3})e^{j5\pi/6} i_{dc}$
I_2	$\bar{i} = (2/\sqrt{3})e^{-j5\pi/6} i_{dc}$
I_3	$\bar{i} = (2/\sqrt{3})e^{-j\pi/2} i_{dc}$
I_4	$\bar{i} = (2/\sqrt{3})e^{-j\pi/6} i_{dc}$
I_5	$\bar{i} = (2/\sqrt{3})e^{j\pi/6} i_{dc}$
I_6	$\bar{i} = (2/\sqrt{3})e^{jpi/2} i_{dc}$

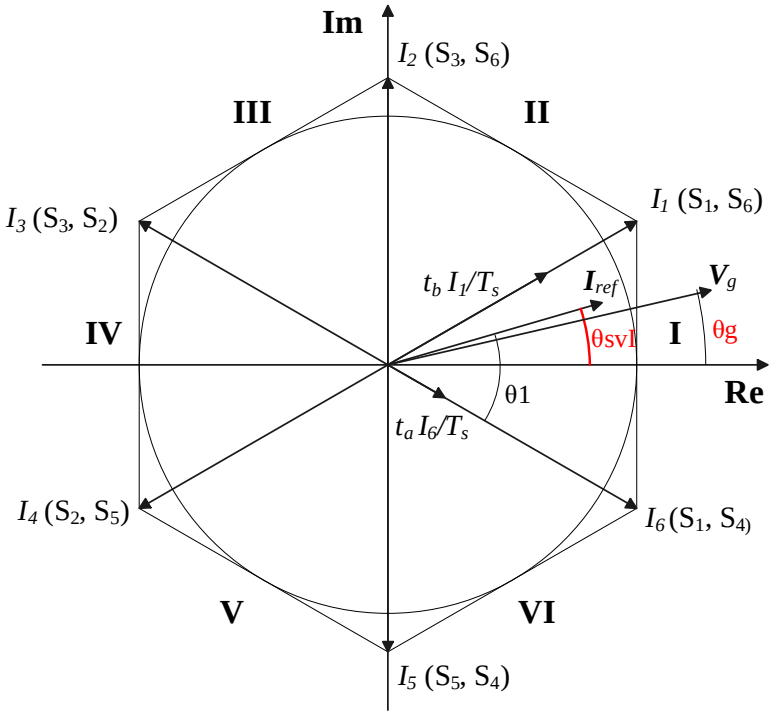


Figure 1.3. Space vector representation.

The CSI operates by chopping the DC current to the output terminals through a PWM scheme. Several modulation strategies have been proposed in literature [5, 6]. The initial step is the definition of the modulation index, which is described by (1.1.1), where $|i_{ref}|$ is the module of the current space vector and i_{dc} is the DC input current.

$$m = \frac{|i_{ref}|}{i_{dc}} \tag{1.1.1}$$

In Fig. 1.3, the maximum value of m is $\frac{\sqrt{3}}{2}$, defined by the inner circle of the hexagon and therefore the range of m can be described by (1.1.2).

$$0 < m < \frac{\sqrt{3}}{2} \tag{1.1.2}$$

With reference to the same figure, any given current reference vector I_{ref} is obtained as a time weighted linear combination of the active vectors of the corresponding sector (or sextant): t_a and t_b for the two active vectors and t_z for the Null vector (d_a and d_b represent simply the normalized time intervals with respect to the switching period T_s) as shows in Equations 1.1.3 .The basic sequence of the active and Null vectors is shown in Figure 1.4.

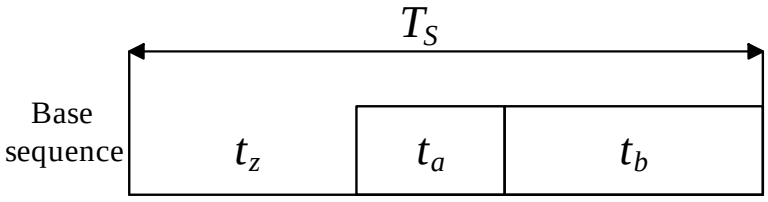


Figure 1.4. Bases sequence of active and Null states

The angle $\theta 1$ is used for the computation of the dwell time intervals t_a and t_b, while θ_{SVI} is the angle of the current space vector I_{ref} which is used to compare it with the angle of grid voltage space vector $\vec{V_g}$, named θ_g.

$$\begin{cases} t_a = d_a T_s \\ t_b = d_b T_s \\ t_z = T_S - (t_a + t_b) \end{cases} \tag{1.1.3}$$

The space vector of the grid voltage can be represented as $\vec{V_g} = V_g e^{j\omega t = j\theta_g}$, while the space vector of the injected current is $\vec{I_{ref}} = I_{ref}^{j\theta_{SVI}}$. When the converter works in unity power factor operation $\theta_g = \theta_{SVI}$.

Equation 1.1.4 shows the calculation of the normalized time intervals of the two active vector which border the current space vector, where θ_1 is the angle of the current space vector referred to the active state vector placed in clockwise respect to it (see Fig. 1.3).

$$\begin{cases} d_a = 2/\sqrt{(3)} m \sin(\frac{\pi}{6} - \theta_1) \\ d_b = 2/\sqrt{(3)} m \sin(\frac{\pi}{6} + \theta_1) \end{cases} \tag{1.1.4}$$

1.2 A Modified Three-phase Current Source Inverter

This section shows a modified CSI topology named CSI7 that presents an additional power switch. This topology with a suitable SVM strategy, tailored for grid-connected PV applications, allows to reduce the semiconductor power losses and the distortion of injected output current.

The Current Source Inverter (CSI) topologies are evaluated in three-phase grid-connected for photovoltaic applications as shown in Figure 1.5. PV energy conversion has attracted the interest of industry and academia, especially due to increased international environmental awareness and local policies that incentive the owners of grid-connected photovoltaic plants. Despite the end of these advantageous policies, PV technology is still growing because of the ease of installation (being a full solid-state solution) and of the possibility of minimizing the exchange of energy with the electric grid by the adoption of local energy storage. The usual installation of photovoltaic (PV) panels implies the presence of a metal frame to which the solar cells are assembled. In the case of large installation, the metal frame constitutes a sizeable part of the structure. For safety reasons, the metal surfaces must be grounded, to prevent the electrocution of the personnel and to detect faults towards ground. Although necessary from the point of view of the safety, because of the presence of a parasitic capacitance (C_{PV}) between the solar cells and the metal frame, it is possible for ground leakage current to flow through the circuit composed by the ground connection of the electrical grid (R_g), the equivalent PV parasitic capacitance, C_{PV}, and the power converter as shown in Figure 1.5. The magnitude of this ground leakage current can be high and can constitute a safety

risk itself, if precautions are not taken [7].

This ground leakage current, that is a common-mode current (named i_{cm}), increases the distortion of the output injected current and decreases the efficiency of the inverter. The issue of the ground leakage current has been addressed extensively for the VSI topologies, where usually modified structures of the power electronics are adopted [8, 9]. Also passive solutions based on common mode filters have been proposed [10].

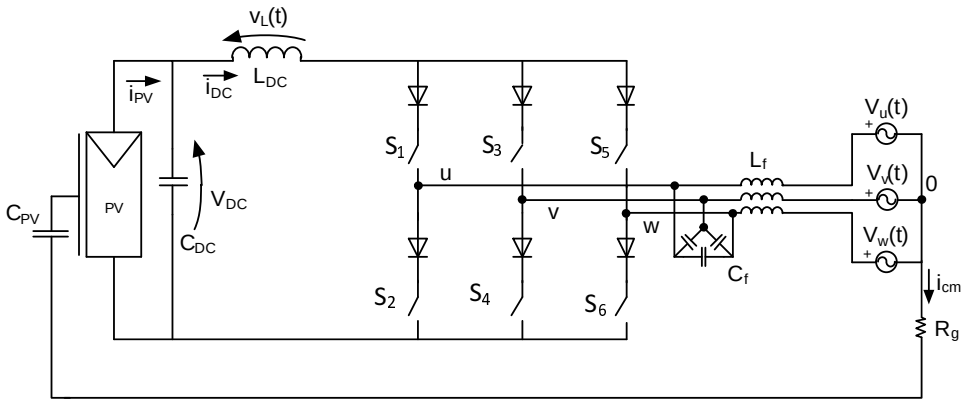


Figure 1.5. Three-phase CSI topology for Photovoltaic application.

Because of the development of the semiconductor devices and market needs, reverse blocking devices did not achieve performance comparable to the devices without reverse voltage blocking capabilities. This has forced the CSI adopters to add diodes in series to the switches, with the obvious drawback of increasing the conduction losses.

In conventional VSI topologies, to avoid using bulky Electrolytic Capacitors (EC), which have a lifetime much shorter than PV modules. In order to be economically viable, the lifetime of grid-connected converters has to be comparable to that of PV panel, e.g. 20+ years. The CSI topology can allow to increase the power converter lifetime thanks to the replacement of the DC Link capacitances with an inductor, that in case of three-systems and high switching frequency can be of usable size.

This is one of the most challenging requisites because the power converter is installed in a harsh environment with high operating temperature and thermal cycling. Another feature of PV inverter topologies is the strong requirement to guarantee a low ground leakage current due to the presence of the undesired parasitic capacitance between the PV modules and the mounting frame connected to earth [11], [12]. This is of particular interest in case of thin-film PV modules that are characterized by a large parasitic capacitance up to 1uF/kWp, order of magnitude greater than crystalline silicon PV modules [13], [14].

1.2.1 CSI7 Topology

The traditional CSI topology is characterized by higher semiconductor power losses with respect to VSI topologies [15], especially in the case of high step-up voltage operation. In fact the six power switches (made by series connected (MOSFETs,SiC,IGBT or GaN) + diodes, Fig. 1.5) constituting the classic CSI topology must withstand both the DC output current of the PV Panel and the high voltage of the grid. The resulting conduction power losses are quite high since at any given time the input DC Link current flows always through 2 power switches and 2 diodes. Therefore efficiency of the CSI improves as the DC input voltage increase. Semiconductor power losses remain virtually unchanged in presence of a very large variation of the input DC voltage, depending only on the DC input current value.

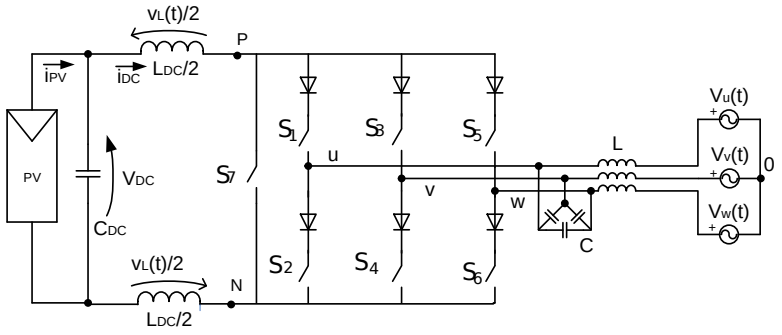


Figure 1.6. Three-phase CSI7 topology.

Since the CSI performance is evaluated in a PV String Converter applications, the conduction power losses would be intrinsically very high. The introduction of the power switch S_7 (see the modified topology in Figure 1.6), allows to reduce the number of power semiconductors in series during the short circuit of the input DC inductance from four devices to only one(Null Vector). If a high step-up voltage ratio is required, this short-circuit time is a very large fraction of the total PWM period. With reference to the space (state) vector representation of Fig. 1.3, the six power switches $S_1 - S_6$ can be driven as in a classic CSI solution when the converter apply the six active (non-Null) space vectors (SV), $I_1 - I_6$, see [16]. Null vectors are traditionally obtained by short-circuiting the DC-link through a leg short-circuit. In the CSI7 solution these Null vectors are not employed: the Null state vector is created by turn on the additional power switch S_7. All the active vectors ($I_1 - I_6$) are defined by the switches configuration $S_1, S_2, S_3, S_4, S_5, S_6$ of the bridge.

In the CSI7 topology, shown in Fig. 1.6, a simple power switch (MOSFET, IGBT, SiC or GaN) without a diode in series for S7 can be adopted only if the voltage across it is always positive from drain (collector) to source (emitter). Figure 1.7 shows the instantaneous phase voltages and the respective SV sectors of current space vector when the CSI7 operates at unity power factor. Figure 1.8 details the instantaneous values of the line-to-line voltages, v_{uv} e v_{uw} for sector I. The following analysis is conducted for sector I, but the assumptions are valid also for the others SV sectors. The evolution of line-to-line voltages during sector I of the space vector current is fundamental in order to understand the circumstances leading to a negative voltage applied across switch S7, whereas a diode must be inserted in series.

During the sector I, with PF=1, the two active vectors applied are I1 (S1 and S6 ON) and I6 (S1 and S4 ON). During the application of these two switches configuration, the voltage across the switch S7 is respectively equal to voltages

v_{uv} (I1) e v_{uw} (I6) plus two voltage drops across the inductive part (L) of the output filter. It is important to point out that during the active vectors the inductive voltage drops determine a positive incremental contribution of the voltage across S7 and therefore neglecting these voltage drops represents a worst case scenario in order to find the operating condition range in which this condition is satisfied.

Figure 1.8 not only shows that the line-to-line voltages v_{uv} e v_{uw} are positive in case of unity power factor but also that there is a phase margin equal to $+\pi/6$ and $-\pi/6$ between the space vector of the grid voltage and the injected grid current, $\phi = \theta_g - \theta_{SVI}$, in which the voltage across S7 is still positive. This implies that the CSI7 converter can operate with a simple switch for S7 (without the diode in series) with a PF that can decrease down to 0.866, thus giving the capability for a reasonable amount of inductive and capacitive reactive power injection.

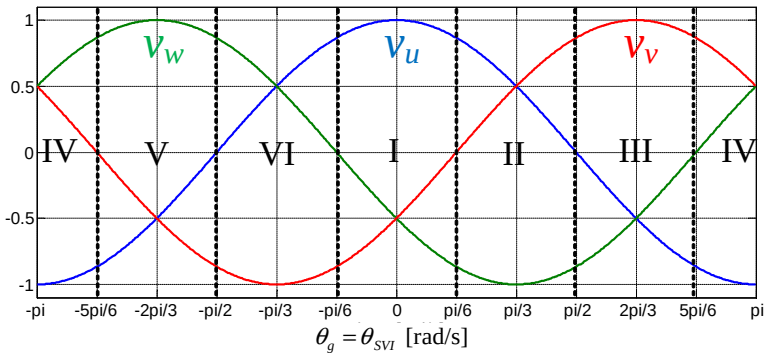


Figure 1.7. Grid phase voltages with sector numbers of the space vector current in case of unity power factor.

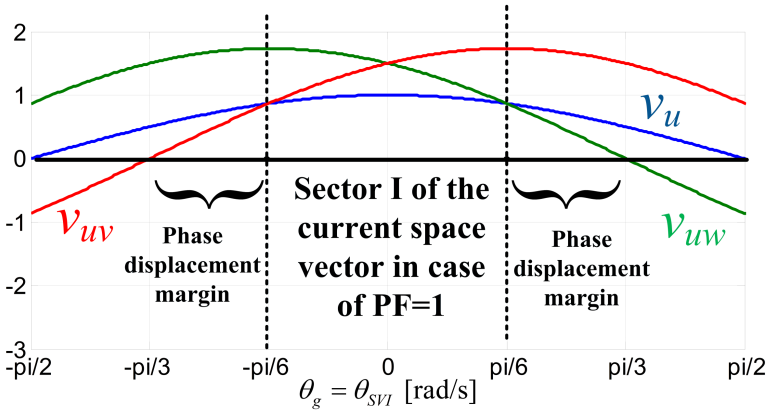


Figure 1.8. Power factor operation range to guarantee a positive voltage across S7 during the I sector.

1.2.2 CSI issue analysis and proposed solution

To maintain control linearity, the SV space of Fig. 1.3 is limited to the inner circle of the hexagon, hence the modulation index value ($m = |I_{ref}|/I_{DC}$) is restricted to $0 \leq m \leq \sqrt{3}/2$. Different SV sequences are available, from basic ones [17], to more sophisticated ones, aiming at minimizing switch commutations and switching losses or at reducing distortion in supply current [18]. The PWM strategy to be implemented should minimize THD of the injected output current and power losses, guaranteeing overlap times between CSI commutations to avoid voltage spikes.

1.2.2.1 Output Current Distortion

Because the output filter is a CL-type filter which has a lightly damped second-order characteristic, it shows a lightly damped resonant behavior: output glitches and spectral components at the resonant frequency can cause the output filter to ring .Glitches can be caused during the transition of the current space vector from one SV sextant to the adjacent or by an undesired path of the output current of CSI due to the introduction of overlap times. This glitch effect can be attenuated using an active damping as presented in [19], [20]. In

the present work, instead of implementing passive or active damping solutions for CL resonance of the output filter, the modulation that was identified aims at minimizing the excitation of the output CL filter by avoiding glitches generation. The first cause of glitch generation can be eliminated with an accurate choice of SV sequence for every sextant in order to avoid the consecutive application of the same active state vector at end of one sextant and at the beginning of the next as well as avoiding transition between two active state vectors that are more than $\pi/3$ apart. The second cause is eliminated with the introduction of the power switch S_7 since the overlap time between an active state vector and a null state vector is obtained by widening its ON-time: i.e. leading and lagging the ON state with respect to the other active vector transitions.

1.2.2.2 Overlap Time

The overlap time in CSI inverter modulation is required in order to avoid momentary DC input inductor open circuit, a condition symmetrical to dead time introduction in VSI inverter modulation. In CSI operation an overlap time, t_{ov}, is needed for safe commutations between current space vectors. This overlap time causes distortion in the injected current waveforms if it is not accurately compensated. In case of a high boost factor, the modulation index m is so low (this assumption will be detailed in the following section) that it makes difficult any finer subdivision of the active times t_a and t_b.
An effective overlap time compensation can be obtained only if every active state vector is separated from the others by the null state vector which represents the dominant state vector during overlapping. Figure 1.9 shows the effect of overlap time t_{ov} on the commutation strategy. The overlap time is introduced as the firing signal of power switch S_7. Because the null state is dominant with respect to other active vector, the effective active vector times for the alternated sequence are:

$$\begin{cases} t_a{}' = t_a - 2t_{ov} \\ t_b{}' = t_b - 2t_{ov} \end{cases} \tag{1.2.1}$$

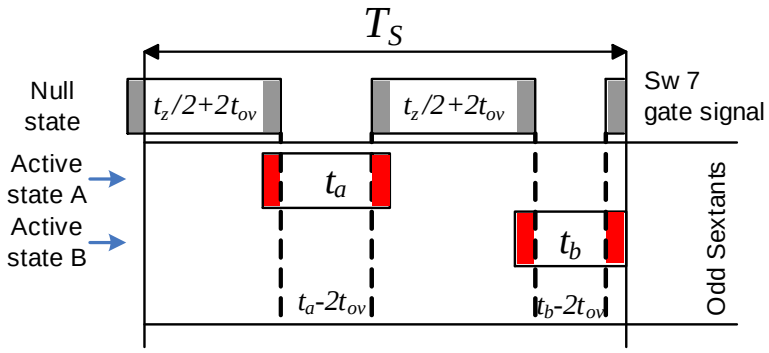


Figure 1.9. Alternated sequence - overlap time t_{ov} effect (scale exaggerated for demonstration purpose).

1.2.2.3 Alternated SVM Sequence

A further degree of freedom of the SVM is the sequence with which the vectors are generated. In this thesis two possibilities are analysed, the Base sequence and the advanced Alternated sequence, see Fig. 1.10. In this figure t_a and t_b represent the dwell time intervals for the application of the two active vectors (current vectors A and B) and t_0 the time interval for the application of the Null vector in a switching period T_S. The Alternated SVM sequence must be customized depending on the odd/even sextant type and a specific transition sequence must be implemented to avoid resonance excitation of the output filter [21]. Dwell times are calculated according to the SVM. As it is shown in the following simulation and experimental subsections, the Alternated sequence avoiding glitches during sextant transitions allows to reduced output current distortion.

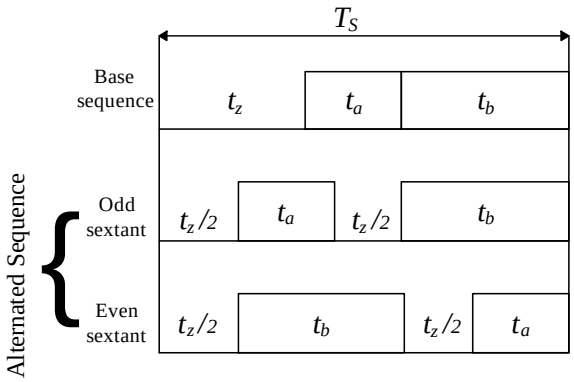


Figure 1.10. Comparison of the commutation sequences: Base (top) and Alternated (bottom)

Thanks to the overlapping time of implemented Alternate SVM, the additional switch S7 is switched on while the full-bridge is still generating an active vector. This operation draws the DC current to S7, releasing the full-bridge switches, whose current goes to zero. When these switches are turned off at the end of the overlapping time, S7 is already carrying the whole DC current, so they are switched off with Zero Current Switching. In the case of Base SVM this does not happen for the turn-off of one transistor (S1-S6) during the transition from current vector A to current vector B.

The power switch S_7, besides ensuring a strong reduction of conduction power losses, also helps to avoid glitches generation since it is the only contributor to null state vector generation, because of S_7 conduction voltage drop is lower than the other reverse-blocking switches (transistor with series connected diode). By using S_7 together with the alternate commutation sequence, the overlap time ensures that S_7 is active during every turn-on and turn-off transient of the reverse-blocking switches (S_1 to S_6). This ensures that all the commutations of S_1 to S_6 happen under zero current (ZCS), as all the input DC current flows on S_7. Under these operating conditions S_7 is the only device operating with hard switching. The SV modulation times t_a, t_b were compensated accordingly, by adding $2t_{ov}$ to them. The advantage of the latter is that, with the introduction

of the additional switch S7, the null vector can be applied by S7 alone, while all the other transistors are turned Off.

1.2.3 CSI control strategy for PV Inverter

In order to extract the maximum available energy from the PV source, the output voltage of the PV string is controlled by a Maximum Power Point Tracker (MPPT). Therefore the first goal for assessing the performance of a PV CSI concerns its capability to operate in steady state conditions under a large input DC voltage variation. A steady state condition with an almost constant input DC current, i_{DC}, can be obtained when the mean value of the voltage across the input inductor L_{DC} of the CSI is null. Since the injected grid current is always at the same frequency of the grid voltage and thanks to the symmetry of the grid generator the evolution of the voltage across L_{DC} is the same for every SV sextant. The integral of $v_L(t)$ over a switching period, T_s in the sextant I of the SVM is shown in eq. (1.2.2).

$$\begin{aligned}\int_t^{t+Ts} v_L(t)\mathrm{d}t = \int_t^{t+Ts} ((V_{DC} - v_{wu}(t))t_a + \\ +(V_{DC} - v_{vu}(t))t_b + V_{DC}t_z)\mathrm{d}t = 0\end{aligned} \tag{1.2.2}$$

It is then possible to compute the voltage V_{DC} which satisfies eq. (1.2.2) obtaining a linear relationship between output voltage and the modulation index, as reported in [22].

This property is very important in order to limit the current ripple of I_{DC}, which shows only an harmonic at the switching frequency. Figure 1.11 shows the relationship between the modulation index m and the V_{DC} at different power factor operation.

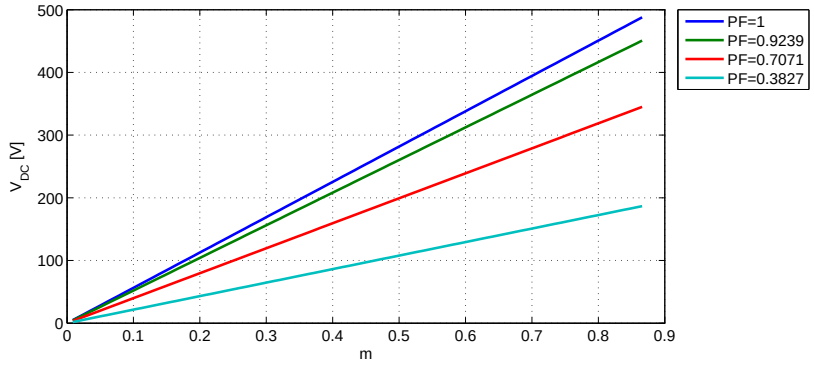


Figure 1.11. Relation between modulation index and V_{DC} of the PV module.

The CSI performance presented previously indicates the feasibility of the CSI to operate with a photovoltaic source as the output voltage of the PV panel can be properly controlled by a MPPT algorithm.

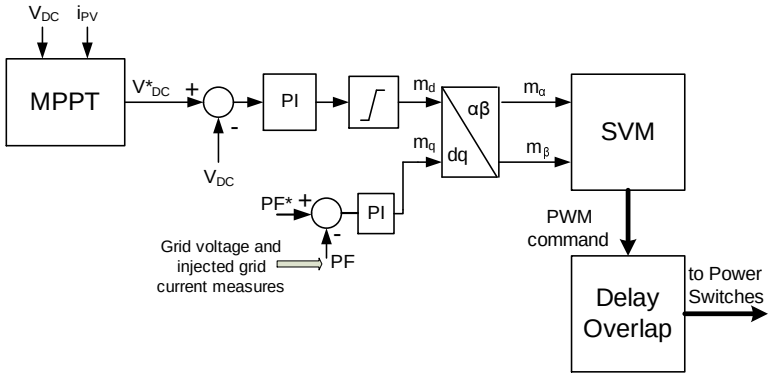


Figure 1.12. Schematic of the proposed control.

Figure 1.12 shows the proposed CSI control. The input voltage control loop employs a PI regulator which provides the modulation index m_d, proportional to the active current injected into the grid. In other words, the amplitude of the ideal active current can be obtained as $I_d = m_d * I_{DC}$. The modulation index m_q can be fixed to zero or varied to further fine-tune the power factor of the CSI: in fact the presence of the capacitance-inductive output filter determines reactive power absorption. The modulation indexes m_α m_β are computed by Park's transform and used as input of the SVM. The two indexes are used to determine

the polar coordination of the current space vector: module $m = \sqrt{m_\alpha^2 + m_\beta^2}$ and angle $\theta = arctg\frac{m_\beta}{m_\alpha}$.

1.2.4 Numerical simulations

The CSI7 topology and modulation control strategy was numerically modeled in Matlab Simulink environment, employing PLECS plugin for the power converter stage. The simulated system incorporated a PV array and the power converter architecture shown in Fig. 1.6. The control of the CSI7 converter was implemented as shown in Fig. 1.12, for simplicity m_q was fixed to zero. The simulations were carried out in order to verify the effectiveness of the adopted SVM in terms of injected grid current distortion without the insertion of the parasitic equivalent capacitance C_{PV}. Table 1.3 summarizes the parameters used for simulations and following experimental results.

Figure 1.13 shows the phase injected grid current and voltage in case of base PWM and traditional CSI solution. Figures 1.14 and 1.15 show the waveforms of the injected grid currents with the Alternated switch sequence respectively without the overlap compensation and without the change in the SV sequence for odd and even sextants. The lack of this sequence inversion determines an excitation of the output CL filter that involves an unacceptable injected current distortion. Figure 1.16 shows the phase injected grid current with the adopted SVM strategy: in this case the waveform distortion is drastically reduced. It is important to stress that no active damping techniques were used neither in simulations nor in following experiments.

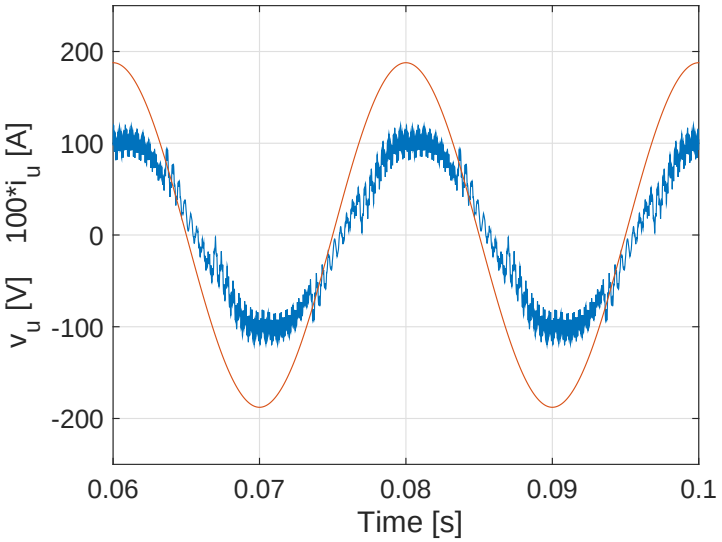


Figure 1.13. Simulation results. Phase grid voltage and injected current, THD 11.88%) in case of base PWM for traditional CSI topology.

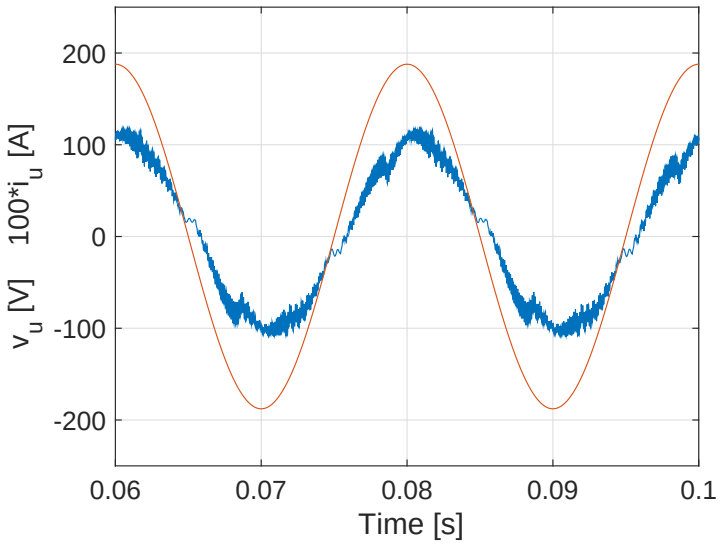


Figure 1.14. Simulation results. Phase grid voltage and injected current , THD 8.2%) in case of adopted SVM for CSI7 topology without overlap compensation.

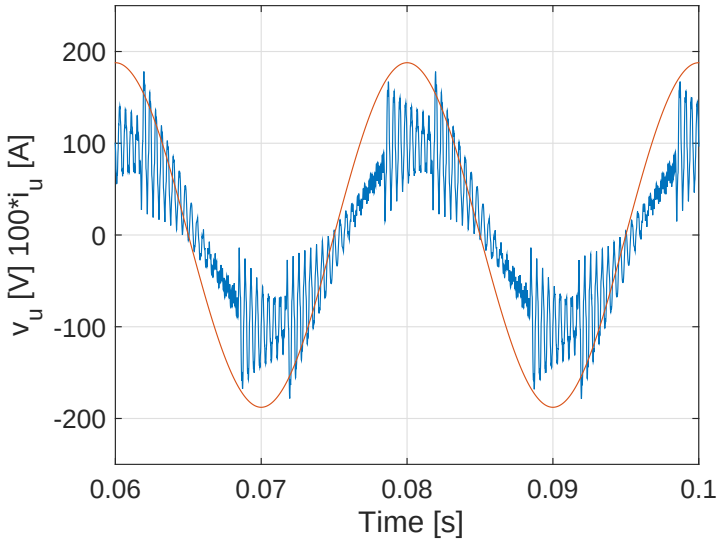


Figure 1.15. Simulation results. Phase grid voltage and injected current , THD 25%) in case of adopted SVM for CSI7 topology without the inversion sequence.

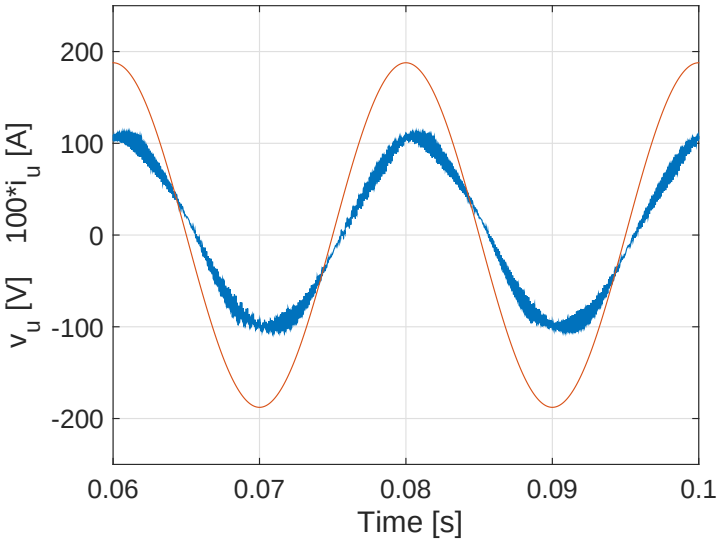


Figure 1.16. Simulation results. Phase grid voltage and injected current , THD 4.4%) in case of adopted SVM for CSI7 topology.

As stated before, by introducing the overlap time with S_7 in the alternate commutation sequence, S_7 is active during every turn-on and turn-off transient of

the reverse-blocking switches (S_1 to S_6). As a consequence, all the commutations of S_1 to S_6 happen under zero current (ZCS), as the input DC current flows on S_7. Figure 1.17 shows switches commutations inside the first sextant: as it can be seen S_7 is the only device operating with hard switching. The same considerations apply for all the other sextants. Furthermore, in order to avoid useless commutations, S1 is kept constantly on in the sextant, even during null state (S7 on). Since S_7 is the only switch that can manage hard switching commutations, the use of a band gap transistor is the best choice. In case of low m large part of semiconductor power losses are localized in this switch and therefore also the thermal design has to be accurate.

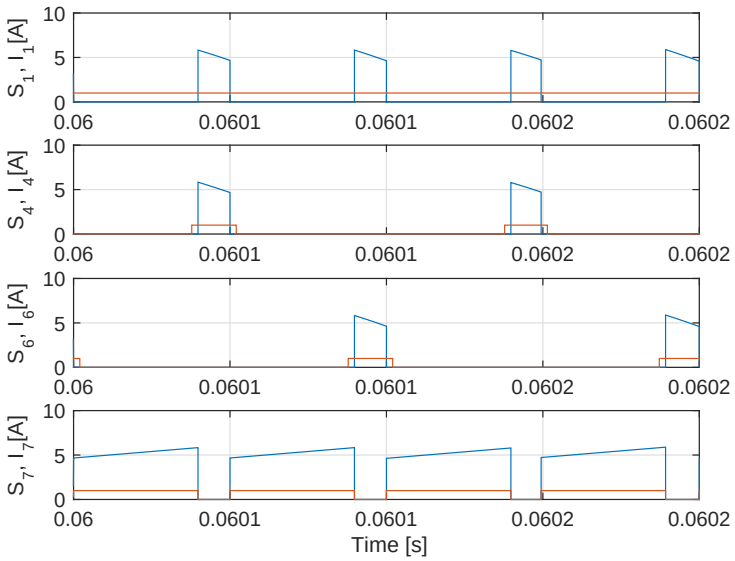


Figure 1.17. First sextant operation: switching sequence and device currents of S_1, S_4, S_6 and S_7.

1.2.5 Experimental Results

A laboratory prototype was built to evaluate all the theoretical assumptions. A TMS320F28069 controller was used to implement the space vectors modulations of the traditional CSI and of the CSI7. In addition to this, all the

algorithms for the injection of electric power into the grid were implemented. The experimental setup is shown in Figure 1.18. The CSI7 was connected to a variable DC Voltage Source. A three-phase transformer was connected between the grid and the outputs of CSI7. The neutral of the transformer secondary winding was connected to earth through the resistance R_g, which simulates the ground resistance of a three-phase grid. An equivalent capacitor simulates the parasitic capacitance to earth of PV panels and it was connected between the ground and the negative pole of the DC voltage source. Through this equivalent capacitor and R_g flows the ground leakage current of the PV system. A Digital Power Analyzer PPA 5530 was used for harmonic analysis and efficiency measurements: THD was measured by the same instrument and was computed from the series of the first 100 harmonics.

Table 1.3 summarizes the conditions of the experimental tests. The power switches used in the converter prototype are the commercial IGBT IHY15N120R3 1200V 15A. To further reduce conduction power losses, a SiC MOSFET can be used for S7. It is important to put in evidence that the power semiconductors were not chosen in order to maximize the efficiency. The measure of the efficiency should be mainly considered only as performance comparison of different modulation strategies running on the same hardware.

Figure 1.19 shows a picture of the power board of the laboratory prototype. The input inductor L_{DC} was split in two input inductors in order to obtain a better performance in terms of output common-mode voltage and therefore lower ground leakage current [23].

The first set of experiments was conducted in order to verify the effectiveness of the adopted SVM for CSI7 topology, in particular the overlap compensation and the alternated sequence in the odd and even sextants. In these first experiments the equivalent parasitic capacitance C_{PV} that was not inserted. The performance of the CSI7 solution was compared to the classic CSI topology

Table 1.3. Experimental and Simulation parameters.

Name	Description	Value	Units
V_{DC}	DC voltage source	60	V
V_g	rms line-to line grid voltage	230	V
f_g	grid frequency	50	Hz
f_s	switching frequency	10	kHz
t_{ov}	overlap time	2	μs
L_{DC}	input inductance	2	mH
L	AC Filter inductance	1.4	mH
C	AC Filter capacitance	1	μF
R_g	ground resistance	4.7	Ω

driven by the base SVM: this represents the reference case. Figure 1.20 shows the grid voltage and current corresponding to 348 W of injected electric power. The THD of the injected current was measured equal to 11%.

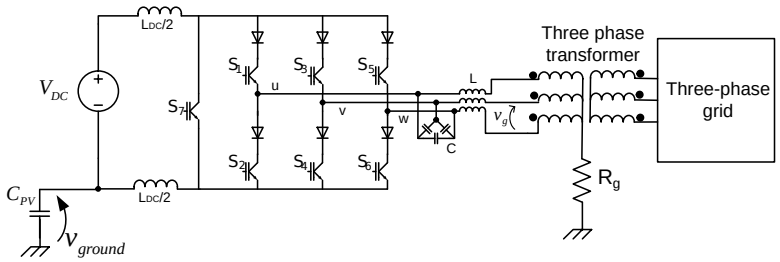


Figure 1.18. Experimental test setup.

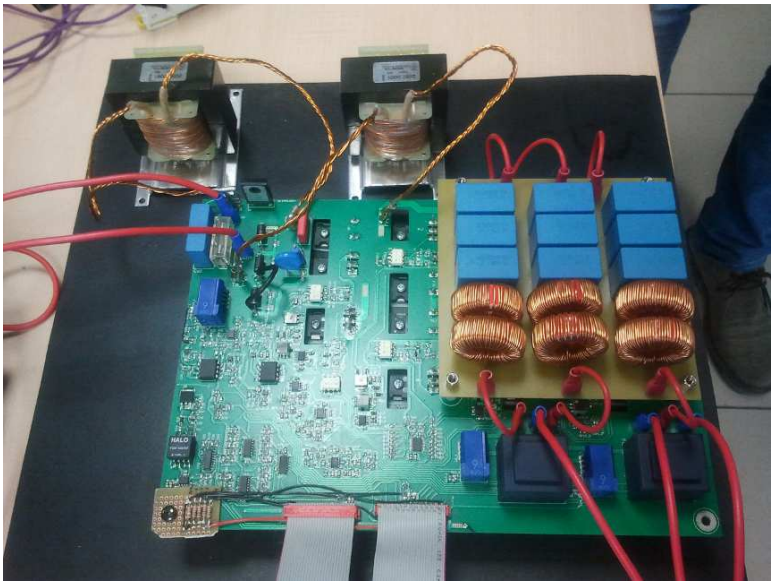


Figure 1.19. Power board of CSI7 laboratory prototype

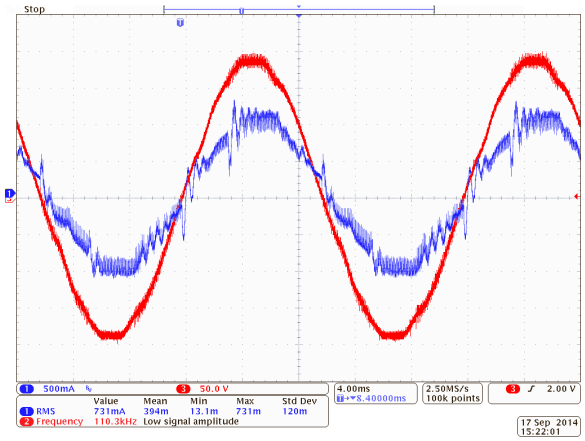


Figure 1.20. Experimental results. Phase grid voltage (red trace, 50V/div) and injected current (blue trace, 0.5 A/div, THD 11%) in case of base SVM.

The effectiveness of the adopted SVM for the CSI7 topology was assessed through the following tests. For a fair comparison with respect to the previous reference case, the same value of injected electric power was used, i.e. 348 W. Figure 1.21 shows SVM performance when the overlap compensation was not applied, while in Fig. 1.22 the inversion sequence was not applied. The THD of the injected currents result 8.9% and 11.5% respectively. Figure 1.23 shows

the performance of the complete SVM reaching a THD=4.5%.

Eventually table 1.4 compares the THD of simulation and experimental results in the same operating conditions. The only significant difference in the comparison is related to the use of adopted ($0A0B$) PWM strategy without the inversion sequence; in this case the presence of distributed/parasitic resistances in the system allows to realize a passive damping for the output CL filter. Passive damping that is not present in the simulation environment.

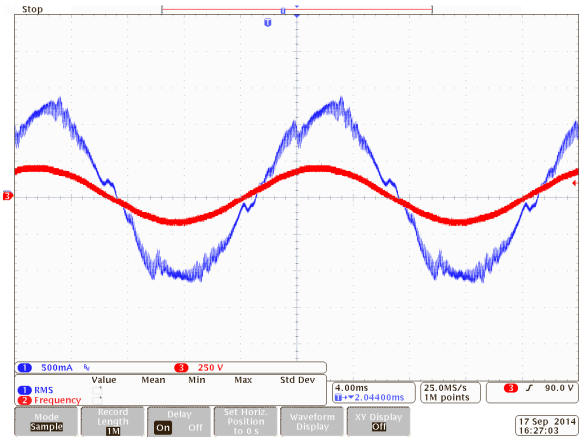


Figure 1.21. Experimental results. Phase grid voltage (red trace, 250V/div) and injected current (blue trace, 0.5 A/div, THD 8.9%) in case of adopted SVM for CSI7 topology without overlap compensation.

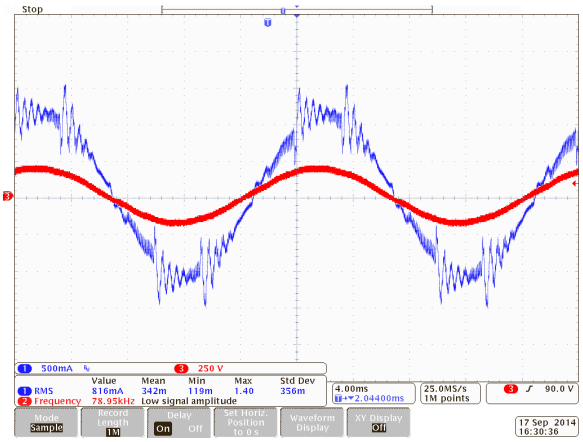


Figure 1.22. Experimental results. Phase grid voltage (red trace, 250V/div) and injected current (blue trace, 0.5 A/div, THD 11.5%) in case of adopted SVM for CSI7 topology without the inversion sequence.

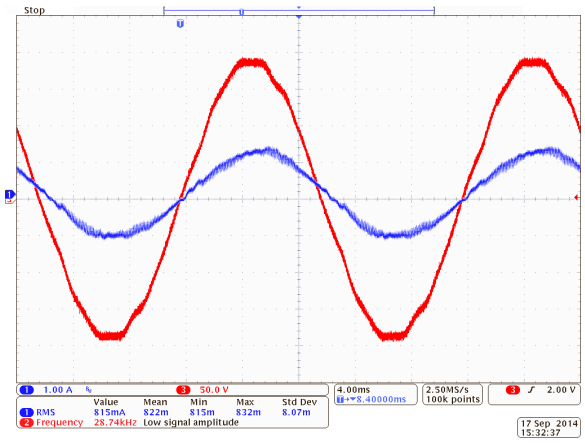


Figure 1.23. Experimental results. Phase grid voltage (red trace, 50V/div) and injected current (blue trace, 1 A/div, THD= 4.5%) in case of the complete adopted SVM for the CSI7 topology.

Figure 1.24 shows the good dynamic response of CSI7 in case of step variation of the injected grid current, obtained with a step variation of the modulation index m_d. With reference to Fig. 1.12 the test was conducted without the outer MPPT and V_{DC} control loop.

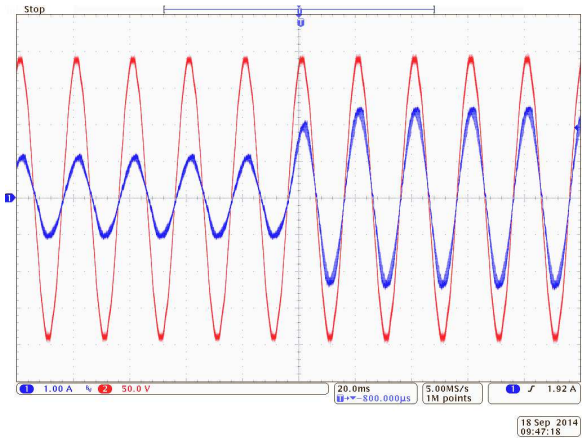


Figure 1.24. Experimental results. Step variation of the injected grid current (blue trace, 1A/div). The figure shows only one phase current and grid voltage.

Figure 1.25 shows the experimental comparison efficiency of the CSI7 solution and traditional CSI. This behavior was expected since in case of a relatively small DC input voltage (see Table 1.3) the time interval in which one leg is short

Table 1.4. Simulations and Experimental THD Comparison

SVM Name	Simulation THD	Experimental THD
CSI 0AB	11.8%	11%
CSI7 0A0B no OV.	8.2%	8.9%
CSI7 0A0B no inv. seq.	25%	11.5%
CSI7 0A0B	4.4%	4.5%

circuited is predominant during every PWM period. The same figure shows also the efficiency of the CSI7 solution with an higher DC input voltage, $V_{DC} = 210V$. Despite the power semiconductor devices were not chosen for efficiency maximization, the overall efficiency results almost acceptable for actual PV systems in this last case.

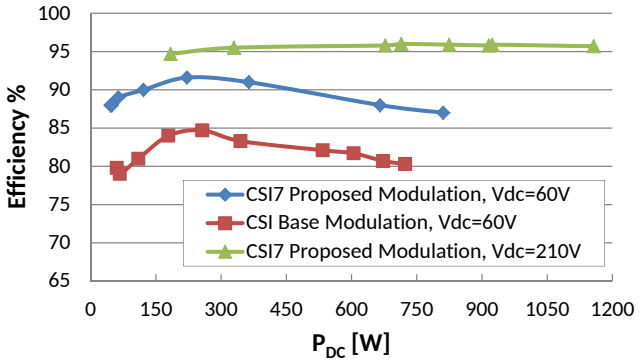


Figure 1.25. Experimental results. Efficiency comparison between CSI7 solution and traditional CSI solution.

1.2.6 Evaluation of PWM strategies

A theoretical analysis of the switching losses was carried out by comparing three different SVM control strategies during one PWM cycle. Only a subset of the SVM control strategies were chosen among the ones available in literature. The present work was focused on the alternated modulation sequence ($0A0B$) because of the benefits on output glitches elimination. Other high efficiency commutation strategies exist, such as ($AB0BA$) that are aimed at

Table 1.5. Comparison among SVM strategies

SVM	Conduction (null state)	Conduction (active state)	Hard Switch Commutations	Comm. ZCS
0AB (Basic CSI)	2 Transistors 2 Diodes	2 Transistors 2 Diodes	3	3
0AB (CSI7)	1 Transistor	2 Transistors 2 Diodes	3 (2xS7)	3
AB0BA (CSI7)	1 Transistor	2 Transistors 2 Diodes	4 (2xS7)	4
0A0B * (CSI7)	1 Transistor	2 Transistors 2 Diodes	4 (4xS7)	4

reducing switching losses (e.g. in [24]). Table 1.5 summarizes a comparison among different SVM strategies: basic CSI topology with basic SVM $0AB$, CSI7 topology with basic SVM $0AB$, CSI7 topology with the proposed SVM $0A0B$ and CSI7 topology with $AB0BA$ SVM. As it can be seen, the introduction of S7 obviously increases the converter efficiency for all the modulation strategies, because of the beneficial effect on the conduction losses during null state.

Referring to Table 1.5 some observations can be made concerning commutation conditions during one PWM cycle. In particular, the presence of the overlap time, combined with the reverse blocking diodes characteristics of the CSI topology ensures certain conditions.

- During a PWM period, when the SVM strategy involves the direct transition between two active vector (-AB- or -BA-), one of the commutation happens under ZCS and the other is hard switching. This happens for all the SVM.
- For the basic CSI architecture (no S7 present) the same applies when transitioning between a null state and an active state (or vice versa).
- For the CSI7 architectures, all the transitions between a null state and an

active state (and vice versa) happen with the reverse blocking switches (S_1-S_6) commutating under ZCS.

As it can be seen from Table 1.5 the switching count is the same for $0A0B$ and $AB0BA$ sequences. With the adopted modulation ($0A0B$), switching losses are all allocated on S7. This can be disadvantageous if all the switches are identical. On the other hand, this can be advantageous to reduce switching losses if a SiC MOSFET is used for S7 (as presented in [25]).

1.3 CSI and CSI7 Topology Comparison

The aim of this chapter is the in-depth analysis of the CSI7 topology and its comparison to the traditional CSI in terms of ground leakage current and semiconductor power losses. The performance comparison is carried out in case of photovoltaic grid-connected systems and in particular with a different number of PV panels connected in series.

1.3.1 Single DC input Inductor or Split DC input Inductors in CSI

Figure 1.26a shows the traditional CSI with the presence of only a DC input inductor while in Figure 1.26b the DC input inductor is split between the positive and negative DC rails. Fig. 1.27 shows the CSI7 topology with same configurations: with and without the split of the DC input inductor.

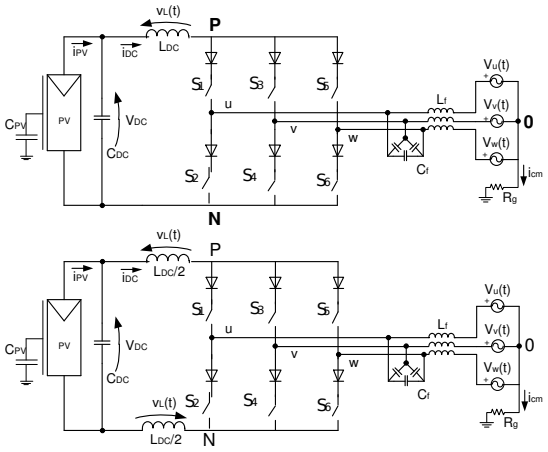


Figure 1.26. Schematic of traditional CSI topology. a) single inductor, b) split inductor

Two different SVM sequences are compared against each other. Classic Base sequence and the Alternated sequence, see section 1.2.2.

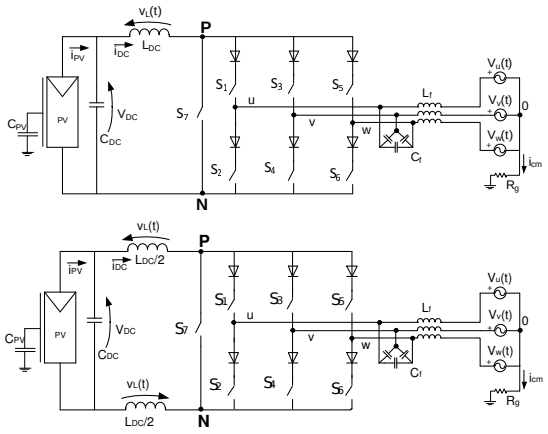


Figure 1.27. Schematic of CSI7 topology. a) single inductor, b) split inductor

In case of Alternated SVM with CSI7 topology the commutations of the six switches S1-S6 occur always in ZCS. In case of base SVM this does not happen for the turn-off of one transistor (S1-S6) during the transition from active current vector A to active current vector B (see Figure 1.10). It is also important to highlight that the amount of ground leakage current i_{cm} is strongly dependent on the common-mode equivalent circuit, which is different in case of CSI or CSI7 topologies because of different application of zero active vector that takes place with the short-circuit of one of the legs for CSI topology and with the turn-on of S7, with all the other switches in OFF-state in case of CSI7 topology.

1.3.2 Consideration on Ground leakage current

The ground leakage current in PV systems as shown in Figure 1.26, is mainly caused by the frame-to-earth parasitic capacitance of the PV panels and the common-mode voltage variation introduced by the power converter operation [26]. For CSI topologies, the common-mode voltage, v_{cm}, will be assessed. According to literature on CSI, [4], [27], the v_{cm} can be computed using the star connection of the three-phase grid voltage as voltage reference, resulting in (1.3.1).

$$v_{cm} = \frac{V_{P0} + V_{N0}}{2} \tag{1.3.1}$$

In case of traditional CSI topologies, it is common practice to split the DC input inductance. Figure 1.28 shows the equivalent common-mode circuit in case of split DC inductance: in case of a single DC input inductor, common-mode inductance on DC side becomes null. The other components present in the common-mode circuit are the ground resistance R_g, the equivalent PV parasitic capacitance C_{PV} and 1/3 of the inductive part of the output filter, i.e. $L_f/3$. The filter capacitors C_f in common-mode path result in a parallel-series connection. In case of inductive and capacitive values used in acutal converters, the impedance of this equivalent capacitor (connected in series with the other bipoles) is strongly lower respect to the impedance of the other inductive components at switching frequency. For this reason the capacitive component can be neglected in the equivalent common mode circuit.

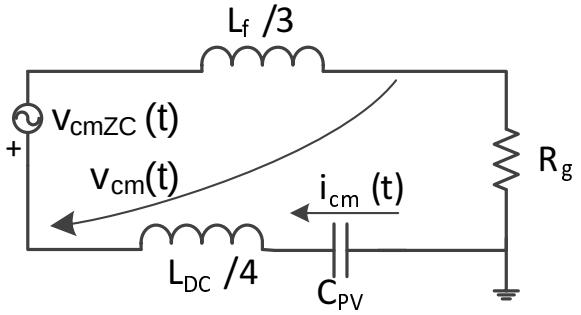


Figure 1.28. Commom-mode circuit in case of traditional topologies with split DC Inductor.

For a CSI topology, the common-mode voltage is not independent from the common-mode current (as it is the case in VSI). If the definition (1.3.1) is adopted, i_{cm} perturbs v_{cm} because it is also flowing through the output filter inductor L_f. The non-uniqueness of the common-mode voltage definition causes problems in the analysis, making it difficult to compare different solu-

tions. For this reason, a novel definition of common-mode voltage is hereby adopted, to make the analysis of the CSI ground leakage current similar to the VSI one. In the following v_{cmZC} identifies the v_{cm} signal with a null common-mode current i_{cm}, i.e. with a zero C_{PV}.

The two topologies CSI and CSI7 differ in the common-mode voltage generation. In case of traditional CSI during the application of the three different null vectors, the instantaneous common-mode voltage assumes the following voltage values: $v_u/2$,$v_v/2$ and $v_w/2$. In case of the CSI7 solution, during the null vector configuration, the instantaneous v_{cm} is 0 if the switches are considered ideal, thanks to the disconnection of the PV panels from the grid at the price of an increased number of commutation per cycle, see Figure 1.29.

The complete decoupling between the grid voltage and the DC input is what allows for the superior performance of the CSI7. Altough the CSI topology is also reported with a single inductor in the DC link, because of the poor performance [28] of this solution, only the split-inductors version is considered in this work.

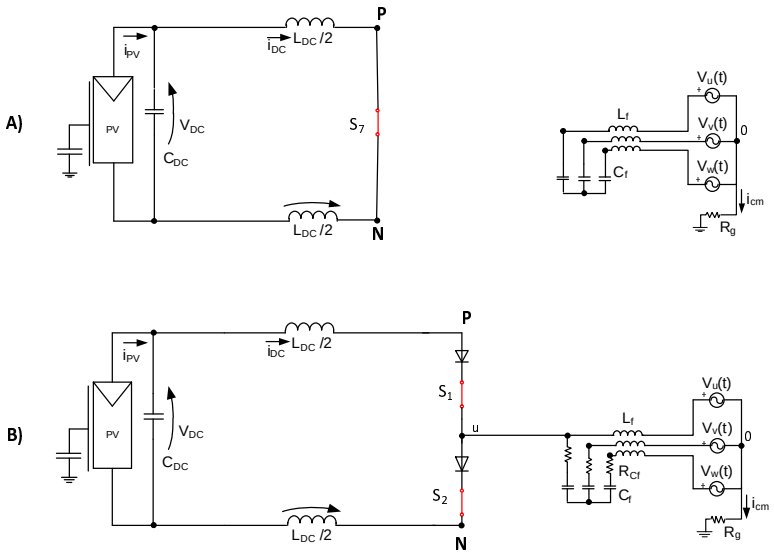


Figure 1.29. Equivalent Circuit under zero Vector: A)CSI7 , B)CSI

The equivalent common-mode circuit in case of classic CSI of Fig. 1.28 presents

1/4 of the total DC input inductance thanks to the split DC inductor. This split is therefore mandatory to reduce the i_{cm}, since with a sole input DC inductor its contribution disappears in the common-mode circuit. Figure 1.30 shows the common-mode circuit of CSI7 topology, where the decoupling between mains and DC Input occurs when the zero vector is applied ($S7$ is switched ON and all the other switches are OFF). For a correct modelling of the common-mode circuit in case of actual switches, an equivalent capacitive value depending on transistor output capacitance has to be considered, see Figure 1.30.

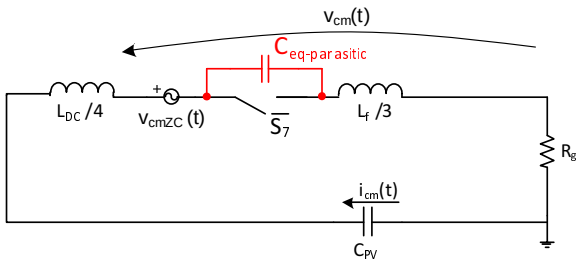


Figure 1.30. Equivalent common mode circuit considering parasitic capacitors in CSI7 topologies.

1.3.3 Numerical simulations

The two topologies and SVMs were simulated in Matlab - PLECS environment using the same application circuit detailed in Fig. 1.31.

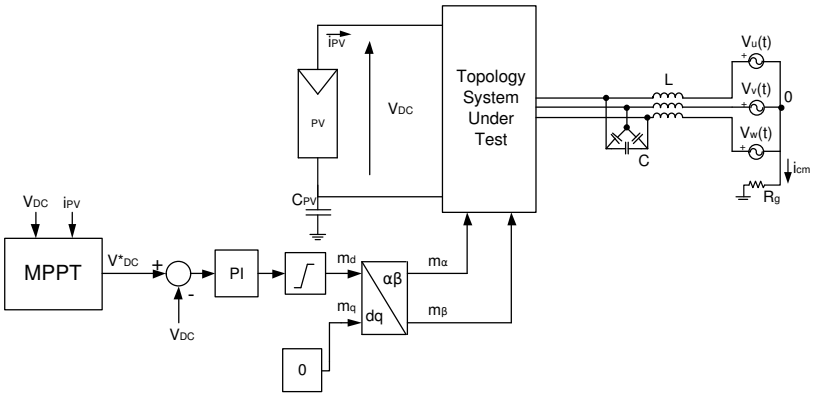


Figure 1.31. Test Bench for the simulation of different solutions.

Table 1.6. Nameplate data of the PV module used in simulations

Name	Value	Unit
V_{mpp}	30.3	V
I_{mpp}	8.24	A
$C_{PV_{single-panel}}$	25	nF

The PV power source is formed by a varying number of PV modules and the AC side is connected to the grid with a capacitive-inductive filter. Table 1.6 summarizes the parameters of the SHARP ND-RC250 PV module: a worst case scenario of 100nF/kWp (as indicated in Technical Information of SMA [29]) was considered for the equivalent parasitic capacitance C_{PV}, resulting in a value of $25nF$ for each module. The simulations were carried out with strings of 2, 4, 6 and 8 PV modules in MPP operation and consequently with different values of equivalent PV parasitic capacitance and PV power source, see Table 1.7, the parasitic components of switches and diodes are neglected. The operating parameters are summarized in Table 1.8.

The classic MPPT and the input voltage control with a PI regulator were adopted. No current control is mandatory, as the injected grid current is directly controlled via the duty cycle, see [21]. For the sake of simplicity the modulation index m_q was imposed equal to zero: doing so, a small reactive power can flow, determined by the CL filter supplied by the grid. The park transformation $dq - \alpha\beta$ obtained with the measure of the angle of grid voltage vector determines the input of SVM.

Table 1.7. Summary of PV Source scenarios

Numbers of PV modules	P_{DC} [W]	V_{mppt} [V]	C_{PV} [nF]
2	500	60.6	50
4	1000	121.2	100
6	1500	181.8	150
8	2000	242.4	200

The performance comparison was carried out with two topologies and two

different SVM modulations:

1. Traditional CSI with Base SVM
2. Traditional CSI with Alternated SVM
3. CSI7 with Base SVM
4. CSI7 with Alternated SVM

In order to perform a fair comparison between Base and Alternated SVMs, the switching period T_s in case of Base SVM is halved with respect to Alternated SVM one, $T_{S-BasePWM} = 33.33\mu s$ and $T_{S-AltPWM} = 66.67\mu s$. Table 1.8 shows all the other parameters.
In this way, the number of hard switching commutations (per unit of time) of the seventh switch S7 results the same along with the ripple at switching frequency of the injected grid current [21, 28]. In the same works it is possible to see that, in case of CSI7 topology with alternated SVM, the other switches commutate in ZCS (Zero Current Switching).
In order to set the resonance frequency of the equivalent common-mode circuit of Fig. 1.28 to be always lower than the minimum switching frequency, i.e. $f_{S-AltPWM} = 15kHz$, a three-phase AC common-mode inductance was added to all solutions simulated. In actual application a common-mode filter is always used also for EMC issues.
Since a smaller C_{PV} values determines an higher resonance frequency, it was considered a minimum value of C_{PV}, often determined by additional filters added in the power converter for EMI problems, equal to 10nF. Considering this value, it was chosen $L_{cm} = 3 \times 20mH$ to obtain a resonance frequency still lower to $f_{S-AltPWM} = 15kHz$. In this scenario the resonance of frequency response $\frac{i_{cm}}{v_{cmZC}}(j\omega)$ results equal to 11kHz, see Fig. 1.32.

Table 1.8. Simulation and Experimental Parameters

Name	Value	Unit
L_{DC}	2	mH
$T_{S-BasePWM}$	33.33	µs
$T_{S-AltPWM}$	66.67	µs
T_{ov}	1	µs
V_{grid} (line-to-line)	400	V_{RMS}
f_{grid}	50	Hz
L_f	1.4	mH
C_f	1.5	µF
R_g	4.7	Ω

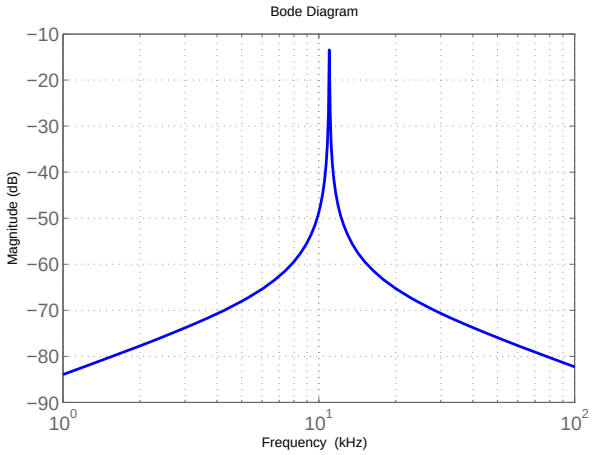


Figure 1.32. Bode Diagram of $\frac{i_{cm}}{v_{cm}}(j\omega)$ in case of $C_{PV} = 10nF$ and $L_{cm} = 3 \times 20mH$.

At first, the performance comparison was carried out with the use of a PV source formed by 4 PV modules. Waveforms of v_{cmZC}, injected phase current, and i_{cm} and their FFT are shown.

In the present work, simulations of the CSI7 topology were carried out assuming the latter condition (negligible parasitic capacitance). In actual applications, this is related to a low value of output capacitance of the power semiconductors. In this case, the main harmonic content of v_{cmZC} is located at $2/T_S$. In the first scenario (not considered in simulations) a lower harmonic content would be present and the main harmonic content would be located at $1/T_S$.

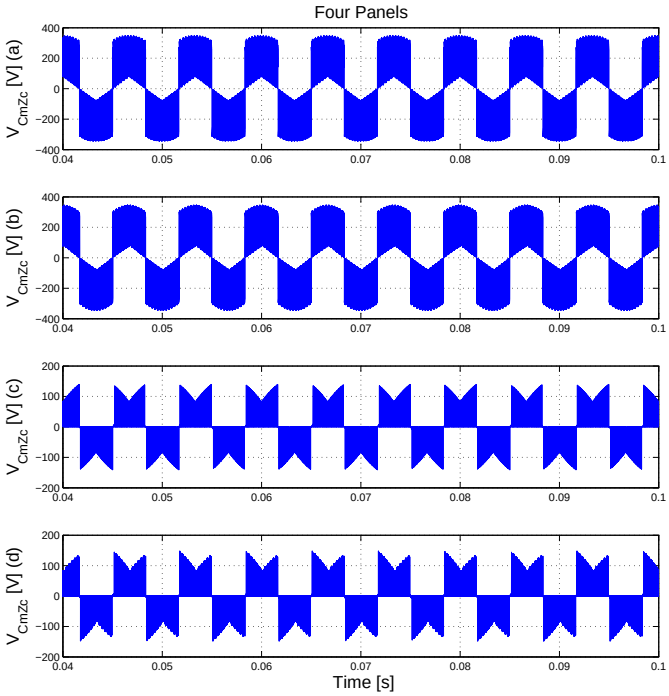


Figure 1.33. Simulation waveforms of v_{cmZC} in the four scenarios with 4 PV modules with null C_{PV}.From the upper trace to the lower trace: traditional CSI with Alternated SVM (a) and Base SVM (b), CSI7 with Alternated SVM (c) and Base SVM (d).

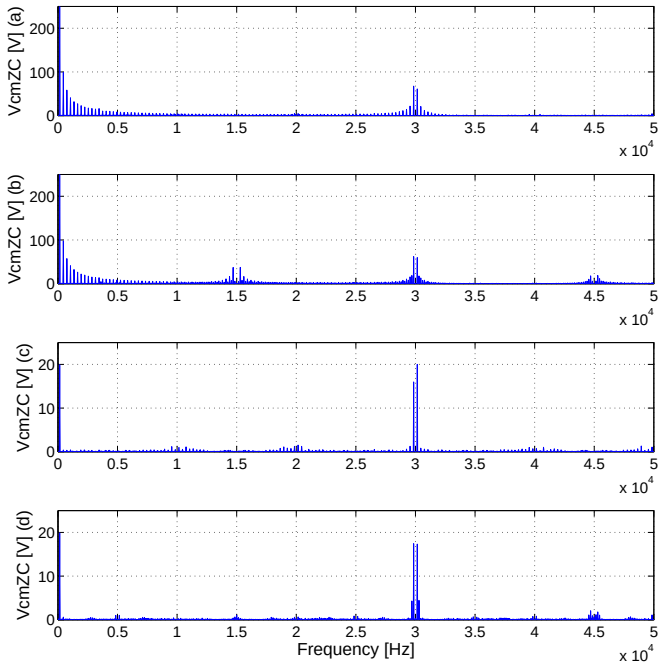


Figure 1.34. Simulation waveforms of FFT in the four scenarios with 4 PV modules with null C_{PV}.From the upper trace to the lower trace: traditional CSI with Alternated SVM (a) and Base SVM (b), CSI7 with Alternated SVM (c) and Base SVM (d).

Figure 1.33 shows the v_{cmZC} waveforms in the four scenarios with null C_{PV} value in case of ideal switches, and whereas Fig. 1.34 shows their spectra. It is possible to see the lower harmonic content of v_{cmZC} in case of CSI7 topology, both with Base and Alternated SVMs. Under the same operating conditions, figure 1.35 shows the injected grid current in the four scenarios. From this figure and Fig. 1.39 it is possible to see as the minimum THD of the injected grid current is present in the case of CSI7 topology with Alternated SVM, see [21].

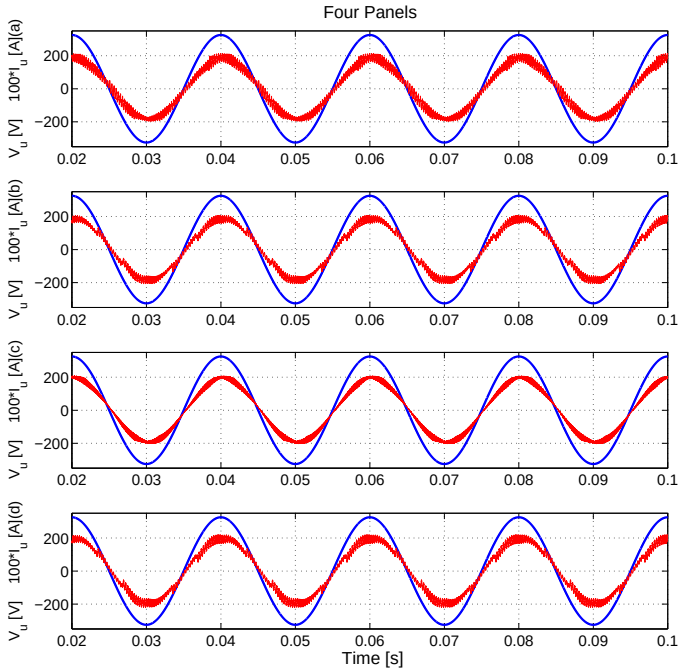


Figure 1.35. Simulation waveforms of Phase voltage and injected grid current in the four scenarios with 4 PV modules with null C_{PV}.From the upper trace to the lower trace: traditional CSI with Alternated SVM (a) and Base SVM (b), CSI7 with Alternated SVM (c) and Base SVM (d).

Figures 1.36 and 1.37 show the effect of C_{PV} in case of four PV modules. It is possible to see a high values of i_{cm} in case of traditional CSI topology, which determines an unacceptable THD for the injected grid current, Figure 1.38.

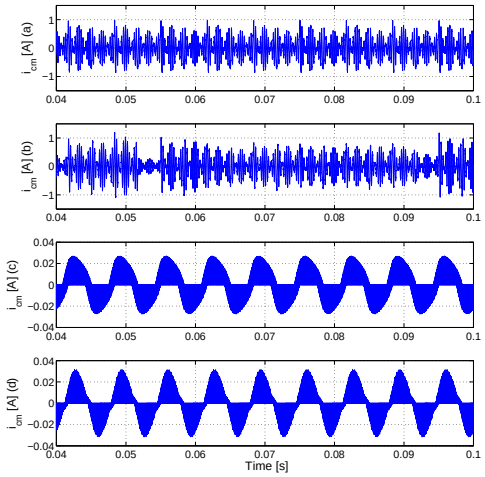


Figure 1.36. Simulation waveforms of i_{cm} in the four scenarios with 4 PV modules with $C_{PV} = 100nF$.From the upper trace to the lower trace: traditional CSI with Alternated SVM (a) and Base SVM (b), CSI7 with Alternated SVM (c) and Base SVM (d).

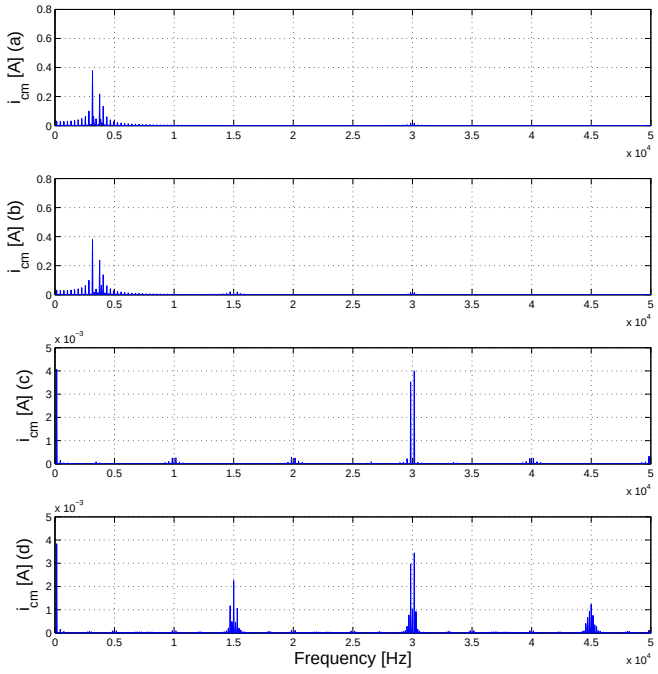


Figure 1.37. Simulation waveforms of FFT in the four scenarios with 4 PV modules with $C_{PV} = 100nF$.From the upper trace to the lower trace: traditional CSI with Alternated SVM (a) and Base SVM (b), CSI7 with Alternated SVM (c) and Base SVM (d).

Figure 1.37 shows the spectra of i_{CM}. As expected in the case of CSI topology, a significant harmonic content is present also at low frequencies in the spectra of v_{cmZC}.

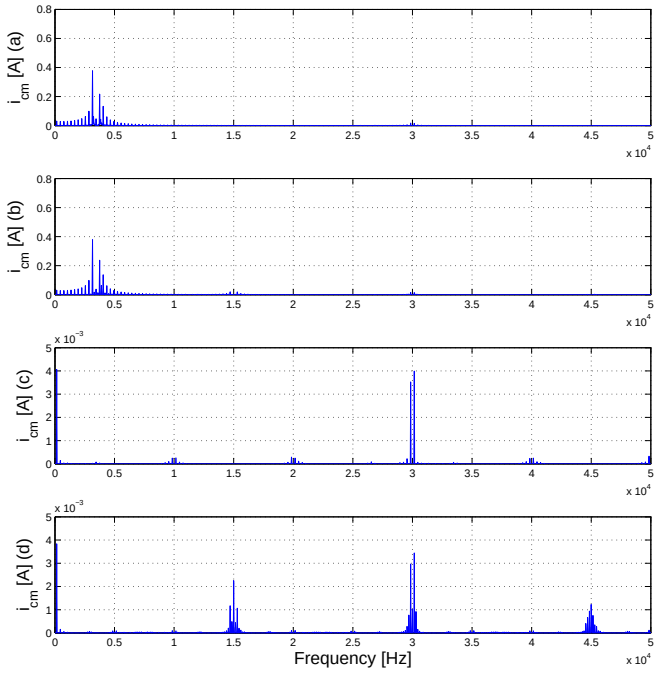


Figure 1.38. Simulation waveforms of Phase voltage and injected grid current in the four scenarios with 4 PV modules with $C_{PV} = 100nF$.From the upper trace to the lower trace: traditional CSI with Alternated SVM (a) and Base SVM (b), CSI7 with Alternated SVM (c) and Base SVM (d).

The histograms of Figures 1.39 and 1.40 show the THD of the injected grid current in the four scenarios with and without C_{PV}, in case of varying number of PV panels. Table 1.9 highlights a negligible increase of the THD due to C_{PV} in case of CSI7 topology with Alternated SVM.

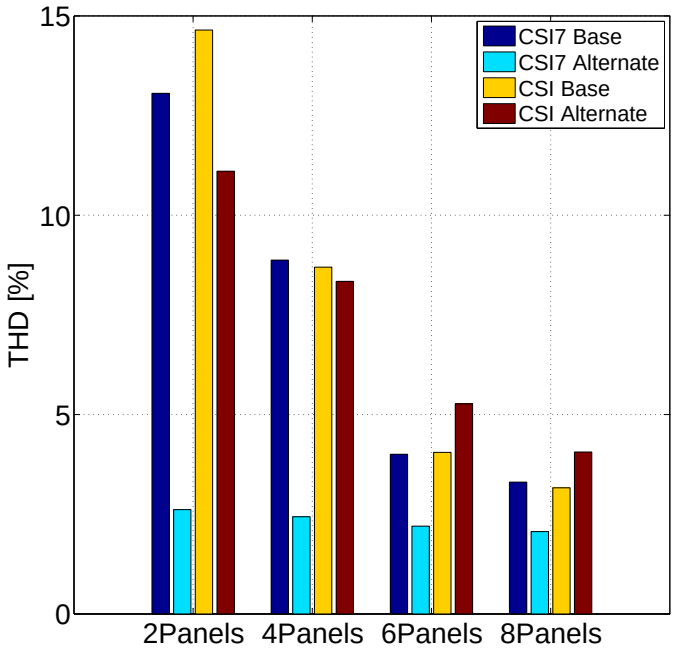


Figure 1.39. THD of the injected grid current with a null C_{PV} in four scenarios and different numbers of PV modules

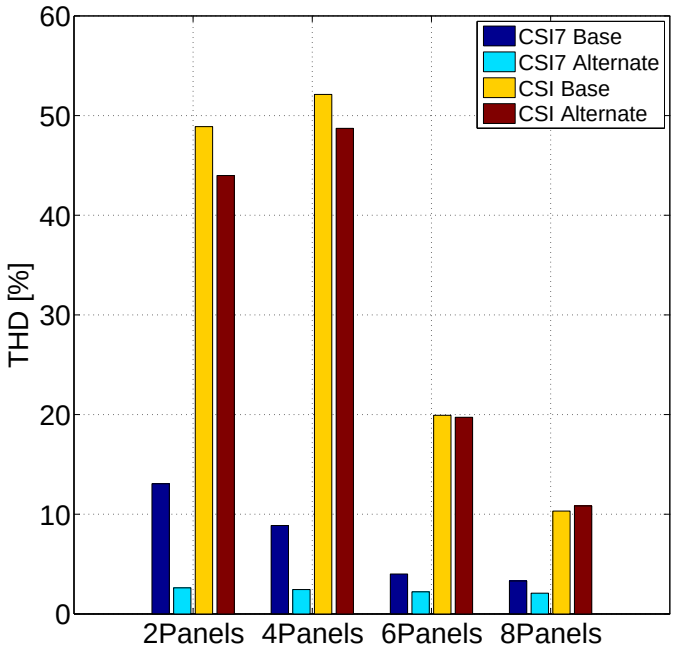


Figure 1.40. *THD* of the injected grid current with C_{PV} in four scenarios and different numbers of PV modules

Figure 1.41 summarizes the evolution of RMS values of i_{cm} in the four scenarios and with a different number of PV modules. Comparing Fig. 1.40 and Fig.1.41 it is possible to appreciate the very low values of i_{cm} also in case of CSI7 topology with Base SVM despite the higher THD of the injected current.

Table 1.9. THD of the injected grid current in case of CSI7 with Alternated SVM

THD [%]	2 Modules	4 Modules	6 Modules	8 Modules
Null C_{PV}	2.6162	2.4367	2.2014	2.0663
With C_{PV}	2.6188	2.4443	2.2186	2.0866

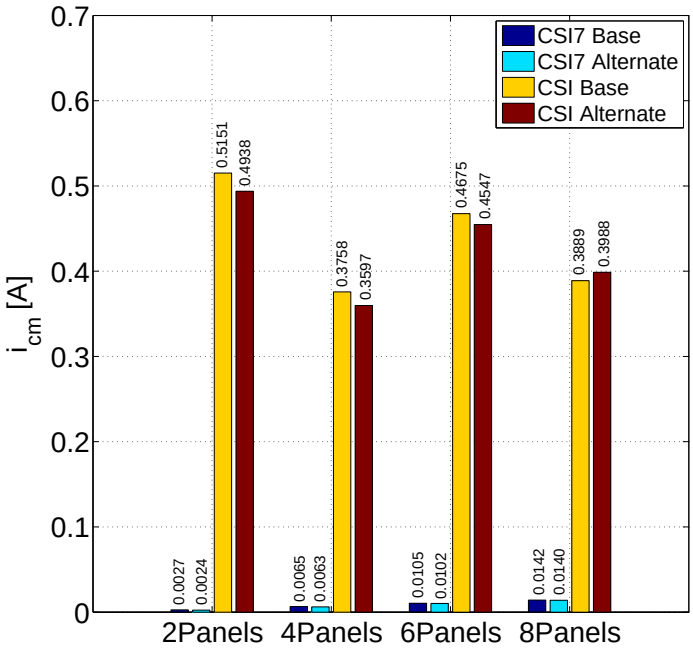


Figure 1.41. RMS value of i_{cm} with different numbers of PV modules, traditional CSI with Alternated SVM (yellow) and Base SVM (red), CSI7 with Alternated SVM (blue) and Base SVM (magenta).

The last set of simulations were carried out in order to compare semiconductor power losses in the four scenarios separating switching and conduction losses for the six switches of the main full-bridge and for the additional S7 switch present in CSI7 topology. This information allows for a proper selection of power switches tailored for the particular topology. The semiconductor power losses were computed with the support of PLECS thermal models. For the sake of simplicity, the same power switches and diodes were chosen for the four scenarios: IGBT 1200V 15A (IGW15N120H3) and diode 1200V 30A

(RHRG30120).

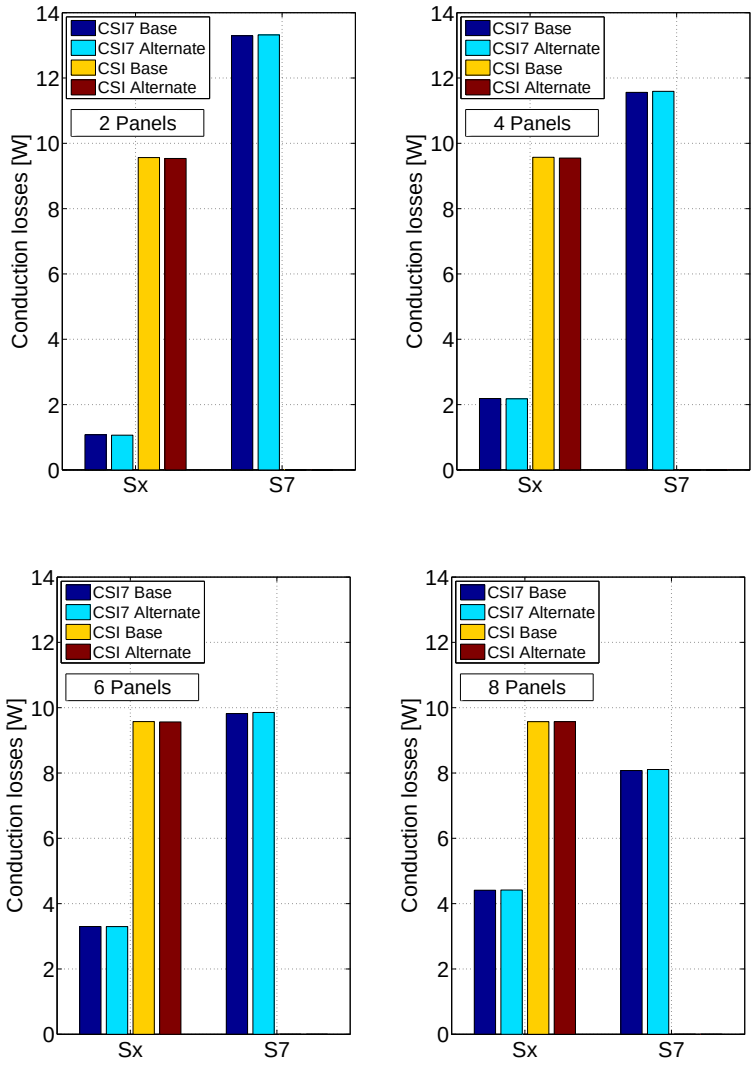


Figure 1.42. Semiconductor conduction losses: S_x represents the losses of a single switch of the main full-bridge.

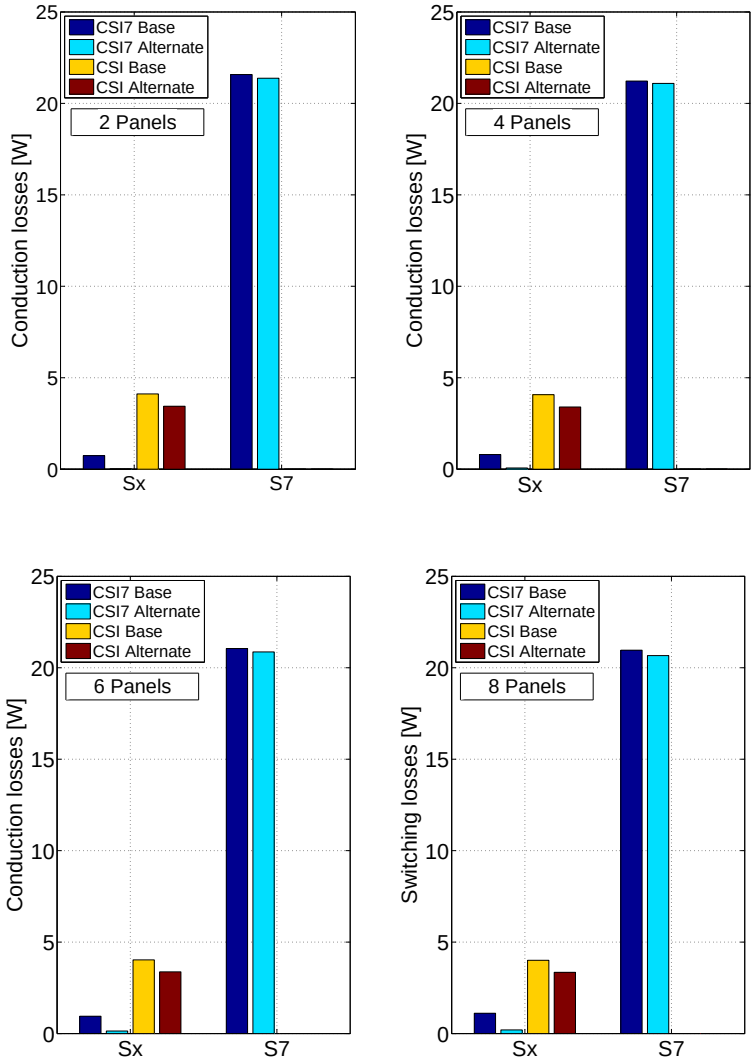


Figure 1.43. Semiconductor switching power losses in the four scenarios and with a different number of PV modules.

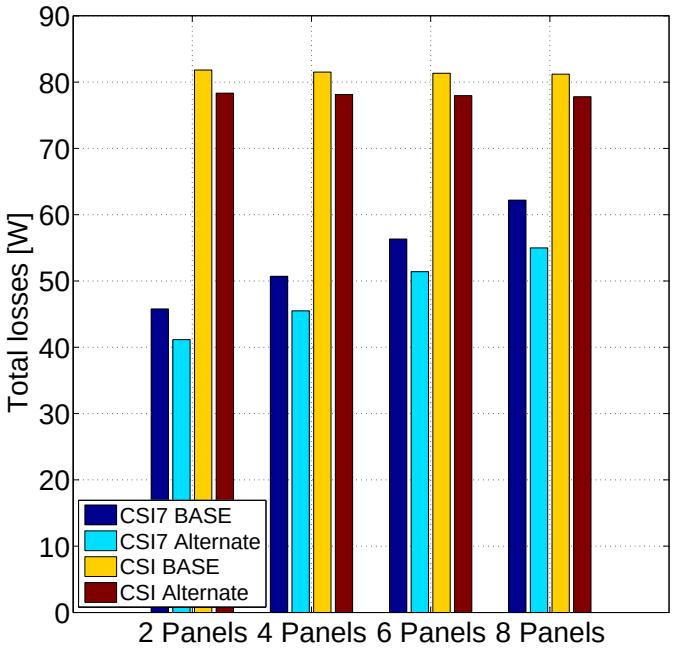


Figure 1.44. Total semiconductor power losses in the four scenarios and with a different number of PV modules.

Figures 1.42 and 1.43 show respectively the evolution of semiconductor conduction and switching power losses for every power switch S_x of the main full-bridge and for the additional S_7, if present. From these figures, it is important to highlight that, in case of CSI7 with Alternated SVM, the switching power losses of every S_x transistor of the main bridge are almost zero thanks to ZCS commutations, and are independent of the number of PV modules. All the switching power losses are concentrated on the seventh switch in CSI7 topology with Altenated SVM: for this reason the use of a Silicon Carbide device for S_7 is advantageous in terms of power losses reduction, see [30] and [31]. Concerning conduction power losses in traditional CSI topology, as expected there is no difference in power losses by varying the number of PV modules in the input string. In case of CSI7 topology there is a decrease of losses on S_7 when the number of PV modules increases: however the concurrent losses

increase on S_x devices reduces the impact of S_7 on conduction power losses reduction.

Figure 1.44 compares the total semiconductor power losses in the four scenarios with different number of PV modules. Even employing the same Si devices for all the transistors, the total power losses are nonetheless lower in the case of CSI7 topology with Alternated SVM due to the application of the zero vector with the seventh switch, allowing ZCS for the other S_x transistors.

1.3.4 Experimental Validation

The experimental validation was carried out with the prototype power converter shown in Fig. 1.19, according to the operating parameters summarized in Table 1.8. Input DC voltage was set equal to $V_{DC} = 120V$ with a $C_{PV} = 100nF$ corresponding to the presence of 4 PV modules. Instead of grid tied operation, the experiments were carried out in island operation, with the use of a balanced resistive load (3 x $R_L = 252\Omega$). For this reason the phase injected grid current results equal to $0.91A_{RMS}$ in order to obtain a three-phase output voltage equal to V_{grid} (line-to-line)= $400V_{RMS}$. The additional common-mode inductor L_{CM} was not added.

Only the two most significant scenarios were experimentally evaluated: traditional CSI topology with Base SVM and CSI7 topology with Alternated SVM. The goal of the experimental validation is related to the ground leakage analysis between these two solutions.Because of this reason, the THD of the injected grid current is not evaluated, as the difference between the grid impedance and the resistor load would make the comparison not representative of the actual condition.

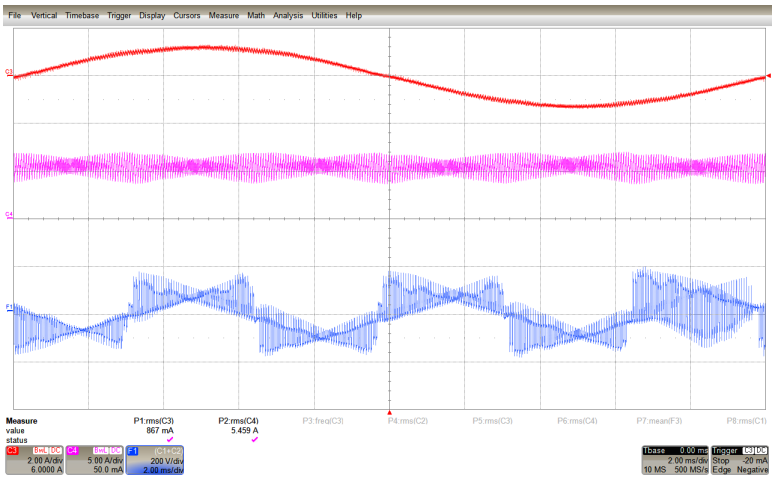


Figure 1.45. CSI7 topology with Alternated SVM with a null C_{pv}, Time/div: 2ms. I_{phase} (2A/div, upper red trace), $I_{Ldc/2}$ (5A/div middle pink trace) and V_{cmZC} (200V/div, lower blue trace).

Figures 1.47 and 1.48 show the injected grid current, V_{cmZC} and its spectrum with a null C_{PV} in case of CSI with Base SVM. Figures 1.45 and 1.46 the same quantities in case of CSI7 with Alternated SVM.

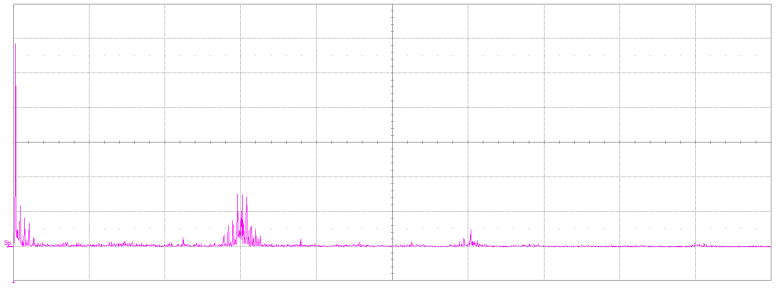


Figure 1.46. CSI7 topology with Alternated SVM with a null C_{pv}. Spectrum of V_{cmZC}, horizontal 5kHz/div, vertical 10V/div.

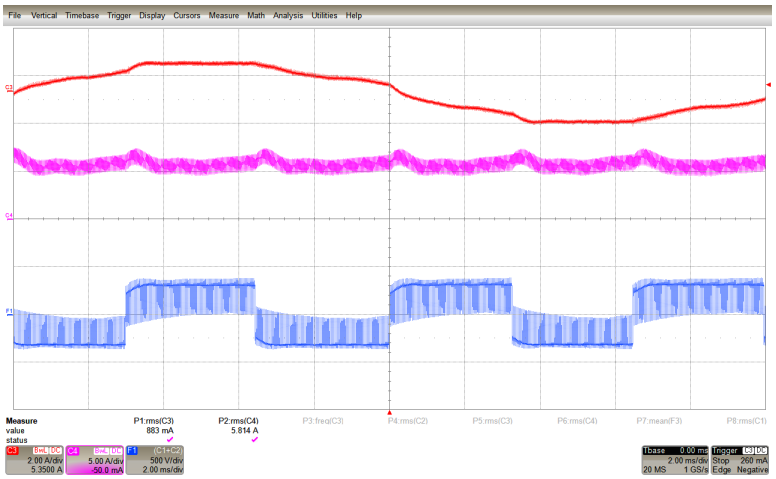


Figure 1.47. CSI topology with Base SVM with a null C_{pv}, Time/div: 2ms. I_{phase} (2A/div, upper red trace), $I_{Ldc/2}$ (5A/div middle pink trace) and V_{cmZC} (500V/div, lower blue trace).

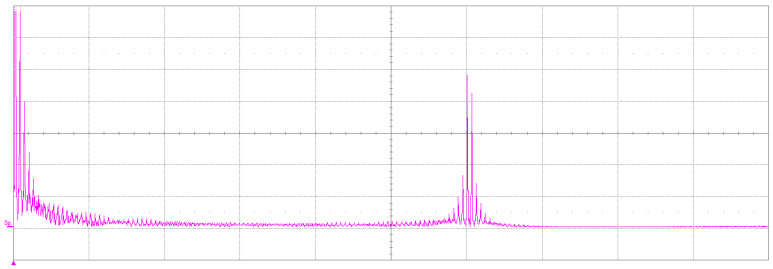


Figure 1.48. CSI topology with Base SVM with a null C_{pv}. Spectrum of V_{cmZC}, horizontal 5kHz/div, vertical 10V/div.

For CSI7 topology with Alternated SVM, when comparing these figures against simulation results, the main difference is the harmonic content of V_{cmZC}. As explained in the following section 1.4.1, because of output capacitance of the power devices employed in the prototype the v_{cmZC} value during the application of the zero vector remain similar to the last voltage value imposed by the previous active vector. As a result the first switching harmonics encountered are not grouped around 30kHz (switching frequency of the S_7) but around 15kHz. Figure 1.49 shows a magnified view of v_{cmZC} during a T_S, demonstrating the effect described.

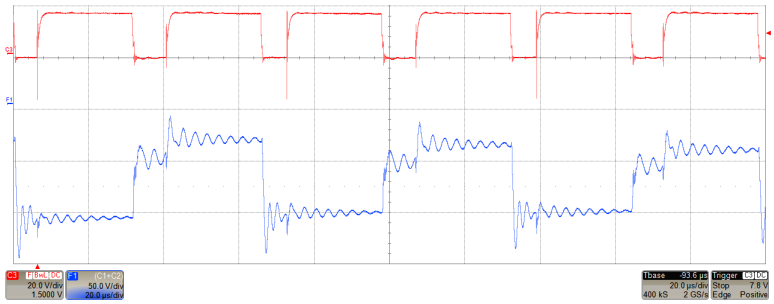


Figure 1.49. Enlarged view of v_{cmZC} waveform during a T_S

Figures 1.50 and 1.51 show the injected phase current, the i_{cm} waveform and its spectrum in case of CSI topology with Base SVM . Figures 1.52 and 1.53 show the same quantities in case of CSI7 topology with Alternated SVM. The RMS of i_{cm} resulted equal to 22.53mA in case of CSI7 topology with Alternated SVM while in case of CSI topology with base SVM resulted equal to 251mA. Looking at Fig. 1.50 it is possible to notice that the i_{cm} waveform is distorting the injected phase current.

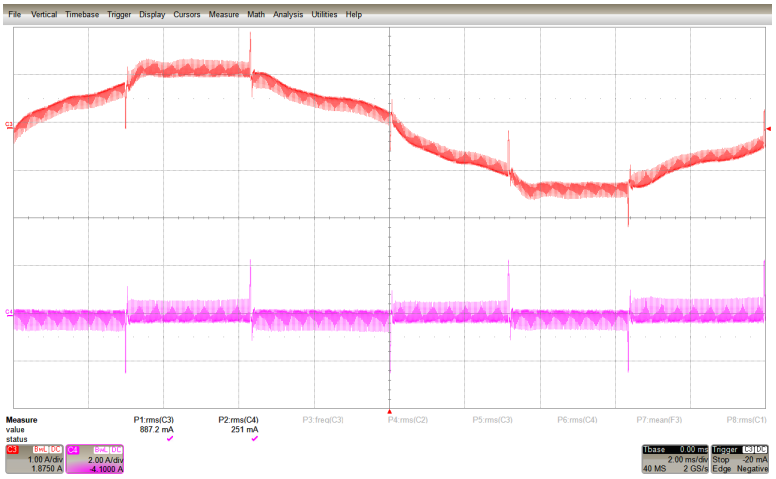


Figure 1.50. CSI topology with Base SVM, injected phase current (upper trace, 1A/div) and i_{cm} (lower trace, 100mA/div).

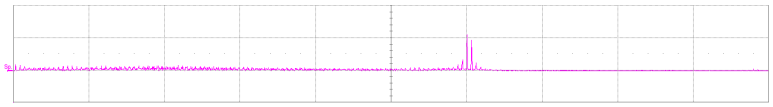


Figure 1.51. CSI topology with Base SVM. Spectrum of i_{cm}, horizontal 5kHz/div, vertical 100mA/div.

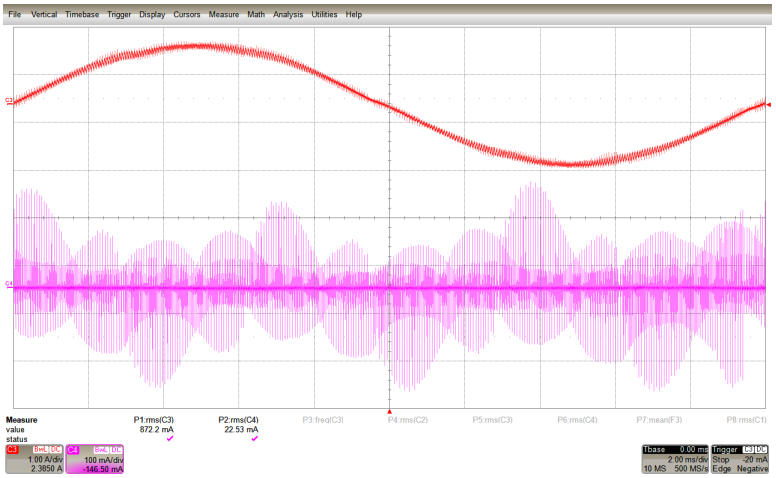


Figure 1.52. CSI7 topology with Alternated SVM, injected phase current (upper trace, 1A/div) and i_{cm} (lower trace, 1mA/div).

Figure 1.53. CSI7 topology with Alternated SVM. Spectrum of i_{cm}, horizontal 5kHz/div, vertical 1mA/div.

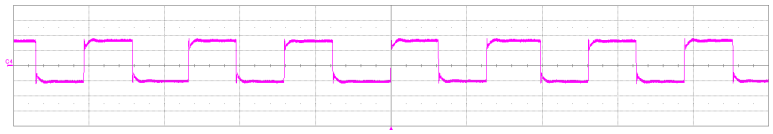


Figure 1.54. $v_{C_{PV}}$ waveform in case of CSI and Base SVM, vertical 200V/div, horizontal 5ms/div.

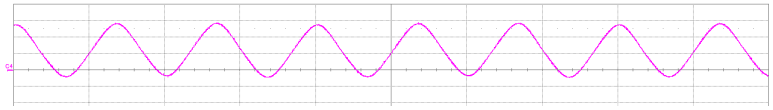


Figure 1.55. $v_{C_{PV}}$ waveform in case of CSI7 with Alternated SVM, vertical 50V/div, horizontal 5ms/div.

Table 1.10. Experimental parameters.

Name	Description	Value	Units
V_{DC}	DC voltage source	60	V
V_g	rms line-to line grid voltage	230	V
f_g	grid frequency	50	Hz
f_s	switching frequency	10	kHz
t_{ov}	overlap time	2	μs
L_{DC}	input inductance	2	mH
L	AC Filter inductance	1.4	mH
C	AC Filter capacitance	1	μF
R_g	ground resistance	4.7	Ω

Figures 1.54 and 1.55 show the voltage waveform (v_{Cpv}) across the equivalent parasitic capacitance C_{PV} in the two topologies. The results confirm the higher harmonic content of v_{Cpv} in case of traditional CSI + Base SVM that determined higher i_{CM} RMS and harmonic content.

1.3.5 Grid-Connected operation

A second set of experiments was aimed at evaluating the ground leakage current, by comparing the CSI7 solution against the traditional CSI topology in grid-connected operation. Table 1.10 summarizes the conditions of the experimental tests and Table 1.11 shows the two different values of the equivalent parasitic capacitance C_{PV} used in case of CSI and CSI7.

Table 1.11. Equivalent PV parasitic capacitance values for CSI and CSI7 solution in case of grid-connected operation.

C_{PV} value	Description
$220nF$	used for CSI7 solution
$22nF$	used for traditional CSI solution

Figure 1.56 shows the ground leakage current and ground voltage across a $220nF$ equivalent PV parasitic capacitance in case of the CSI7 solution. Un-

der these operating conditions the resulting rms value of the ground leakage current is about $26mA$. Figure 1.57 shows the ground leakage current and ground voltage across a $22nF$ equivalent PV parasitic capacitance in case of traditional CSI solution. As it can be seen, even by reducing the parasitic equivalent capacitance by an order of magnitude the resulting rms value of the ground leakage current exceeds $150mA$. In order to avoid damage to the converter prototype due to very high ground leakage current values, it was not possible to conduct this experiment with the same $220nF$ equivalent PV parasitic capacitance.

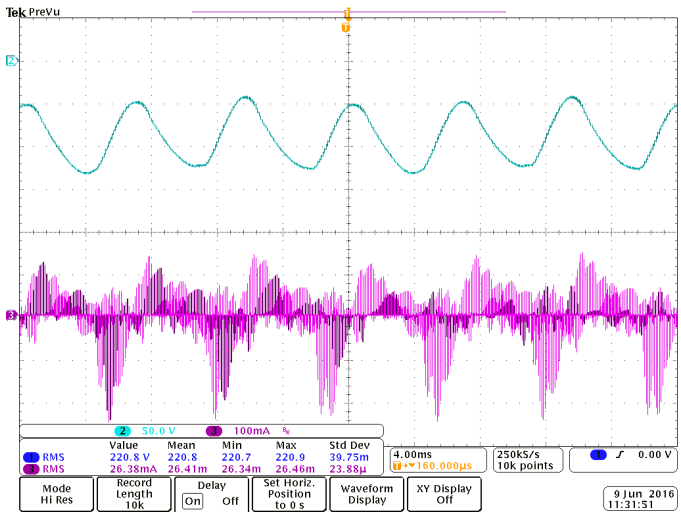


Figure 1.56. Experimental results. Ground voltage (50V/div) and ground leakage current (100mA/div) in case of CSI7 solution.

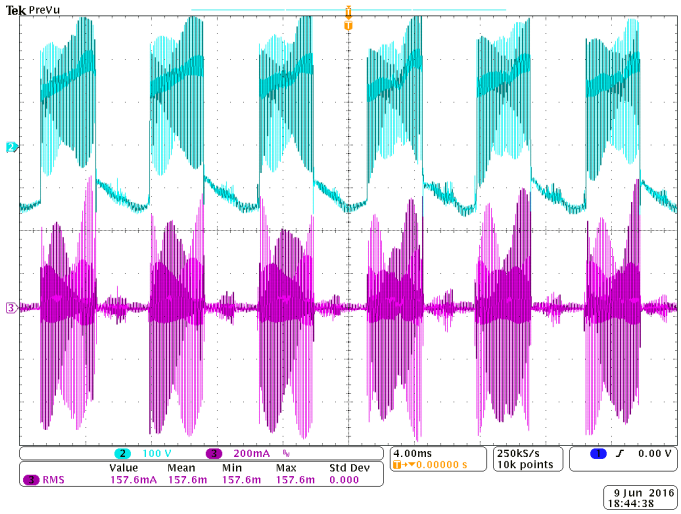


Figure 1.57. Experimental results. Ground voltage (100V/div) and ground leakage current (200mA/div) in case of base SVM for traditional CSI topology.

1.4 Output transistor capacitance C_{oss} and PCB parasitic capacitances effects on ground leakage current issue

In case of CSI7 topology with Alternated SVM, when the zero vector is applied, devices $S1 - S6$ are in off-state. As a consequence, there is no connection between the DC input and the grid as shown in Figure 1.29. Considering real power semiconductors, parasitic capacitances are associated with output transistor capacitance C_{oss}, diode junction capacitance C_j and PCB stray capacitance. Figure 1.58 shows the presence of these additional parasitic capacitances. The value of v_{cmZC} during null vector is affected by the aforementioned capacitances and the instantaneous values of grid voltage.

During the application of this null vector, an equivalent parasitic capacitance, named $C_{eq-parasitic}$, can be computed for the series-parallel connection of these parasitic capacitances, as shown in Figure 1.59.

Figure 1.59 describes the two extreme cases of v_{cmZC} values during the zero

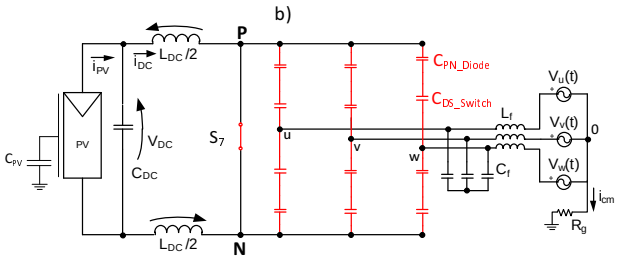


Figure 1.58. Equivalent Circuit under zero Vector of CSI7 with parasitic capacitors.

vector application, i.e. during $t_Z/2$. The two extreme cases are:

- v_{cmZC} remains unchanged to the previous instantaneous value during the application of an active vector.
- v_{cmZC} reaches zero value (in case of negligible parasitic capacitance).

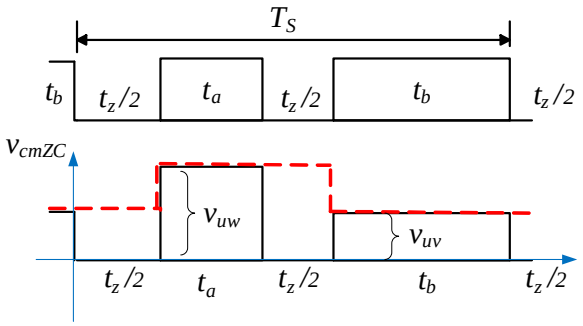


Figure 1.59. Different v_{cmZC} transients in CSI7 topology with Alternated SVM during zero active vector times t_Z.

1.4.1 Numerical Simulation

The CSI7 behaviour with different values of parasitic capacitances is analysed in Matlab-PLECS environment. The simulation parameters are summarized in Table 1.12.

Table 1.12. Simulation Parameters

Name	Value	Unit
L_{DC}	2	mH
T_{PWM}	40	µs
T_{ov}	1	µs
V_{grid} (line-to-line)	400	V_{RMS}
f_{grid}	50	Hz
L_f	1.4	mH
C_f	1.5	µF
R_g	4.7	Ω
C_{PV}	150	nF

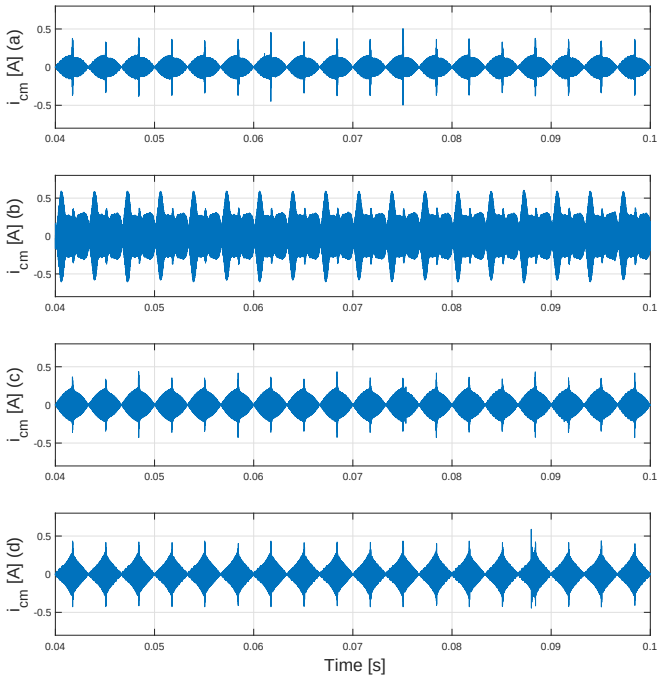


Figure 1.60. Simulation waveforms of i_{cm} in the four scenarios with different values of $C_{eq-parasitic}$.From the upper trace to the lower trace: $C_{eq-parasitic} = 220pF$ (a) $C_{eq-parasitic} = 440pF$(b), $C_{eq-parasitic} = 660pF$ (c) $C_{eq-parasitic} = 880pF$ (d).

Figure 1.60 shows four traces of the i_{cm} with different equivalent parasitic capacitances, $C_{eq-parasitic}$ while Figure 1.61 shows the FFTs of these signals. It

is possible to see that the worst case scenario happens in case of $C_{eq-parasitic} = 440pF$. This is due the variation of the resonance frequency of the common-mode circuit. In case of $C_{eq-parasitic} = 440pF$ the resonance of frequency response $\frac{i_{cm}}{v_{cmZC}}(j\omega)$ results equal to $100kHz$, as shown in bode diagram of Figure 1.62. That matches exactly the $4th$ switching frequency harmonic determining high i_{cm} values. For this reason attention must be given to the resonance of frequency response of the equivalent common- mode circuit.

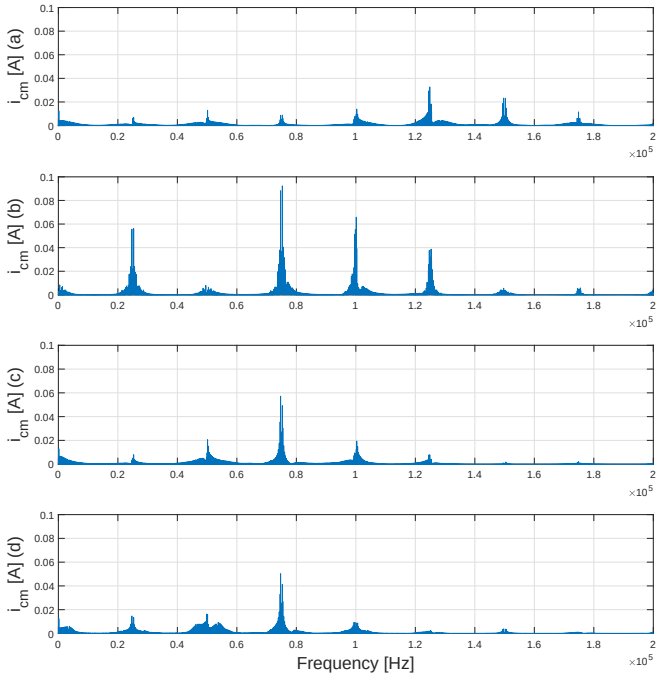


Figure 1.61. Simulation waveforms of FFT in the four scenarios with different values of $C_{eq-parasitic}$.From the upper trace to the lower trace: $C_{eq-parasitic} = 220pF$ (a) $C_{eq-parasitic} = 440pF$(b), $C_{eq-parasitic} = 660pF$ (c) $C_{eq-parasitic} = 880pF$ (d).

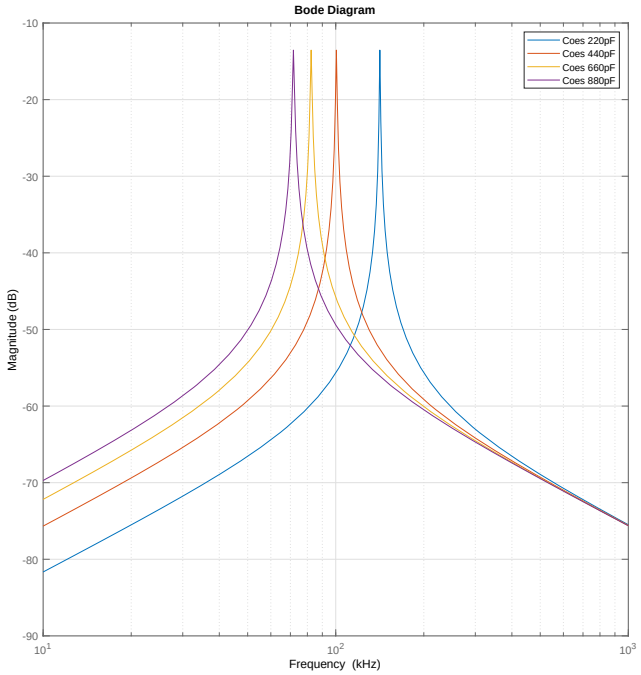


Figure 1.62. Bode Diagram of $\frac{i_{cm}}{v_{cm}}(j\omega)$ in the four scenarios with different value of $C_{eq-parasitic}$.

1.5 CSI7 Topology with common-mode return path

This chapter analyses in detail the effect of a simple solution for ground leakage current mitigation applicable to transformerless three-phase Current Source Inverter, but in particular to the modified topology CSI7. In the present work the solution is applied to grid-connected converters for string photovoltaic applications: scope of the circuit modification is to provide an internal return path from the wye-connected capacitors of the output CL filter. This additional return path is able to significantly reduce the ground leakage current without adversely affect output injected current THD.

Figure 1.63 shows the modified topology applied to CSI7 converter. The novelty of the proposed approach relies in the use of two additional capacitors in the DC link whose mid-point is connected to the wye-connected capacitors of the output CL filter. The internal return path does not lose its effectiveness even when employing only one additional capacitor (of doubled capacitance) connected between the wye connection of the CL filter and the positive or negative terminal of the DC Source. This creates an internal return path with lower impedance that prevents the ground leakage current from flowing into the grid.

A similar approach has been attempted for a single-phase VSI converter in [10]. Advantages and disadvantages of this kind of approach will be analyzed in this section.

In order to carry out the analysis, a new definition of common mode voltage will be used: V_{cmZC} is the common mode voltage at zero ground leakage current condition. This modification is necessary, because, differently from the case of

VSI, the common-mode voltage of the CSI depends on the actual current.
Objective of the following sub-sections is to provide a guide to the design of C_{mid} so that an acceptable ground leakage current reduction as well as the minimization of the circulating current i_{rp} can be achieved.

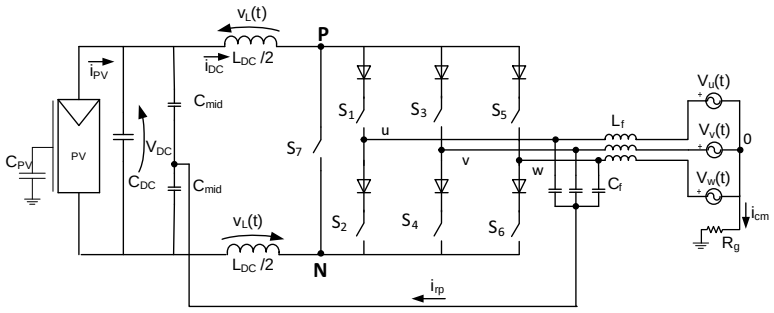


Figure 1.63. Schematic of CSI7 topology with integrated i_{CM} return path.

As reported in the scientific literature, the high frequency content of the common-mode voltage determines a ground leakage current to flow through the parasitic capacitance of the PV panels [26]
According to literature, in CSI the v_{cm} can be calculated by using the wye-connected point of the three-phase grid voltage as voltage reference, [4], [27], resulting in eq.(1.3.1).
As anticipated and shown in eq. (1.3.1), v_{cm} depends on the value of i_{cm}. For this reason, the quantity v_{cmZC}, that dentifies the v_{cm} signal with zero i_{cm}), will be used for the analysis.

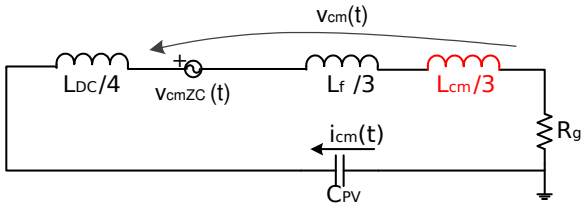


Figure 1.64. Common mode circuit of the CSI.

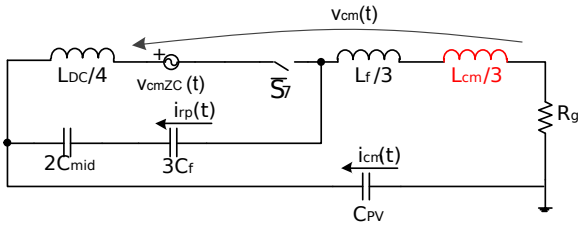


Figure 1.65. Common mode circuit of CSI with integrated i_{CM} return path.

The common mode circuit of a grid-connected CSI converter is shown in Figure 1.64. The inductor L_{CM} is a three-phase common-mode choke that is often adopted for electromagnetic interference (EMI) mitigation in off-the-shelf power converters. Because the common-mode inductor is connected in series with the parasitic capacitance, an appropriate choice of the this component must be operated, so that the switching harmonics are at higher frequencies. Having the resonance at lower frequency also allows for an improvement of the power quality, as the common-mode circuit could act as a second order filter for the common-mode voltage harmonics.

In Figure 1.65 the common-mode circuit of the CSI7 with integrated return path is depicted. As can be seen, a switch models the decoupling of the mains and the DC input when the zero vector is applied. As it appears evident from the circuit, the return path is more effective if the impedance $2C_{mid}$ and $3C_f$ is lower than the path composed of the inductors and the parasitic capacitance. In fact, the two branches act as a current divider for the i_{cm}.

Although the integrated return path could be applied to any CSI-based topology, it will be shown in the next section that the magnitude of the current flowing through this additional branch could be too high in case of traditional CSI.

1.5.1 Classic CSI vs CSI7 Behavior

Figure 1.66 shows the switches sequence for the first sextant in case of CSI topology with Alternated modulation. In case of traditional CSI topology, the zero state is applied by turning on the switches S_1 and S_2, as shown in Fig.1.66-1. When taking into consideration the additional return path in case of traditional CSI topology, the circuit during the zero state becomes the one shown in Fig.1.68. In this figure it is possible to see that there is a circuit formed by only one of the capacitors C_{mid} and DC input inductors $L_{DC}/2$ (due to the presence of the two diodes) and the output CL filter connected as in Fig. 1.68 together with the grid phase voltages. Since before the application of the zero vector the voltages across the capacitors C_f are very close to the grid phase voltages, and the voltage across every C_{mid} is equal to $V_{DC}/2$ a large current can flow in the resulting multi-resonant circuit.

Figure 1.67 summarizes the switches sequence for the first sextant in case of CSI7 topology with Alternated modulation. In case of CSI7 topology, the zero state is applied by turning on the additional seventh switch S_7 with all the other switches off, as shown in Fig.1.67. When introducing the additional return path, the circuit becomes the one depicted in Fig.1.69. The CSI7 topology allows to use to use advantageously the return path because during the zero state the voltages on filter capacitors don't change significantly thanks to the disconnection of the main full-bridge outputs from C_f capacitors.

Summarizing the issues of the application of the return path, the proposed solution is only viable in case of CSI7 topologies with split DC input inductors, as the split DC input inductors limit the value of i_{RP}, as it can be seen by analyzing the common-mode circuit of Fig. 1.65. In fact, in case of a single input inductor the equivalent impedance related to L_{DC} disappears.

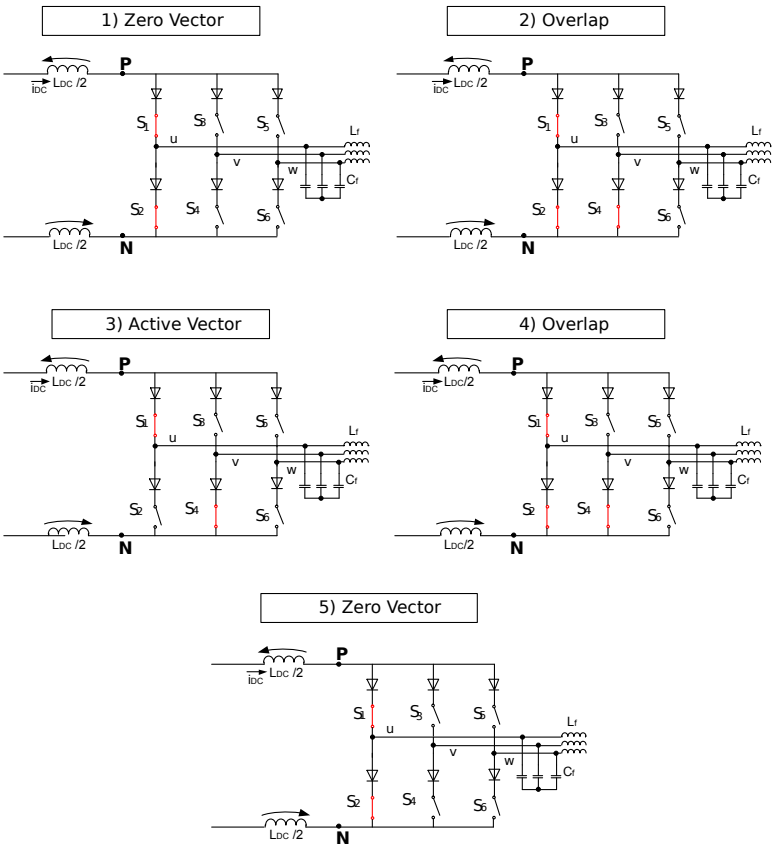


Figure 1.66. Switch configuration of Classic CSI during Alternated modulation (sequence covers one half period): (1) zero vector; (2) overlap time; (3) active vector; (4) overlap time; (5) zero vector.

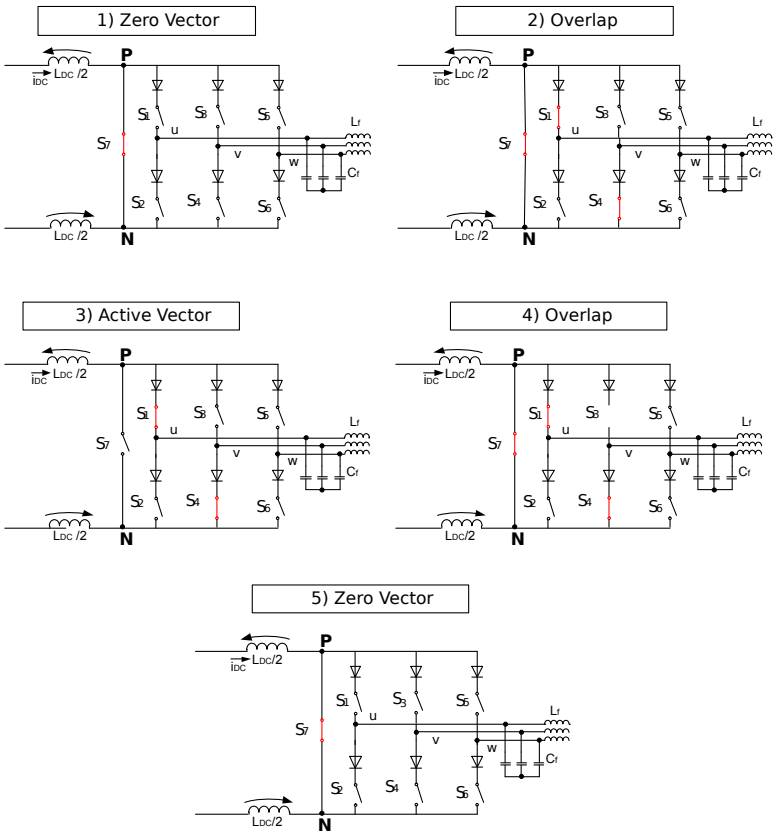


Figure 1.67. Switch configuration of CSI7 during Alternated modulation (sequence covers one half period): (1) zero vector; (2) overlap time; (3) active vector; (4) overlap time; (5) zero vector.

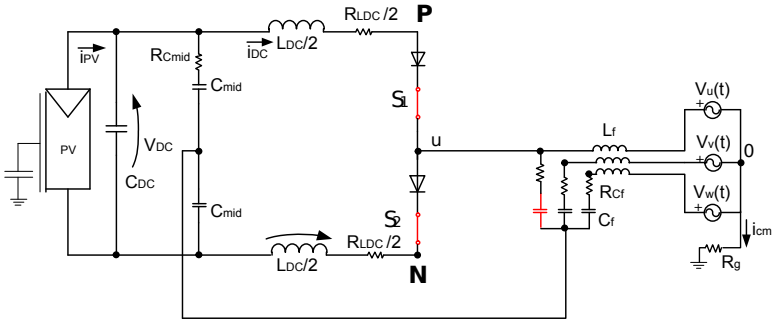


Figure 1.68. Zero state simplified circuit in case of CSI Topology with integrated i_{CM} return path

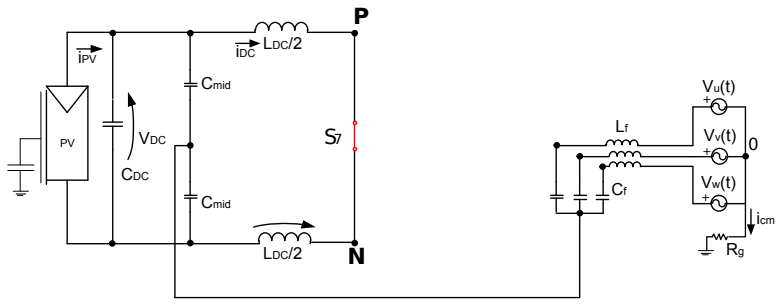


Figure 1.69. Zero state simplified circuit in case of CSI7 Topology with integrated i_{CM} return path

1.5.2 Considerations on DC split capacitance values

The design of the split capacitance must achieve the two objectives:

- minimization of the split capacitance to reduce the cost and weight of the converter
- reduction of the ground leakage current i_{cm}
- minimization of the current in the return path i_{RP}

These requirements translate into the need of a considerably low impedance of the overall return path at the harmonic frequencies of v_{cmZC}. It is important to highlight that the output filter $3C_f$ is connected in series to the return path, so increasing the value of the split capacitance much above the output filter ones would lead to no additional current reduction.

The common mode impedance $i_{cm}/v_{cmZC}(j\omega)$ of the circuit of Fig. 1.65 is evaluated. The parameters are listed in TABLE 1.13 and 1.14 and the results are shown in Fig. 1.70.

The same parameters will be used in Section 1.5.3 for the numerical simulations. As can be seen from the graph of Fig. 1.70, values in the range of uF for the return path capacitor allows for a marked attenuation, whereas increasing C_{mid} above 7 uF, there is no significant benefits. If $C_{mid} = 0$, it means that the CSI converter does not have a return path.

The resulting ground leakage current depends not only on the value of the common mode impedance, but also on the value of the common mode voltage v_{cmZC}. For this reason, the harmonic component is evaluated in Figs 1.71 and 1.72. The main switching harmonics are located at twice the switching frequency $2f_s = 50kHz$ whereas the harmonics introduced by the space vector modulation are at $3f_{grid}$.

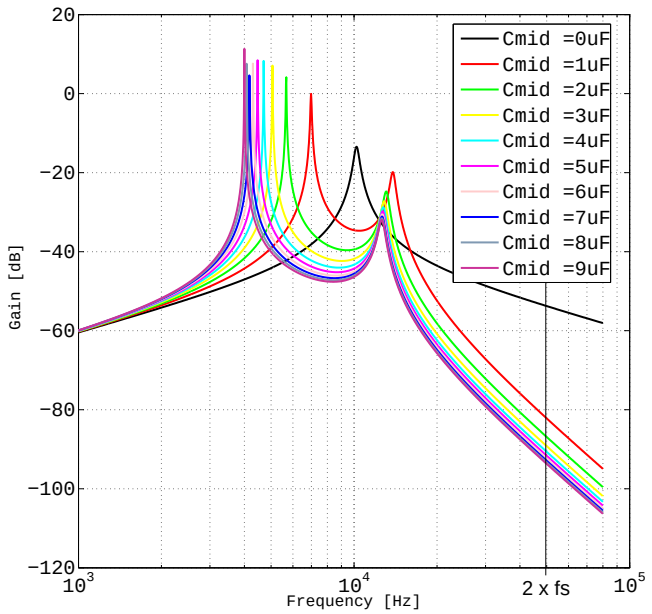


Figure 1.70. Bode Plot of $i_{cm}/v_{cmZC}(j\omega)$ of the CSI7 with integrated return path and 8 panels.

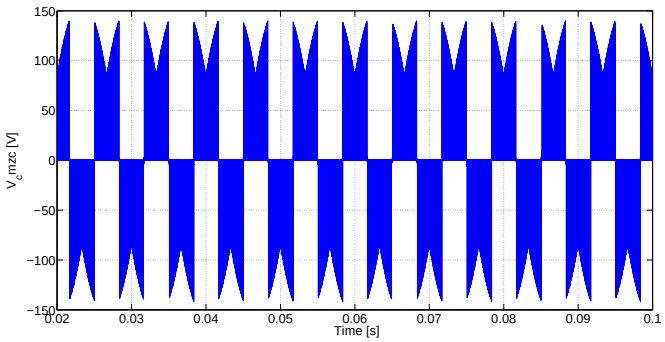


Figure 1.71. v_{cmZC} with 8 PV modules

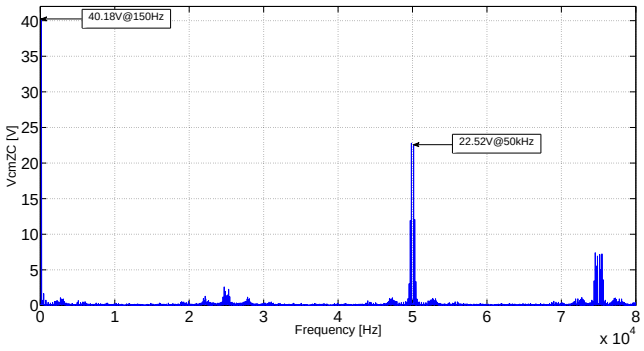


Figure 1.72. FFT of v_{cmZC} with 8 PV modules

As anticipated, the selection of the return path capacitor C_{mid} must also comply with a limitation of the return path current. The value $7uF$ represents the optimum of the capacitance size and leakage current minimization, but a lower value could be chosen to limit the magnitude of the return path current i_{RP}.

1.5.3 Numerical simulations

All the numerical simulations were carried out in Matlab - PLECS environment considering a string PV source composed by a varying number of PV modules, working under MPP condition. The same parameters of TABLE 1.14 are used, considering 150nF/kWp as the worst case scenario, that translates into $37.5nF$ for each module.

Two sets of simulations were carried out separately, in order to assess the internal return path solution feasibility in case of different CSI topologies operated with Alternated modulation and to assess the usefulness of the developed CM equivalent circuits under the definition of V_{cmZC}.

1.5.3.1 Evaluation of The proposed solution

The first set of simulations is aimed at verifying the effectiveness of the proposed internal return path solution at reducing i_{cm} value in CSI7 topologies.

Table 1.13. Power Converter Parameters

Name	Value	Unit
L_{DC}	2	mH
f_S	25	kHz
T_{ov}	2	us
V_{grid} (line-to-line)	400	V (rms)
f_{grid}	50	Hz
L_f	1.4	mH
L_{cm}	2	mH
C_f	1.5	uF
R_g	4.7	Ohm
C_{mid}	7	uF

Table 1.14. Nameplate values of the PV module used in simulations.

Name	Value	Unit
V_{mpp}	30.3	V
I_{mpp}	8.24	A
$C_{PV_{single-module}}$	37.5	nF

For a better modelling of the actual condition, a common mode choke with inductance equal to L_{cm}=3x2mH is considered.

Table 1.13 summarizes all the relevant simulation parameters for the power converter simulations.

A simulation comparison between three different topologies with alternated SVM is carried out in Figure 1.73 considering the ground leakage current as benchmark: CSI, CSI7 and CSI7 with return path (CSI7+RP). Even with a visual inspection of the waveforms, it is evident that there is a significant benefit changing from a CSI topology to a CSI7 one. CSI7+RP reduces the ground leakage current even further.

Figure 1.74 shows the phase voltage, grid current and i_{RP} in the case of CSI7+RP. Return path current i_{RP} results 0.17 A (rms) with a phase current of 1.41 A (rms).

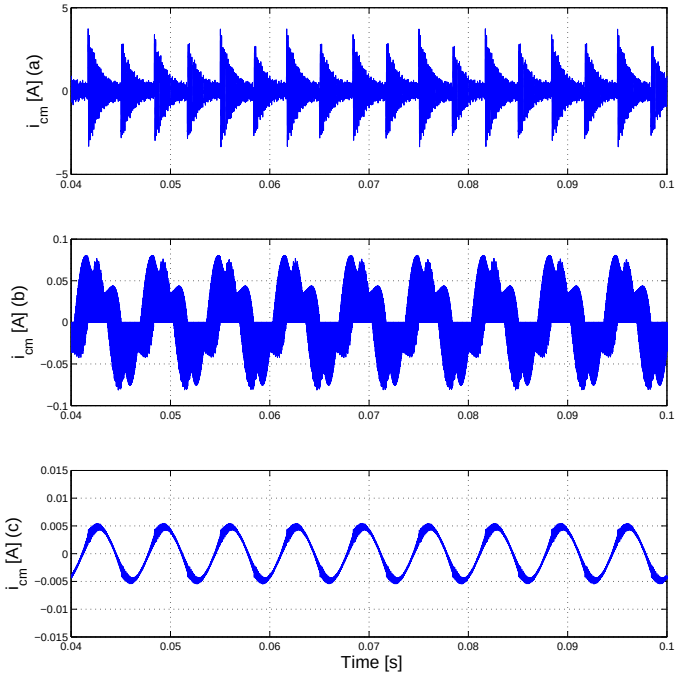


Figure 1.73. Simulation results. i_{cm} with CSI (a), CSI7 (b) and CSI7+RP (c). PV source composed by 4 modules (1kW).

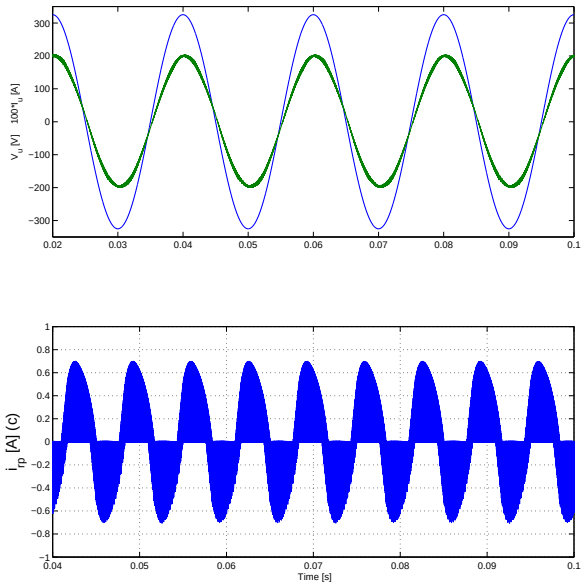


Figure 1.74. Simulation results. Voltage and current (green trace, x100) and i_{RP} waveforms in case of CSI7+RP. PV source composed by 4 modules (1kW).

An analysis of the current flowing through the filter capacitors I_{C_f} shows that no great difference exists between the topologies.

The performance comparison considering a different number of PV modules vor the CSI7+RP is reported in Table 1.15. The increase of the modules implies an increase of the ground leakage current. It can be seen that this increment is non linear (more than proportional) because the increase of C_{PV} reduces the effectiveness of the return path if considering the same value of C_{mid}, for different number of modules. In fact, an increased C_{PV} would reduce the impedance of the grid return path compared to the internal return path.

From the same table it is possible to see that the RMS value of i_{RP} is proportional to the number of PV modules due to the proportional increase of the harmonic amplitudes of v_{cmZC}. The value of the return path current is always moderated.

1.5.3.2 Validation of the Common-Mode Circuit

A second set of simulations was used to assess the proposed CM equivalent circuits. The applied method is a two-step process comprising a first step during which the converter operation is simulated with zero C_{PV} and with the disconnection of i_{cm} RP. The resulting V_{cmZC} is measured and applied to the equivalent CM circuit (see Fig. 1.65 by means of a controlled voltage source, in order to obtain the expected quantities i_{cm} and i_{RP}.

A subsequent simulation of the entire converter with the specified value of C_{PV} and with the connection of the additional return path is then run and the resulting same quantities are compared against each other. Since the additional return path is not technically feasible in case of traditional CSI, all the simulation were carried out only for the CSI7 topology with return path.

Table 1.15. Simulation results summary with CSI7+RP and CSI7 (only for I_{cm} between brackets)

Name	2 PV modules	4 PV modules	8 PV modules	Unit
$P_{modules}$	500	1000	2000	W
C_{PV}	75	150	300	nF
I_{cm}	0.51 (8.3)	3.5 (17)	13.7 (33.5)	mA (rms)
I_{RP}	66	170	290	mA (rms)
THD[%] I_u	0.99	0.98	1.08	%

Figures 1.75 and 1.76 show respectively the i_{CM} waveform and a zoomed-in view of the same: as it can be seen by comparing the results obtained with the actual converter simulation against the ones from the equivalent CM circuit, there is a very good level of agreement.

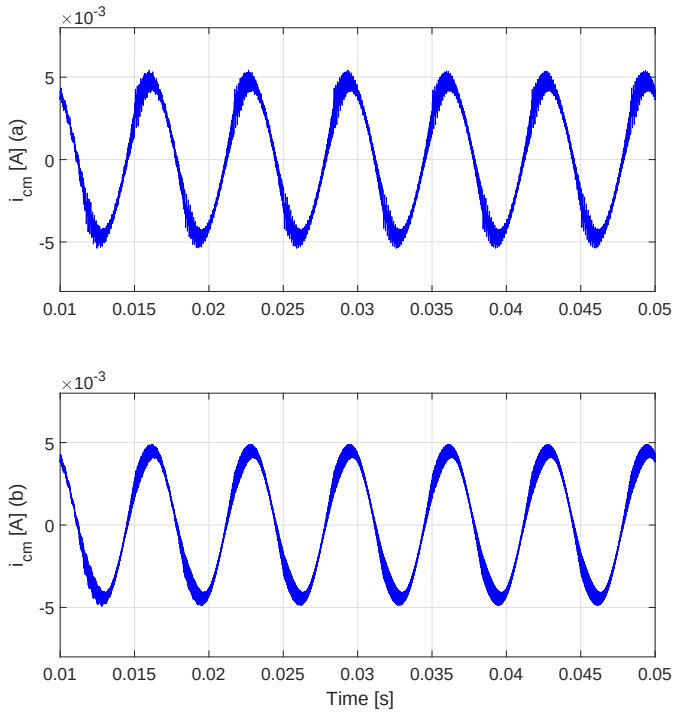


Figure 1.75. Waveform comparison of I_{CM}: upper trace - actual converter; lower trace - equivalent CM circuit.

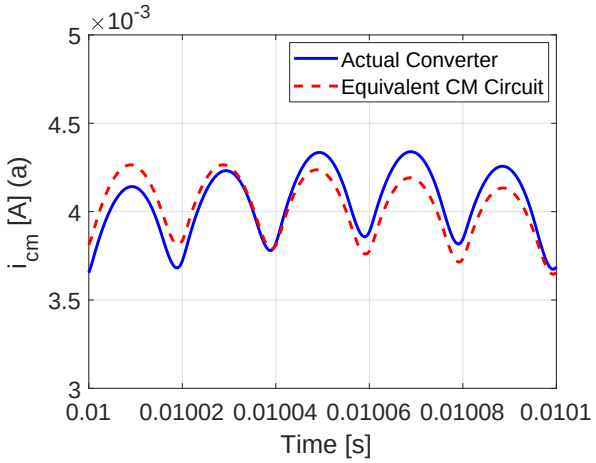


Figure 1.76. Zoomed-in waveform comparison of I_{CM}: solid line - actual converter; dashed line - equivalent CM circuit.

The same considerations apply in case of figs. 1.78 and 1.77, that show respectively the i_{RP} waveform and a zoomed-in view of the same. Comparing the results obtained with the actual converter simulation against the ones from the equivalent CM circuit results in an excellent level of agreement. The good agreement was obtained despite the neglecting of the power converter behavior during overlap times.

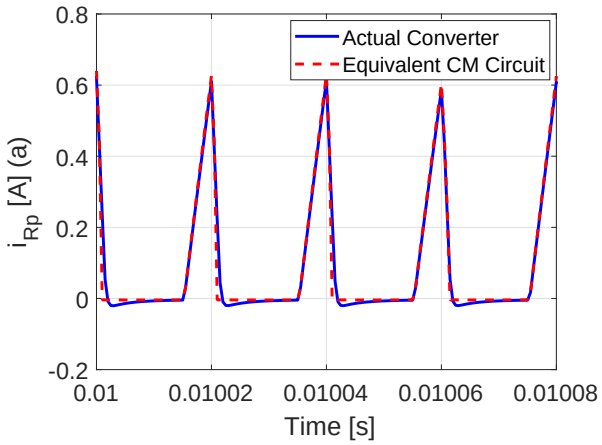


Figure 1.77. Zoomed-in waveform comparison of I_{Rp}: solid line - actual converter; dashed line - equivalent CM circuit.

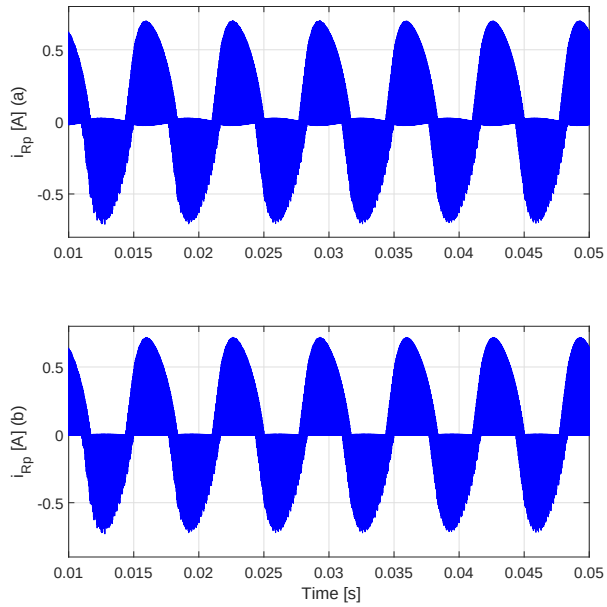


Figure 1.78. Waveform comparison of I_{Rp}: upper trace - actual converter; lower trace - equivalent CM circuit.

1.5.4 Experimental validation

A power electronics converter implementing the CSI7 and CSI7 with return path capabilities was realized and the prototype is shown in Fig. 1.19. The goal of the experiments is to evaluate the performance related to the ground leakage current of the different architectures. To decouple the effects of a real grid, the prototype is run in island operation. A balanced resistive load (value 252 Ohm) is used as load and the other experimental parameters match the ones used in the simulations (TABLE 1.13). The DC voltage $V_{DC} = 120V$ with a $C_{PV} = 100nF$. The reference current is $0.91A$) (rms) to match an equivalent grid voltage V_{grid} (line-to-line)= $400V$ (rms). Because of the intrinsic boost operation of the CSI, the input voltage must be lower than the line-to-line output voltage.

The results are shown in Figures 1.79 and 1.80. A phase voltage with the

ground leakage current i_{cm} and return path current i_{RP} for both solution is shown.

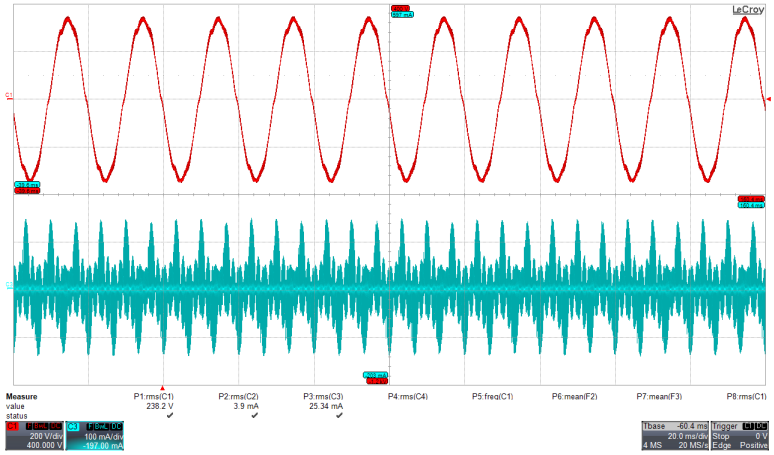


Figure 1.79. Experimental results. CSI7 topology, $i_u(t) * R_L$ (upper trace, 200V/div.), and $i_{cm}(t)$ (lower trace, 100mA/div.).

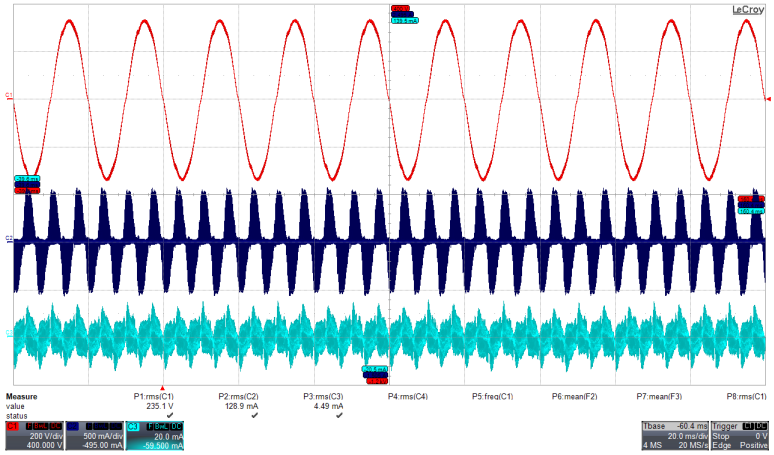


Figure 1.80. Experimental results. CSI7+RP topology, $i_u(t) * R_L$ (upper trace, 200V/div.),$i_{RP}(t)$ (middle trace, 500mA/div.) and $i_{cm}(t)$ (lower trace, 20mA/div.).

Although several assumptions were made in the simulation part and several non-linear effects of the power converter were not modeled, the mitigation of i_{cm} from $25.3mA$ (rms) to $4.5mA$ (rms) is confirmed. The current of the return path amounts to $129mA$ (rms).

Table 1.16. Experimental and simulation results comparison (simulation results between brackets)

	CSI7	CSI7+RP	Unit
I_{cm}	25.3 (17)	4.5 (3.5)	mA (rms)
I_{RP}	n.a.	129 (170)	mA (rms)

In order to obtain a better agreement between simulations and experiments a better modeling of the power switches S_x should be carried out. The non linear output capacitance of the power transistors and the junction capacitance of the diodes should be taken into consideration in the simulation of the entire actual converter.

1.6 CSI Single Phase Topologies

This chapter presents a grid-tied single-phase photovoltaic microinverter based on Current Source Inverter (CSI) topology. The main topic of this work is related to the identification of a topology and a PWM strategy able to minimize the issues of the basic CSI solution: efficiency and ground leakage current. The proposed architecture is called CSI5 topology and allows to reduce strongly the ground leakage current respect to basic CSI, enabling its use in conjunction with thin film modules typical of building integrated installations, with a lifetime more close to that of PV Panels.

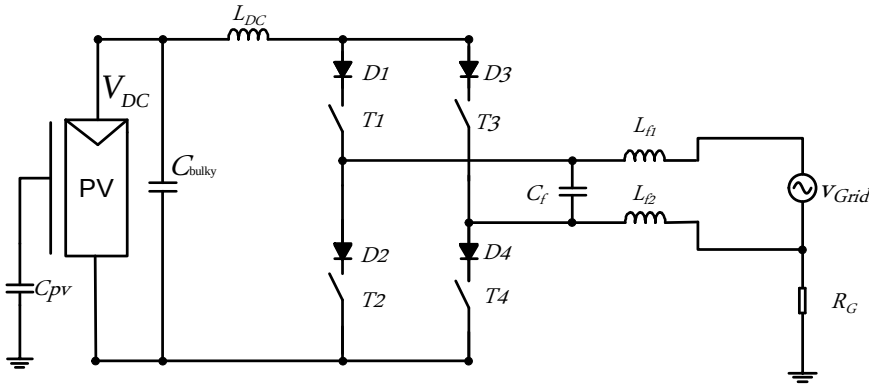


Figure 1.81. Conventional single-phase CSI topology for PV systems.

Electric energy production from photovoltaic sources is nowadays well established. Besides centralized and multi-strings inverters, [32] another type of converter, known as micro-inverter or string inverter faced the market. At the extreme, this approach aims at integrating miniaturized dc-ac inverter into each photovoltaic (PV) module, obtaining a Module Integrated Converter (MIC). In this way it is possible to obtain better performance for the MPPT algorithm applied at PV module level, that is especially effective in case of partial shading. Another benefit is the reduction of installation costs via product

standardization, since standard and low cost AC wires and AC circuit breakers can be used instead of dedicated switch gear components for high power DC connections. Figure 1.81 shows the basic single-phase Current Source Inverter (CSI) for PV grid connected system. This architecture is not used in commercial applications because of big drawbacks in terms of efficiency and power decoupling capability. The latter in fact is a peculiar feature in single phase PV inverter's design: the optimal performance in PV modules power generation is obtained by MPPT algorithm imposing a quasi constant instantaneous output power for every PV module. In case of single phase installations, the instantaneous output power injected into the grid follows a periodic fluctuation at twice the grid frequency. For the sake of simplicity, the single-phase CSI topologies will be analyzed considering an ideal current source as the power source. In this analysis the injection of electric power into the grid operates at unity power factor. The focus of this section is to analyze the performance of the single phase CSI in terms of ground leakage current, against the presence of the distributed parasitic capacitance of PV panels.

Despite its well known drawbacks in terms of conduction losses, CSI topology could offer some advantage when employed in PV applications: it is a single stage architecture, thanks to its inherent boost capability. In PV three-phase grid-connected converters the energy storage component is an inductor [14], with a superior ruggedness and longer lifetime compared to electrolytic capacitors employed in VSI. In MIC solution for single-phase grid the use of only an inductor for the energy storage led to an unacceptable bulky DC inductor and therefore an additional power decoupling circuit is needed. Recently PV CSI architectures have been proposed for full-sized PV arrays both in single phase [33], [34] and three-phase [35] architectures, but also for MIC solutions for three-phase distribution grids [36]. This thesis proposes and analyses a modified Current Source Inverter topology, named CSI5 able to improve the

performance of the conventional single phase CSI in terms of efficiency and also capable of reducing ground leakage current almost to zero. These improvements are analyzed in the following sections in order to verify the effectiveness of this power converter employed as a PV MIC. In particular this section is mainly focused on ground leakage current reduction, enabling the use of the proposed architecture in conjunction with thin-film PV modules in building integrated installations. The power decoupling capability relevant for single phase operation is not analyzed in depth in the present work.

1.6.1 Conventional single-phase CSI topology

Figure 1.81 shows conventional CSI topology applied to PV systems. The Figure shows also an equivalent lumped parasitic capacitance, C_{PV}, of the PV string connected between the earth and the frame of the PV panels [13]. Resistance R_G represents the ground resistance between the neutral connection and the earth. The command sequence of the four transistors in the H-bridge (T1,T2,T3 and T4) is obtained with the simple strategy shown in Fig. 1.82. Considering grid-tied operation, the sinusoidal waveform shown in Fig. 1.82 represent the normalized grid voltage if the reactive power related to the output filter can be neglected and a unity power factor operation is desired. In other cases, this sinusoidal waveform must have a proper phase displacement from the grid voltage, to compensate for reactive power.

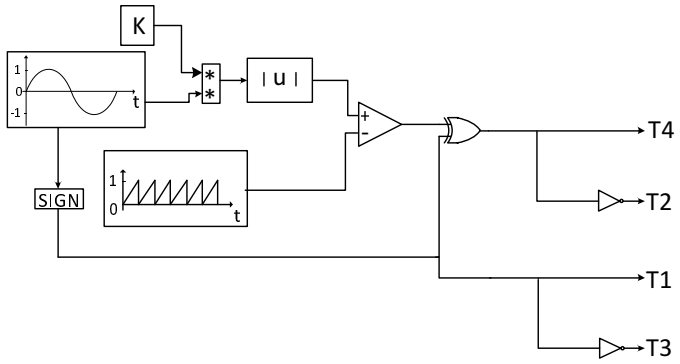


Figure 1.82. Basic single-phase CSI control.

For every semi-period of the grid voltage the states of H-bridge are only two: Active State with the turn ON of one diagonal (in case of positive semi-period T1 and T4 ON) and the Zero State with the turn ON of one of the two legs of H-bridge (in case of positive semi-period, T1 and T2 ON). In the latter case, zero current is provided to the grid. Figure 1.83 shows the insertion of the small overlap time applied to any switch command transition in order to always provide a path for the DC input current in presence of actual commutations of the transistors, operating with different turn-off and turn-on time intervals.

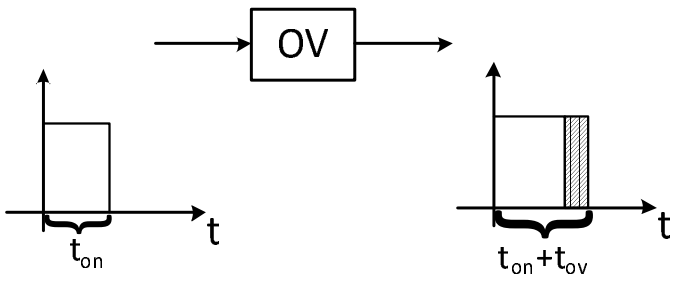


Figure 1.83. Overlap time insertion.

In grid-connected VSI the PWM strategies and different topologies solutions for ground leakage current reduction starts from the analysis of common-mode voltage. In single-phase CSI converter the analysis begins from the ground voltage waveform measured between the neutral of the grid generator and negative terminal of the DC power source. In case of a PV system, it is considered

that this voltage is applied to the equivalent lumped PV parasitic capacitance, C_{pv}, with in series the ground resistance. Since the impedance of C_{pv} against high frequency voltage components is very low, the high frequency component of ground voltage has to be minimized.

In the following the ground voltage waveform, V_{ground} , is computed in case of conventional CSI solution operating at unity power factor. Referring to Fig. 1.84, v_{ground} is analytically computed in case of positive and negative semi-periods of the grid voltage, respectively during both Active and Zero states. Figure 1.85 shows the evolution of v_{ground}. This waveform was computed in a simulation environment with a grid voltage equal to 230VRMS @ 50Hz and with a null value for C_{pv}.

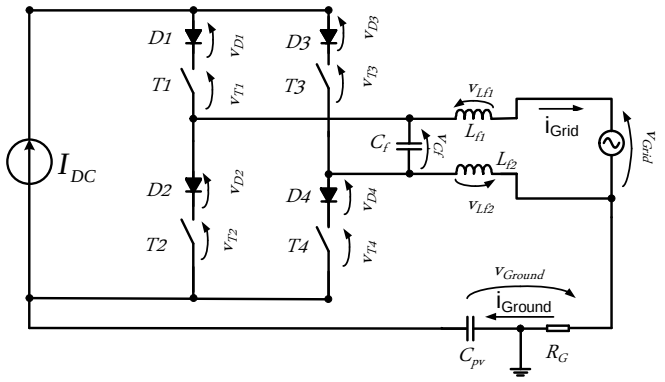


Figure 1.84. Conventional single-phase CSI.

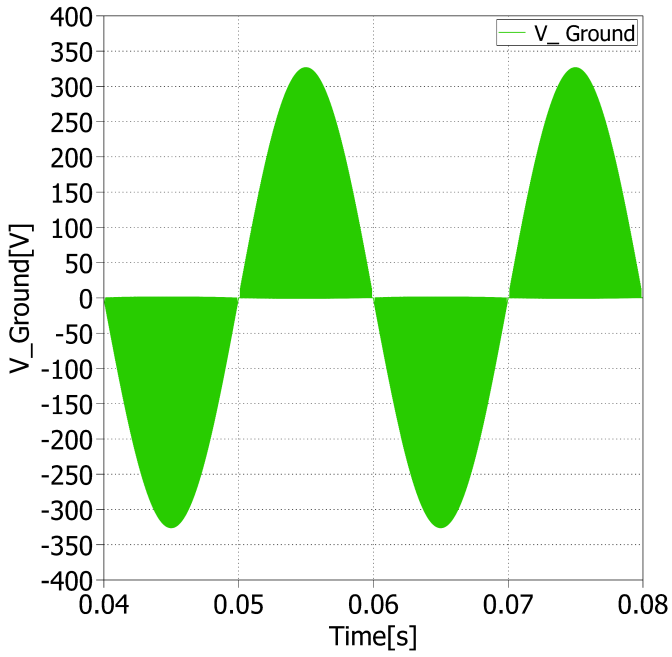


Figure 1.85. v_{ground} waveform in case of traditional CSI solution.

1.6.2 Proposed single phase CSI topology - CSI5

Figure 1.86 shows the proposed modified single-phase CSI that allows a strong reduction of the ground leakage current. The figure shows the fifth switch T5 and the two additional transistors T_{ad1} and T_{ad2} applied to the basic CSI topology. By turning ON the transistor T5, a Zero State is obtained. This configuration is equivalent to the simultaneous turn ON of the two transistors of one leg of the H-bridge but the associated conduction losses are halved. It is important to stress that when the T5 is turn ON all the other 4 switches are Off. Only during the small overlap time T5 and one diagonal of the H-bridge (T1 and T4, or T2 and T3) are simultaneously turned ON.

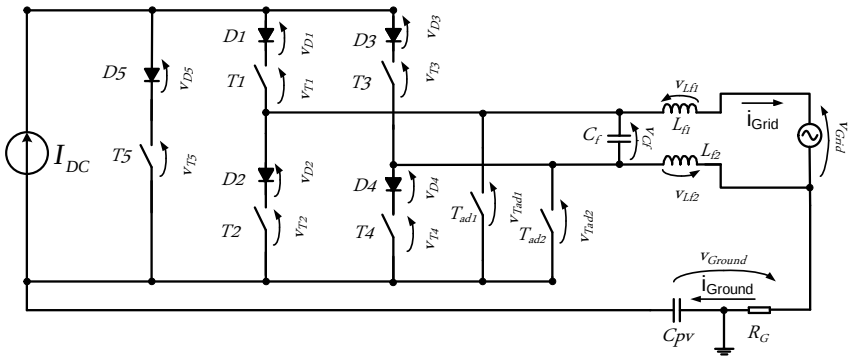


Figure 1.86. Proposed single-phase current source inverter CSI5

In this way it is possible to reduce conduction power losses during the Zero State and it is also possible to obtain zero current commutations (ZCS) for the four transistors of the H-bridge thanks to the overlap time. Since during overlap time the input current flows always through T5, the commutations of the other transistors take place under zero current. On the other hand the commutations of T5 are always hard switching. In order to maximize the converter efficiency T5 should be chosen with different criteria than the other transistors e.g. a SiC device would be preferred. The aforementioned conditions determine a decrease in power losses but they don't represent the main advantage of the proposed topology in terms of ground leakage current reduction. Ignoring the overlap time, the grid generator during the Zero State is disconnected from the DC source if both the two additional transistors are Off or if they are not present in the converter's topology. In fact in this case the voltage at the input of the H Bridge is floating with respect to grid generator. The two additional switches T_{ad1} and T_{ad2} avoid the presence of this floating voltage by clamping it to the better available voltage value with the aim of minimizing the variation of the ground voltage. In this way, T_{ad1} and T_{ad2} allow to impose the ground voltage across the parasitic capacitance C_{pv} during the Zero State and therefore limit the ground voltage variations. In particular, only one of the two additional switches is turned ON during the ON state of transistor

T5: respectively T_{ad2} during positive semi-period and T_{ad1} during the negative semi-period. In order to obtain the best performance for any power factor operation, these two additional switches must also be bidirectional switches with reverse blocking characteristic and not simple single transistor. Figure 1.87 shows the simple schematic block diagram for the generation of the PWM commands for T_{ad1} and T_{ad2}.

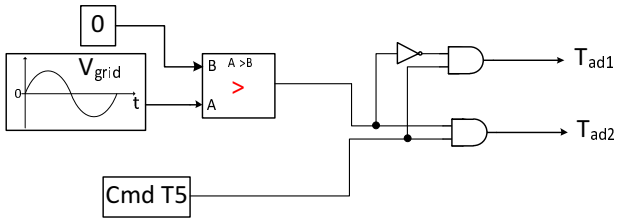


Figure 1.87. Block diagram of PWM commands generation for T_{ad1} e T_{ad2}

Thanks to the proposed topology and PWM control strategy it is possible to reduce the ground voltage variation, thus greatly limiting ground leakage current. Referring to Fig. 1.86 and with the same methodology applied for conventional CSI architecture, the evolution of the ground voltage is computed for an entire period of the grid voltage.

Positive semi-period:

$$Activestate, v_{ground} = +v_{Lf1_{AS}} + v_{D4} + v_{T4} \tag{1.6.1}$$

$$Zerostate, v_{ground} = +v_{Lf2_{ZS}} + v_{T_{ad2}} \tag{1.6.2}$$

Negative semi-period:

$$Activestate, v_{ground} = -v_{Lf1_{AS}} - v_{grid} + v_{D2} + v_{T2} \tag{1.6.3}$$

$$Zerostate, v_{ground} = -v_{C_f} - v_{Lf2_{ZS}} + v_{T_{ad1}} \tag{1.6.4}$$

Figure 1.88 shows the evolution of the ground voltage by applying the proposed solution. As can be seen, during positive semi-period the ground voltage is very low and determined by the low voltage drops across the output filter inductance, diodes and transistors. Instead during negative semi-period the voltage ground variation follows the grid voltage. In this phase the lowest ground voltage variations during Active and Zero State can be obtained when the voltage across C_f is equal to v_{grid}. This could be obtained by choosing C_f with an high capacitance value, that however can not be excessive in order to avoid a large reactive power introduced by the output filter.

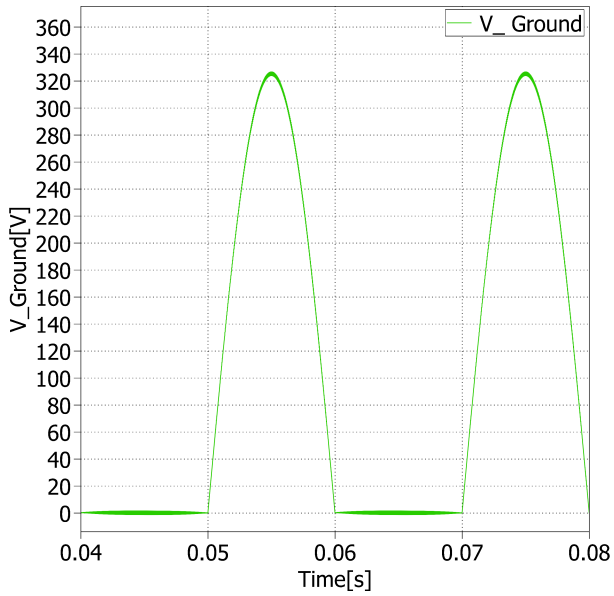


Figure 1.88. v_{ground} waveform in case of proposed solution.

1.6.3 Simulation Results

Both the conventional and proposed CSI topologies were simulated and compared in PLECS environment. The converter topologies are the same showed

in Fig.1.84 and Fig. 1.86. Table 1.17 summarizes the simulation parameters. Two sets of simulations were carried out with different DC sources: an ideal current source (I_{DC}) and a simple model of a PV panel. The overlap time (see Fig. 1.83) was inserted before the transition command of every transistors. In the first set of simulations the modulation index K (see Fig. 1.82) was kept equal to 0.4.

Table 1.17. SIMULATION PARAMETERS

Name	Description	Value	Unit of measurement
I_{dc}	DC current power supply (used as DC source in the first set of simulation)	1.55	A
v_{grid}	Grid Voltage (50Hz)	230	V_{RMS}
L_{f1}, L_{f2}	Inductor output Filter	0.5	mH
C_f	Capacitor output Filter	2.2	uF
C_{pv}	Equivalent PV parasitic capacitance	330	nF
R_G	Ground resistance	3	OHM
t_{ov}	Overlap time	0.5	us
f_{sw}	Switching frequency	30	kHz

Without any degradation of the power quality caused by equivalent parasitic capacitance, the injected power into the grid is equal to 100W. The control strategy implemented in the simulation environment for the two solutions are those showed in Fig. 1.82 and Fig. 1.87 and no additional dedicated power factor correction was employed. Figure 1.89 shows the grid voltage and injected grid current characterized by a strong deterioration due to the presence of a very high ground leakage current, i_{ground}, that is also shown. It is to be pointed out that in both simulations no common-mode filters were implemented.

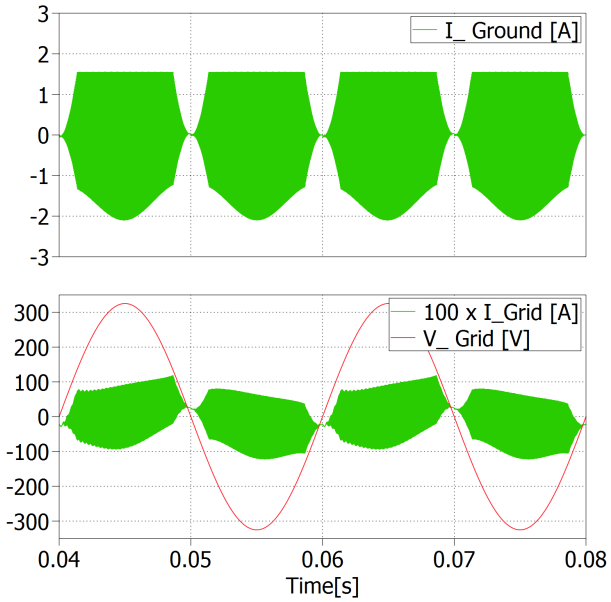


Figure 1.89. Ground leakage current, injected grid current (x100) and grid voltage in case of CSI conventional topology. The RMS of the ground leakage current results equal to 1.09 ARMS.

Figure 1.90 shows the same quantities in case of the proposed solution. It is evident the strong reduction of the ground leakage current. The phase displacement of the injected current is due to output filter reactive power, not compensated by the converter control. This can be compensated adding in the control strategy of Fig. 1.82 a phase displacement for the sinusoidal waveform. Figure 1.91 shows the FFT of the ground leakage current.

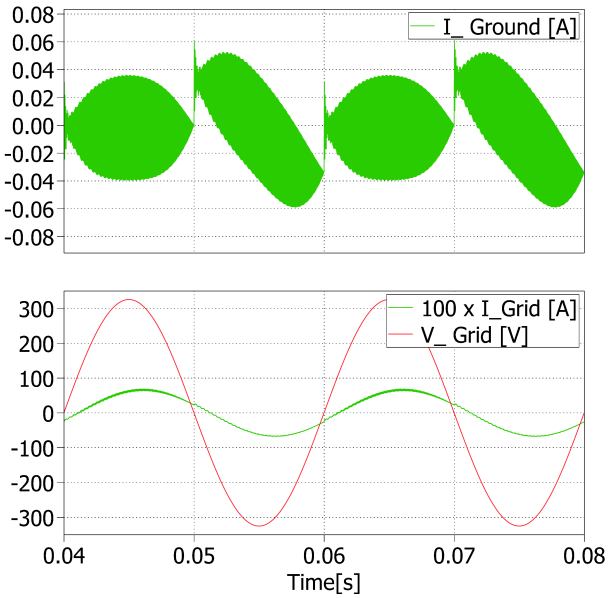


Figure 1.90. Ground leakage current, injected grid current (x100) and grid voltage in case of proposed CSI5 topology. The RMS of the ground leakage current results equal to 27 mARMS.

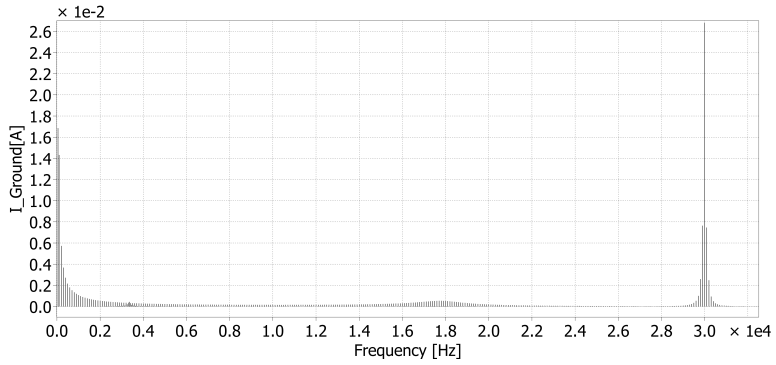


Figure 1.91. FFT of ground leakage current in case of proposed solution.

The currents flowing in the additional transistors T_{ad1} and T_{ad2} are very low, as Fig. 1.92 shows together with the voltage applied to them when they are in Off State, for every semi-period of the grid voltage. The RMS current flowing on T_{ad1} and T_{ad2} are respectively equal to 18 mARMS and 10 mARMS. The two currents are different because of different current paths, Fig. 1.86.

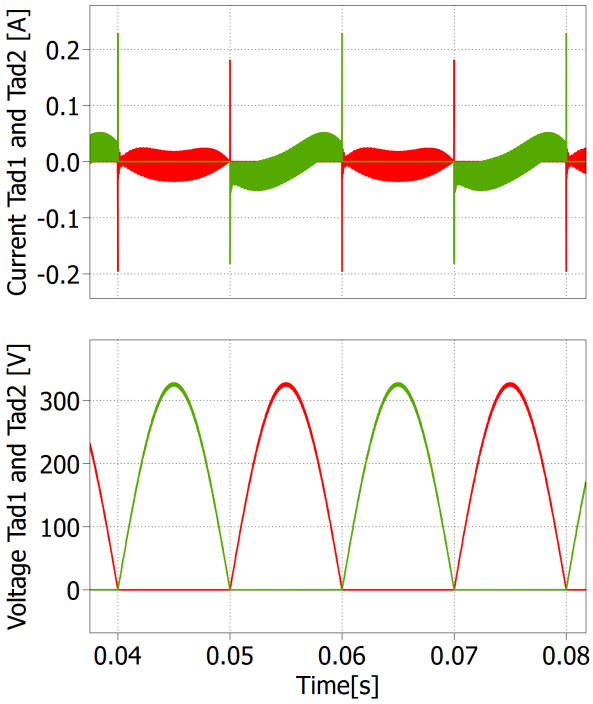


Figure 1.92. Voltage and Current of the additional transistor T_{ad1} (green trace) and T_{ad2} (red trace).

Other simulations were conducted in order to verify the robustness of the solution in case of a difference of inductance of L_{f1} and L_{f2}: in particular with a difference of the 20% (L_{f1}=450μH and L_{f2}=550μH) the RMS of iground results equal to previous value (27 mARMS), while RMS current that flow in Tad1 and Tad2 are respectively equal to 18 mARMS and 12 mARMS: a negligible difference. In the second set of simulations the DC current source was substituted with a PV film panel with VMPP=60V and IMPP=1.75A. Without an active power decoupling solution integrated in the system, if this task is performed only by the input DC inductance, its value would be unacceptably big for practical applications. A first solution to solve this problem is to add an additional transistor and diode between the PV panel and the input DC inductance as showed in Fig. 1.93.

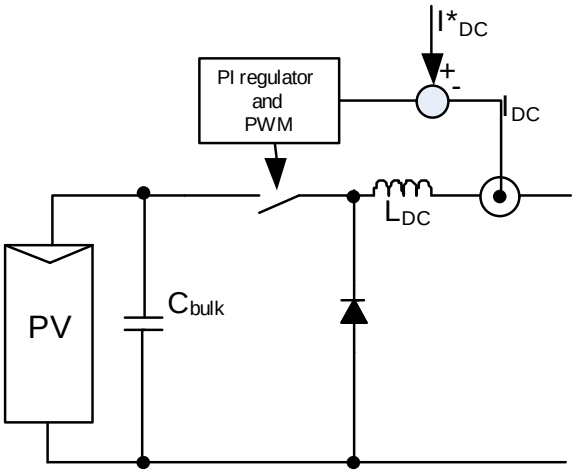


Figure 1.93. DC input current control for input DC inductance minimization.

This figure shows the input DC current loop control of the CSI converter able to guarantee a proper operation with a relatively low value for L_{DC}. It is important to put in evidence that this solution does not implement a power decoupling but only allow to minimize the L_{DC} value. With this power converter architecture the power decoupling remains in charge to the input DC capacitance C_{bulk}. For this new simulation the switching frequency of the DC input current control was set equal to 100kHz, the input inductance L_{DC} was set equal to 500μH and the input capacitance C_{bulk} equal to 2200μF. The other simulation parameters are the same summarized in Table 1.17.
Figure 1.94 shows an acceptable variation of the PV input power, necessary for the tracking of the MPP of the PV panel. The variation of the current that flows in the DC inductance L_{DC} does not determine a THD in the injected grid current thanks to the use of a PAM modulation [37]. In this simulation result the compensation of the reactive power of the output filter was carried out by displacing the reference sinusoidal waveform of Fig. 1.82 by $\pi/8$ phase angle, in order to obtain unity power factor operation.

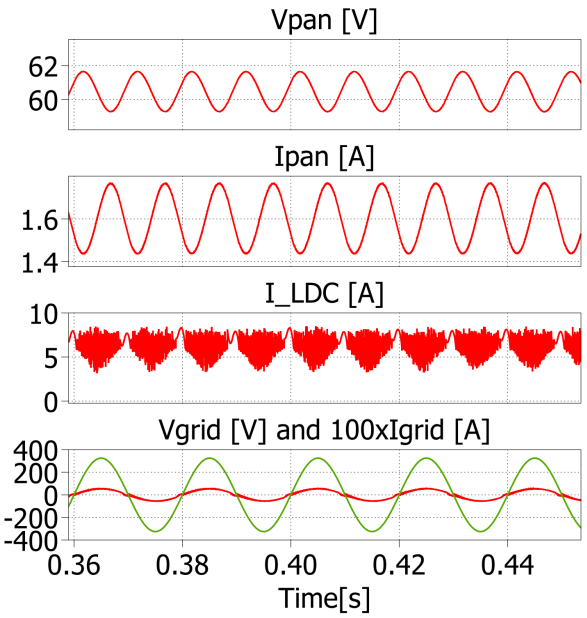


Figure 1.94. Simulation results with PV panel, DC input current regulation and PAM modulation.

1.6.4 Low Voltage Experimental Validation

A low voltage experimental setup was realized to validate the basic CSI5 solution showed in Fig. 1.86 in terms of ground leakage current reduction. In particular the following experimental results compare the performance of the traditional single-phase CSI solution with the proposed one in case of an experimental setup with the following parameters: DC source realized with a DC power supply of 30V with a series resistance of 30Ω, input inductance L_{DC} equal to 1mH, switching frequency equal to 30kHz, output filter of the CSI5 architecture equal to L_{f1}=L_{f2}=1mH and C_f=1.5 uF, R_G=5 Ω and C_{pv}=250 nF. The comparison was carried out in stand-alone operation of the power converter, therefore the grid generator was substituted with a simple power resistance of 42Ω. Figures 1.95 and 1.96 show the scope traces of the experimental setup, highlighting the capability of the proposed solution to reduce the ground leakage current from 22.7 mARMS to 6 mARMS.

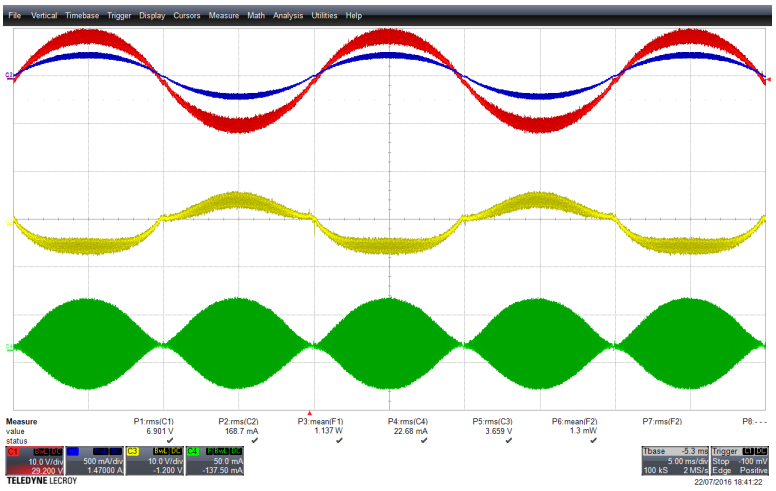


Figure 1.95. Experimental results of Traditional CSI solution. From top to bottom trace: output voltage (red trace, 10V/div), output current (blue trace, 500mA/div), ground voltage (yellow trace, 10V/div) and ground leakage current (green trace, 50mA/div).

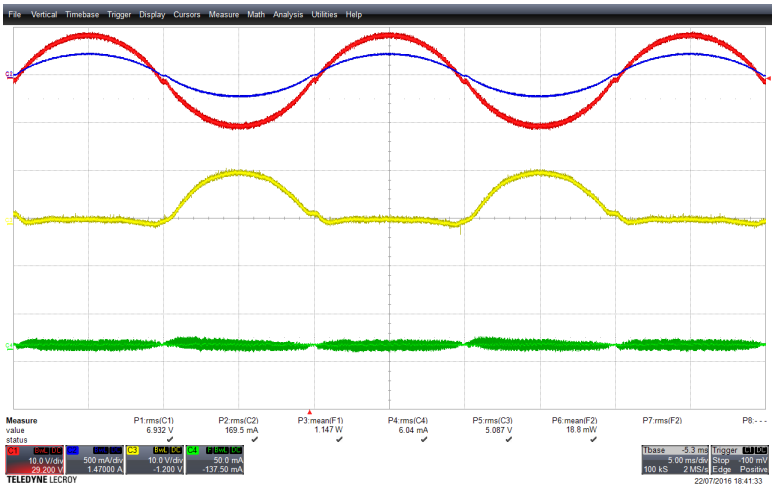


Figure 1.96. Experimental results of proposed CSI5 solution . From top to bottom trace: output voltage (red trace, 10V/div), output current (blue trace, 500mA/div), ground voltage (yellow trace, 10V/div) and ground leakage current (green trace, 50mA/div).

Chapter 2

Advantages of the Current Source Inverter for aerospace motor design

This section deal with the advantages in the use of CSI for the design choices of electric machines used more electric aircraft scenario. This analysis evaluates in particular the size reduction of the electric machine if this last one is driven by a CSI instead of a VSI in case of applications in which the machine works for almost all the time at high speed, i.e. pumps for cabin pressurization. This part is the result of a collaboration with University of Nottingham and University of Nottingham Ningbo-China. The finite element analysis of the electric machine was done by University of Nottingham researchers.

2.1 Setting the context

The actual panorama of variable speed drives is totally dominated by the VSI, the aim of this section is to investigate how the CSI can find its niche in specific applications due to its peculiar characteristics. Indeed, the intrinsic voltage boosting capability can be exploited in applications where the power density is of paramount importance, as aircraft application. A main aim of the more electric aircraft (MEA) concept is the reduction of jet fuel consumption and therefore less emissions. A common school of thought in this area is to try to achieve this by working towards ever more efficient aero engines, with the ultimate aim of a completely bleed-less engine scenario. Thus, all the air being compressed by the engines will be used for propulsion, without having to also feed all the secondary systems onboard the aircraft. However, in modern commercial aviation history, this aspect has never been fully implemented. The traditional limitations on the amount of electrical power that is typically generated on-board was always in contrast with the actual amounts of power that are required to operate all the secondary systems. Examples of huge power drainers include the aircraft ECS and de-icing systems. The absolute values of the power required by these systems were always simply too much. However, the introduction into the market of the Boeing 787 in 2011 represented a paradigm-change in the aerospace community [38]. With its total installed power of 1 MVA (main generators only), the B787 was the first commercial platform to be considered a really "more electric aircraft" (MEA) [39]. This "power anomaly" is easily spotted in Figure 2.1, where the (main) generators power is plotted against the engines take-off thrust for various commercial aircraft. This step-change in the value of power generated on-board the B787 is due to two main aircraft design choices, namely that the cabin's ECS and the aircraft's de-icing system are both electrically controlled. The B787's composites-based body allows for much higher levels of cabin pressurisation and this therefore under-

pins and justifies the use of electrically controlled ECSs. It is also important to note that an added advantage of these choices is that the B787 can then comprise a completely bleed-less engine, i.e. no air is needed to be bled from the turbofans to actuate the secondary systems. For completeness, Figure 2.2 and Figure 2.3 show a schematisation of conventional and a no-bleed engine architectures respectively. Thus, the B787 is the first commercial aircraft to have a fully electrically controlled ECS. Today's implementation comprises a VSD that makes use of a VSI configuration. The system's electrical machines (EMs) are fed by a Power Electronics Converter (PEC) to precisely control the speed and thus allowing optimal and efficient operations. In the B787, the same PEC is also used for engine-starting purposes, operating the variable speed starter/generator in motoring mode [40]. The VSI-based drive has been shown to be extremely well-suited to the application at hand. However, as shown later in this work, considering the nature of the application, then even better performance can be achieved when a machine with higher voltage is employed for the design. Higher voltage for the machine would imply either a VSI with dc-dc front-end with a large capacitive dc-link to step up the bus voltage. However, with a CSI solution, this could be achieved smoothly.

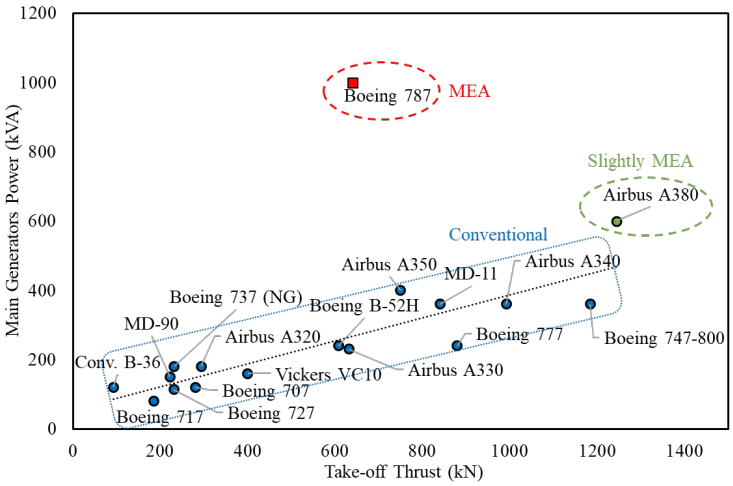


Figure 2.1. Main generators power vs. take-off thrust for various aircraft.

This chapter will therefore develop a comparative study that pits a CSI drive (preferred to the boost converter + VSI solution due to the reduced capacitance required) against the traditional VSI drive for the control of a permanent magnet synchronous machine (PMSM) powering/driving an ECS compressor. Alternatively, Z-source or quasi Z-source Inverter topologies [41], [42] can be used to step-up the input DC link voltage, however the commutations are similar to those of a conventional VSI. This means that, for an EM fed by a Z-source inverter topology, the insulation must be designed to withstand PWM-modulated pulses. Additionally, if wide bandgap devices are used, the stress on the insulation is further enhanced, compromising the overall drive reliability. The advantages of a drive based on the CSI topology against the more conventional VSI in the context of a low voltage, high speed application are derived.

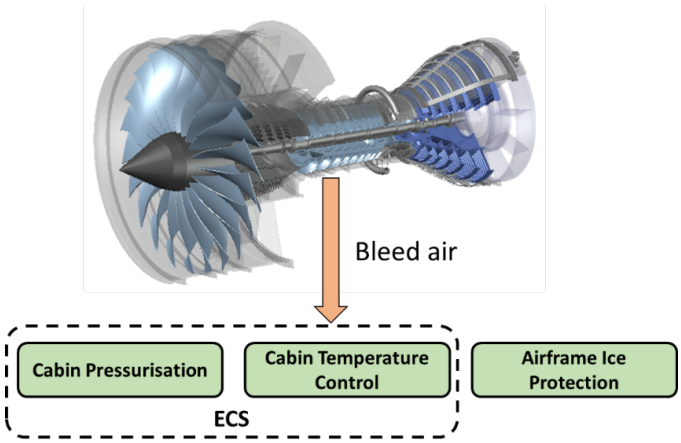


Figure 2.2. Conventional turbofan engine with bleed air extraction for powering secondary sub-systems.

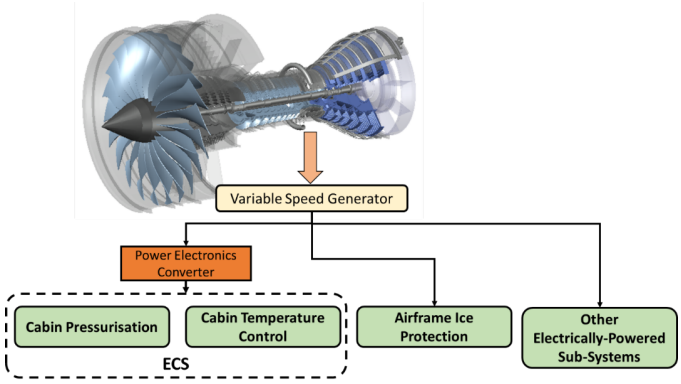


Figure 2.3. No-bleed engine where secondary systems are electrically-powered.

2.2 The Current Source Inverter

For CSI systems, one of the first related patents was presented by L. W. PARKER in 1939 [43]. The intrinsic voltage boost capability of this first topology, named Direct Current voltage booster, was at that time primarily used for driving the then so-common vacuum tubes, that performed the required switching operations. The subsequent designs made use of Silicon Controlled Rectifier, that exhibited the reverse voltage blocking capability could be controlled both in turn-on and turn-off. The development of semiconductor technology and the large availability of Insulated Gate Bipolar Transistors (IGBT) cleared the way for the VSI to become the dominant technology in electrical drives. The high voltage blocking capability, the ease of driving and the very good conduction and switching performance made very easy the realization of a VSD with just 6 IGBT and 6 diodes. The characteristic of the IGBT to be in a blocking state when the gate is not energized constituted a safety element that simplified the protection system: during a fault, all devices could be de-energized, stopping the power flow. Realizing a CSI with devices highly optimized for VSI application proved to be a hard task, since the need of adding a series diode to the IGBT to ensure the reverse blocking capability,

Table 2.1. Topology Comparison.

Characteristic	**VSI**	**CSI**
Output capability	Buck	Boost
Input Filter	Capacitor	Inductor
Leg Switching Behaviour	Dead Time	Overlap time
Output Current THD	Low	Low
Output Voltage THD	High	Low

practically doubling the conduction losses. Due to the presence of an inductive dc link, during a faulty situation, it must be ensured that the inductor current has a free-wheeling path. Even when the power flow stops, the devices must be switched on to avoid the inductor open-circuit and the consequent converter destruction. Additionally, making the CSI bidirectional would imply doubling the number of active devices, making the adoption from industry virtually impossible. The most distinguishing feature of a CSI is that its output voltage is higher than its input voltage. Whereas the VSI topology "slices" the input voltage, behaving as a buck converter (the output voltage is lower than Input voltage), the CSI converter behaves as a boost converter. Also, a CSI requires a current source. This is usually provided by a pre-stage sub-system that operates in continuous conduction mode, which of course deteriorates significantly the system's efficiency.

An input inductor is required for a CSI. For a long time, the frequency limitation of the semiconductor devices also implied that in order to have an almost constant current, the input inductor be of quite an elevated value, resulting in bulky and heavy input inductors. A qualitative comparison of the features of classical VSIs and classical CSIs is shown in Table 2.1. From this initial description, it seems that the adoption of the CSI for a VSD is basically impossible, with the boosting capability the only superior point to the VSI. But technology can always tip the scales.

2.3 Moving forward

Today, new and more powerful technologies are however levelling the playing field more than ever before. New wide bandgap devices such as Silicon Carbide products allow for much higher switching frequencies to be operated in, while at the same time reducing conduction losses. The use of semiconductor devices, such as IGBT-RBs (i.e IXRP15N120), Dual-Gate GaN Bidirectional Switches [44] or SiC Devices (i.e C2M0025120D) can result in reducing the dimension of the input inductor with obvious benefits in terms of power density. Advances in control methodologies is another enabler for the re-birth of CSI drives. The use of an additional switch (CSI7 Topologies) can reduce conduction losses, the THD of output currents and also the ground leakage current. The latter is particularly important for aerospace applications where reliability and fail-safe systems are essential requirements. Considering all this, it is therefore very probable that customised designs can result in CSI systems that can fairly compete with VSIs. Once the differences in terms of efficiency due to the optimized devices and topology would allow to obtain very good result, its inherent voltage boost capability would make it ideal for high speed operations where only a relatively low-voltage source is available. The VSI plus dc-dc converter would still suffer from the need of a capacitive dc link and possibly an output filter (i.e. on the AC side of the inverter) due to the high voltage THD. It is also important to put in evidence that the 6 transistors of the main CSI bridge are subjected to a limited voltage swing during commutations respect to the VSI case. This voltage swing varies during time following output line-to-line voltages, in which amplitude follow obviously the machine speed. The use of the additional device S7 allows also to obtain Zero Current Commutations for the 6 transistors of the main bridge. Summarizing the CSI excellent output voltage waveform implies lower stresses on the insulation systems of the converter itself but also on the insulation systems of the EM, making it the definite winner of

the competition.

2.4 A Case-Study: High-Speed Electrical Drive Design

2.4.1 Background

This section aims at analysing the benefits arising from the implementation of a power converter with boost capability, as the CSI converter, for controlling an electrically-powered ECS compressor. The specifications reflect the actual needs for an aerospace electrical drive system to power a compressor. The system is a classical VSD, comprising a machine, a PEC and a control platform. The main design requirements and constraints for the complete drive are listed in 2.2. The selected voltage level (i.e. 270 V) is conventionally adopted for supplying VSDs in modern aircraft (e.g. B787, A350 and A380). This voltage level is obtained from the main 115/230 V AC variable frequency distribution, through the use of an auto-transformer rectifier unit [39] , [45].

Table 2.2. Main design requirements for the ECS compressor drive.

Parameter	**Quantity**
DC link voltage	270 V
Rated power	25 kW
Maximum speed	25000 rpm
Max EMF THD	5 %
Efficiency	$> 95\%$
Cooling method	Forced liquid (water jacket)
Available flow rate	6 L/min
Maximum hot-spot	150 °C +/- 10°C

The project's objective was to preliminary identify the optimal system-level configuration, including the identification and design of the PEC and of the EM. In light of this work, three main configurations comprising three differ-

ent high speed PMSM designs, were proposed and investigated. The three configurations are roughly categorised as

1. Machine 1, fed by a VSI
2. Machine 2, fed by a VSI
3. Machine 3, fed by a CSI

The three EMs are "tailored" to the available converter. That is, for each converter topology, the most optimised EM able to satisfy/meet the design requirement is proposed. It is worth remarking that the previously-mentioned VSI topologies with boost capability are not analysed in this study. Indeed, the boost capability comes at the cost of a) increased component counts and related losses, b) increased drive complexity and c) detrimental effect on the EM insulation, given by the high voltage, short rise-time PWM modulated pulses.

2.4.2 Development of EMs

The design of high-speed EMs for aerospace is a challenging task and should be tackled through a multi-disciplinary approach [46]. Some of the various disciplines involved in the design procedure of such machines are illustrated in Figure 2.4. Alongside to improved thermal management techniques [47] , [48] and electromagnetic computational tools, the design of high-speed EMs requires mechanical expertise for sizing of the rotor structure [46], [49], [50]. The stiffness and geometrical dimensions of the shaft must be carefully chosen for avoiding resonances, which might severely compromise the whole rotor structure, causing the machine outage. At the same time, the structural integrity of the rotor must be guaranteed in any operating situation, by e.g. using high strength retaining sleeves for the containment of permanent magnets (PMs)

under elevated centrifugal forces. Last (but not least) the EMs for aerospace are commonly employed in safety-critical applications, where a machine failure might endanger human life and/or cause extensive economical loss. It is then required that such EMs operate with an enhanced reliability level with respect to ground-based counterparts (e.g. home appliances, industrial and automotive). Therefore, aerospace EMs' reliability have to be assessed via physics of failure – based lifetime prediction models [51], [52] starting from an early design stage.

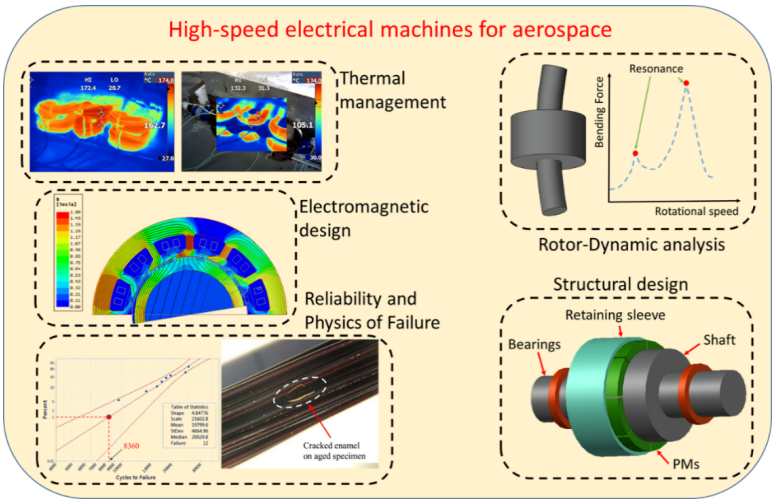


Figure 2.4. Multiphysics aspects involved in the design of high-speed EMs for aerospace.

Differently from Machine 1 and 2, the third machine is developed to be fed through the CSI converter topology presented in the previous Section. One of the main advantages of this drive topology are the benefits deriving from the voltage boost capability of the CSI. A higher per-phase voltage gives to the EM designer more freedom in the slot/pole combination choice, as well as in the selection of the winding layout. Further, because in CSI-fed EMs the terminals voltage is quasi-sinusoidal, the insulation system is less stressed than in VSI drives. In fact, the turn-to-turn insulation is only subject to a portion of the total phase voltage (inversely proportional to the number of turns per phase).

Table 2.3. Main design parameters for the three considered machines.

Parameter	**Machine 1**	**Machine 2**	**Machine 3**
Pole pairs, p	1	2	2
Slot number, Q	12	18	24
Turns per coil	5	3	5
Stator (outer) diameter, D_{out}	150 mm	155 mm	127.5 mm
Axial length, L	85 mm	98 mm	70 mm

On the other hand, in VSI drives (and in particular those adopting wide-bandgap SiC MOSFETS) the turn-to-turn insulation might experience voltage levels as high as two times the DC-link voltage [53]. Thus, a machine fed by a CSI converter can rely on lower grade (i.e. thinner) interturn insulation, enhancing the slot copper fill factor, and guaranteeing a higher power density [54].

The main design parameters of Machine 1,2 and 3 are listed in Table 2.3. The PMs are directly glued on the shaft and they are retained by a carbon fiber sleeve, similarly to Machine 1. A particular design solution, consisting in the PMs skewing by 15 mechanical degrees (i.e. 5 axial segments displaced by 3 degrees each) allows to minimise the torque ripple to 1.5%. This expedient (i.e. PMs skewing) is easily implemented in surface mounted PMSMs, whereas it leads to significant manufacturing complexity in interior PM machines (i.e. Machine 2). The Table 2.4 summarizes the main findings obtained from the FE simulations.

2.5 Discussion

All three machines show an excellent efficiency above the required target of 95 %, with the CSI version peaking over 97%. Similarly, the BEMF THD constraint is satisfied in the three presented cases, although Machine 2 is the closest one to the 5% limit. No restrictions were imposed regarding the torque

Table 2.4. Results from FE analysis for the three machines operating at 25000 rpm.

Parameter	**Machine 1**	**Machine 2**	**Machine 3**
BEMF THD	$< 1\%$	3.71 %	1.6 %
Phase current	111 A (rms)	114.3 A (rms)	42.55 A (rms)
Phase advance	0 deg (i.e. $i_d = 0$)	74 deg	0 deg (i.e. $i_d = 0$)
L_d	0.1532 mH	0.192 mH	0.48 mH
L_q	0.1532 mH	0.446 mH	0.48 mH
Torque constant	0.07352 Nm/A	0.07515 Nm/A	0.2064 Nm/A
BEMF constant	0.0848 V_s/rad	0.1831 V_s/rad	0.2392 V_s/rad
Fundamental freq.	416.7 Hz	833.3 Hz	833.3 Hz
Shaft torque	11.472 Nm	11.88 Nm	12.3 Nm
Torque ripple	0.1 %	7.62 %	1.5 %
Mechanical power	30 kW	31.1 kW	32.2 kW
Total losses	847.44 W	1197 W	772 W
Efficiency (at full load)	97.3 %	96.3 %	97.66 %
Power factor	0.9	0.858	0.92

ripple. However, it is interesting to note the elevated ripple level generated by Machine 2. This is mainly caused by the difficulties, from the manufacturing point of view, of skewing an interior PM rotor. The CSI-fed machine features an outstanding power density increment. In fact, the availability of a higher per-phase voltage provided by the CSI converter, with respect to the VSI one, gives more flexibility in the slot/pole combination choice, as well as in the winding layout selection. For the sake of fairness, from the theoretical point of view, the VSI topology with no flux weakening (i.e. Machine 1) could achieve the same power density level of Machine 3. Nonetheless, it would require a particular winding arrangement with two turns per coil and more than thirty parallel strands. It is then clear that such a design choice is not in line with the "design for manufacturability" approach as, generally, 10 to 15 parallel strands are the maximum practical limit for standard random wound EMs. Furthermore, an elevated number of parallel strands, combined with the relatively high speed of the PMSM might cause non-uniform current distribution in the wire

bundles [55]. This, in turn, originates localised hot-spot winding temperature, which might shorten the interturn insulation lifetime and bring reliability issues. The three machines are apprised in terms of mechanical and thermal performances. It is worth remarking that the stator hot-spot temperature, for the three designs, is within the range 150 °C +/- 10 °C. Nonetheless, Machine 2 is characterised by the highest rotor hot-spot temperature (i.e. 140 °C) among the solutions, since high order harmonics in the airgap magnetic field are source of eddy current losses in the PMs. The rotor stress analysis is computed via 3D FE structural simulations performed in Ansys® Workbench. The reported stress is normalised with respect to the maximum (yield) strength of the materials (i.e. retaining sleeve for Machines 1 and 3 and lamination for Machine 2).The first critical speed of the three rotors is analytically-calculated assuming the shaft as a supported beam, providing thus a conservative result [49]. For all the three designs, the operating speed (i.e. 25000 rpm) is well below the critical speed. Further, thanks to the low aspect ratio of Machine 3 (i.e. CSI-fed), its critical speed is c.a. 120000 rpm (i.e. more than four times the rated speed). Finally, the active weigh (i.e. excluding passive components such as housing and shaft) of the three solutions are evaluated. It is easily observable that the CSI-fed machine weights less than the other two prototypes, followed by the VSI-fed machine with no field weakening. Machines 2 and 3 require less PM material with respect to Machine 1, representing then the most cost-effective designs. Further, it is interesting to observe that the retaining sleeve, which as mentioned is an essential component in high-speed surface mounted PMSMs, represents only the 1% of the total weight (for Machines 1 and 3), due to the low mass density featured by carbon fiber.

Chapter 3

DC Link Current Control for a Single-Stage CSI in Sensorless Motor Drive Application

This chapter present a DC Link current Control that allow to use the CSI with a DC voltage source and a DC input inductor without the use of pre-stage DC-DC converter controlling the DC Link Current for the CSI. This work therefore seeks to challenge this 'accepted' consideration remove this circuit by proposing a new i_{dc} Current Control scheme. Stability analysis of small - signal model is considered through Nyquist criterion with the robustness in presence of variations of the most important system parameters. This control scheme can be applied for all the applications in which the electric machine has to work for almost all the time at high speed, i.e. pumps, compressors. The main perceived limitations of the proposed scheme are the low speed issue. This is due to the fact the CSI can work only as boost converter and for this reason is impossible to apply output voltages lower than V_{dc} and the fact that due to the uni-directional characteristic of the CSI, regeneration is not possible.

3.1 State of the art of CSI drives

Various solutions to control the input current (I_{dc}) have been proposed in literature [1–3], with most of them revolving around the concept of cancellation and addressing of the harmonic content of the input current. A simple but elegant solution, which is actually the most classical one, for an induction machine (IM) drive is proposed in [1]. The general schematic is shown in Fig. 3.1, which comprises two inverter stages, where the fist one is a Current Source Rectifier (CSR) that actively controls the I_{DC} current. The second stage is a six-device PWM-CSI. This setup relies on selective harmonic elimination processes that select the commutation instants of the PE devices to achieve the total rejection of a specific number of lower order harmonics. This is particularly suitable for systems working with low switching frequency and allows to reduce the power losses on the devices at the same time offering an acceptable power quality. In Fig. 3.1, it can be observed how the CSR stage considers the voltage across the input capacitance C_{in}, the current across the input inductance (L_{DC} in Fig. 3.1) and the voltage\current on the motor. A flux optimization algorithm is developed in this work, allowing to reduce the the DC Current in High power motor drive application with a CSR pre-stage. In this solution, due to the presence of CSR, the number of components compared to the CSI is greatly increased.

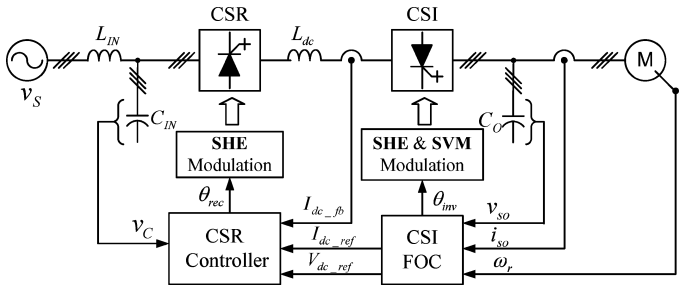


Figure 3.1. Back-to-back Current Source converter motor drive [1]

Another methodology for the implementation of a CSI drive is proposed in [2]. The general schematic is shown in Fig. 3.2, where it can be observed how the front-end of the CSI is implemented with a buck converter for the DC input voltage. In this case, a brushless DC (BLDC) drive is considered and it also includes a position sensorless control scheme. Here, the line-to-line voltages are measured to get the information of the back electromotive forces and a low-pass filter is necessary to guarantee the correct control. This information is afterwards used for the gate signal generation. The value of bus current I_d depends of the current reference I_d^*. This value is calculated by the speed loop and represents the desired current on BLDC. The reference I_d^* is compared to the I_d value and fed to the current loop, that regulates I_d. This solution allows implementing a sensorless control for BDCM with a buck-type CSI, but the number of components is high due to the presence of a buck pre-stage. This also decreases the efficiency due to the additional conversion stage.

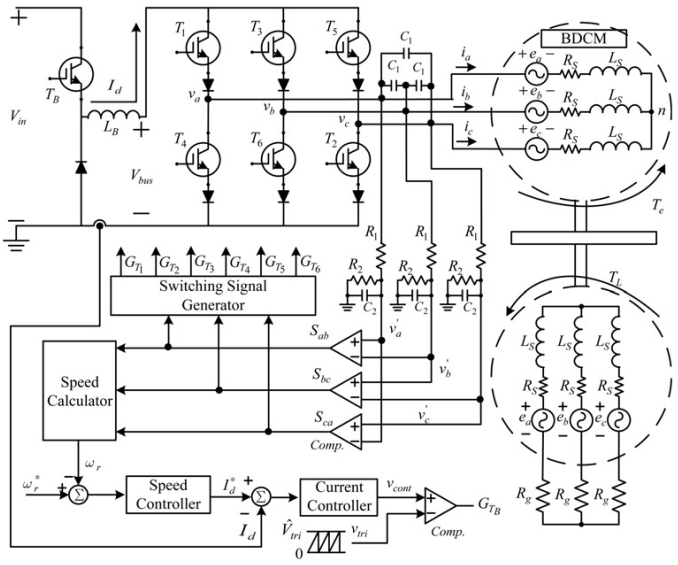


Figure 3.2. CSI with Buck-converter input converter [2]

The topology shown in Fig.3.3 was proposed and investigated in [3]. This configuration implements the null state when the device SWO is switched on . Depending on the duration of on-state T_{on} of SWO switch, the system behaves as a boost converter if the ($T_{on} > 0.5T$) (were T represent the period) as a buck Converter if ($T_{on} < 0.5T$). For this reason this topology is called "Buck-Boost Current source inverter".

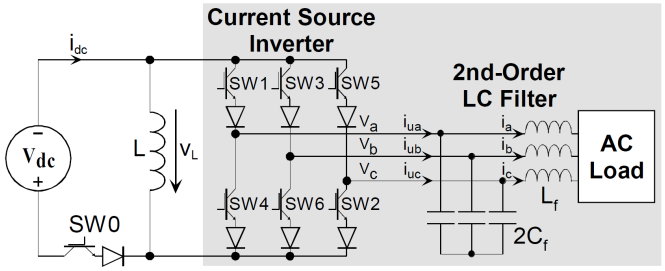


Figure 3.3. CSI with Buck-boost input converter [3]

A variation on the scheme of Fig.3.3 is the circuit shown in Fig.3.4 which was also proposed in [3]. This configuration implements the null state when the SWO is switched on and is called a single-ended primary-inductance converter (SEPIC). The front-end of this topology is similar to an unidirectional buck-

boost converter. The series capacitor C_1 carries the total energy flow from the input to the output. Similar to the circuit shown in the Fig.3.3, this circuit behaves as a boost converter if the ($T_{on} > 0.5T$) and as buck converter if the ($T_{on} < 0.5T$). In Fig.3.3 and Fig.3.4 two different ways to implement a DC current control with a Buck-Boost and SEPIC converter as pre-stage are shown. The state sequence modulating of buck-boost and SEPIC-derived it is divided into three states: null, active and inductive charging. A certain proportion of this states must be respected, to prevent a non-minimum-phase response [3]. The variation of the null state is used to increase the dynamic response of the system by decreasing the system voltage gain, reducing the operating range of the drive.

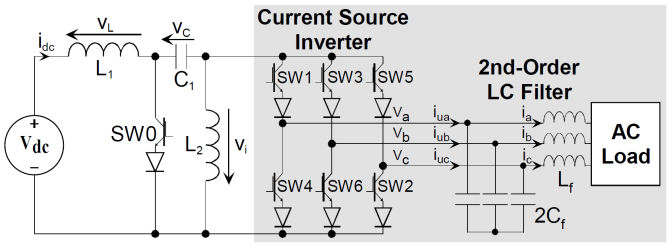


Figure 3.4. CSI with SEPIC input converter [3]

3.2 CSI drives: the way forward

All the above solutions have been shown to achieve the required operation of a CSI, however as mentioned above, they all depend on a reliable and appropriate and constant current source. Therefore they are all dependent on an additional pre-condition stage or front-end converter. This represents one of the main drawbacks of CSIs as this automatically adds weight and complexity to the whole system.

In this work, a solution that does not require an additional front-end converter is therefore proposed. The concept is based on an advanced dynamic control strategy that acts upon and modifies the space vector modulation, in particular

Table 3.1. Additional Switches\Components count

Topology	$N°$ Switches	Add. Comp	Series Switches
CSR [1]	6	0	4
Buck [2]	1	Diode	5
Buck-Boost [3]	1	Diode	5
SEPIC [3]	1	Diode, Ind., Cap.	5
CSI7 (proposed)	0	0	2

the modulation index (m) computation. To investigate the proposed methodology a typical VSD with a CSI configuration as that used in [56] is considered. This choice is based on the topology's ability to reduce the conduction losses, as the zero-state is implemented only with the 7° switch (S_7) and one diode, as shown in Figure 3.5.

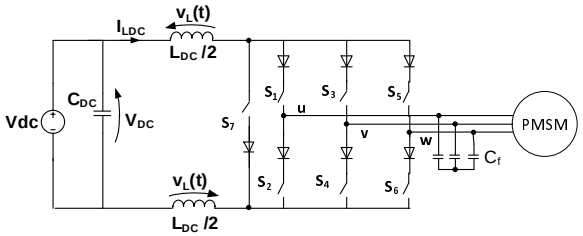


Figure 3.5. Schematic of CSI7.

An extra perceived advantage of the proposed configuration is its significantly lower component count. This can be clearly observed in Table 3.1, which compiles the number of passive components and semiconductor devices required by the proposed solutions and compares them to those of the more-known topologies described above. This clearly indicates the worth of the proposed scheme. The proposed control can be applied to the classic CSI topology and to CSI7 topology (with the seventh device), because the control schematic depends on SVM and not on the type of CSI. In the following, only the CSI7 topology will be considered due to its superior performance.

3.2.1 Sensorless algorithm

As mentioned before, to improve the robustness of the drive and remove the requirement of the speed sensor, a sensorless control will be used. It will be shown in the following how the peculiar characteristics of the CSI make it suitable for the implementation of this kind of control. The scheme considered comprises a PMSM, as shown in Fig. 3.5. It is well-known that the most common sensorless algorithms for PMSM can be divided into model based and high-frequency signal injection. Among the model based sensorless techniques, several solutions have been proposed: flux observers [57], back-emf observer, sliding mode controllers [58], Kalman Filters [59].

A characteristic of the CSI converter is the presence of the capacitive output filter. This strongly reduces the voltage distortion at the machine terminal, thus making a direct measurement possible. With a VSI, in order to measure the motor terminals, either a low-pass filter is needed to filter out the PWM harmonics or an estimation from the duty cycle can be used. Both solutions have drawbacks, including the fact that the filter is effective only if the ratio between switching frequency and fundamental frequency is high enough, otherwise a delay is introduced. The usage of the duty cycle demand as the information of the motor terminals is subject to strong assumptions, since the voltage drop and the PWM delay are neglected.

The direct measurement of the motor terminals with voltage sensors or resistive dividers allows for a fast and precise estimation of the equivalent voltage phasor. A Phase Locked Loop (PLL) can be used to this aim. If two phase voltages are measured, a standard three-phase PLL [60] with very fast dynamic response can be developed. The advantage of a direct estimation of the voltage terminal phasor is that a very wide bandwidth can be obtained, as there are no integral operations required to evaluate the flux.

However, the terminal voltage phasor differs from the back-emf one because

of the voltage drop across the phase resistance and inductance. A possible solution to this issue would be to subtract the resistive and inductive drops from the terminal voltage before they are fed into the PLL. However, calculating the derivative of the motor current would bring unacceptable issues in terms of noise.

A better solution is a feed-forward compensation of the voltage drops, by using the phasor equations. In fact, by using the terminal voltage angle, a first Park transformation can be performed on the phase current in order to calculate the direct and quadrature component of the motor current in this first reference frame. Fig. 3.6 shows the terminal voltage phasor along with the d and q component of the current and the voltage drops. The phase back-emf can be simply computed as shown in eq. 3.2.1.

$$E_{fx} = V_{fx} - RI_{fx} - j\omega LI_{fx} \tag{3.2.1}$$

From Figure 15, the angle error between the back-emf phasor and the terminal voltage can be calculated through the relationship described in (3.2.2). In the the case of a PM machine with an anisotropic rotor, the equations need to be changed to account for the difference in the inductance. However, it is worth noticing that the angle compensation can be neglected if the impedance of the machine is small. In this case, there is no longer the need to perform an inverse tangent operation in real-time.

$$\theta_{comp} = \arctan\left(\frac{\omega_e LI_{d,v} + RI_{d,v}}{|V_f| - RI_{d,v} + \omega_e LI_{q,v}}\right) \tag{3.2.2}$$

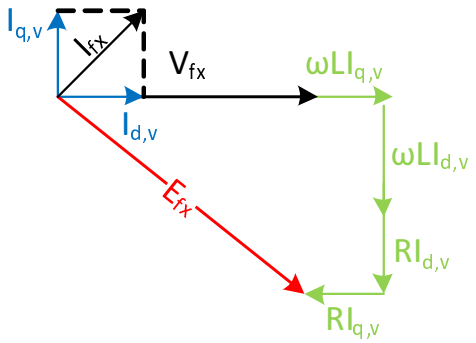


Figure 3.6. Phasor diagram of the terminal voltage with the resistive and inductive voltage drops.

Fig. 3.7 shows the overall block scheme of the PLL with angle compensation. This angle can therefore be used as the reference angle for the current control. A phase displacement of 90 ° is added to the PLL angle to re-synchronize with the most common field oriented control scheme, where the quadrature current is proportional to the torque.

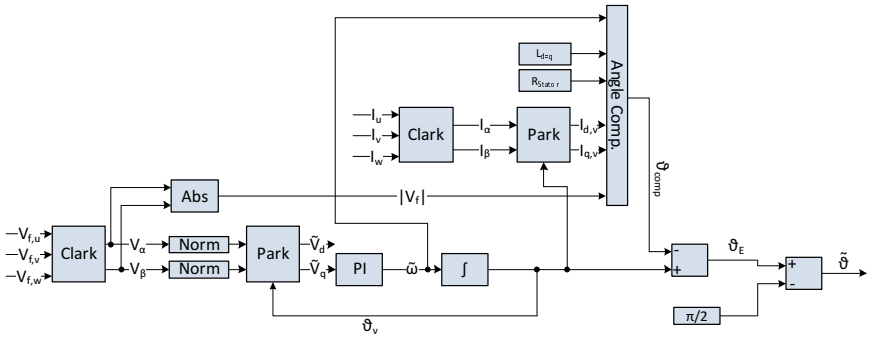


Figure 3.7. PLL structure with angle compensation

3.3 Proposed Control Strategy

In this section, the proposed control strategy is introduced. For this work, the structure of the platform being considered is similar to the scheme given in Fig. 1. The control strategy is based on classical Field Oriented Control (FOC), where the novelty is highlighted in the red box in Figure 3.8.

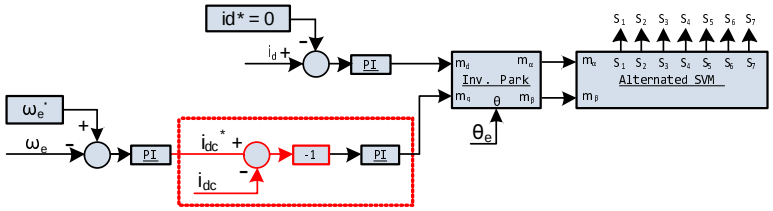


Figure 3.8. Proposed control strategy with i_{dc} current control of a PMSM without front-end converter stage.

In most applications requiring VSDs, a stable bus current is not available. However, in transport applications, DC voltage distribution systems are almost always available [61,62]. Considering all this, then the proposed control scheme can be developed as follows. Firstly, m is defined as $\sqrt{m_d^2 + m_q^2}$ where m_d and m_q values represent the dq motor current components normalized with respect to the DC Link current. After an inverse Park transformation, the normalized m_α and m_β currents components are computed. Thus, the Alternated SVM (ASVM, analised in detail in the first chapter) for a CSI is used to determine the interval times of the required active and zero vectors with the calculation of the modulation index m.

This results in a control scheme that removes the need of a front-end converter stage. This is shown in Fig. 3.8 which supplies the required i_{dc} current. As can be observed, the whole concept is based on the CSI working in boost operation.

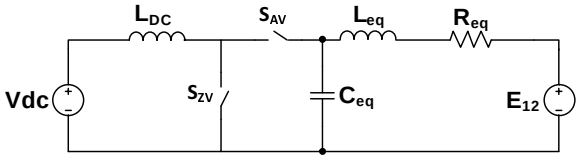


Figure 3.9. Equivalent circuit of CSI converter during the application of the Zero Vector and one of the Active Vectors.

Regulation takes place through a new closed loop control on the i_{dc} current. Considering the similarity between a CSI's behaviour and a Synchronous-Boost converter, such as the one shown in Fig. 3.9, then it can be said that the L_{eq}, R_{eq} and E_{12} represent the equivalent circuit of the machine during the

application of one of the Active Vectors. The zero vector is implemented with S_{ZV} and the active vector with S_{AV}. In fact, the higher output current/power can be transferred with higher values of t_z, i.e. the duty cycle of this equivalent boost converter. For this reason in Fig. 3.8 there is the inversion of the i_{dc} current loop sign.

Eq. (1.1.1) shows the relation between i_{dc} current and output current $|i_{ref}|$ under the hypothesis that i_{dc} current is in Continuous Conduction Mode (CCM). The CCM condition is the fundamental property that guarantees the stability analysis provided in the next section.

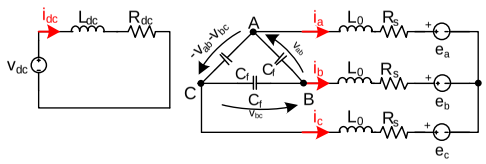
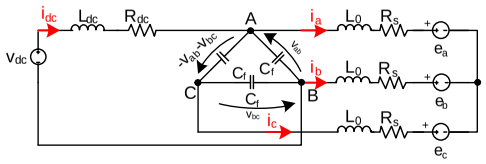
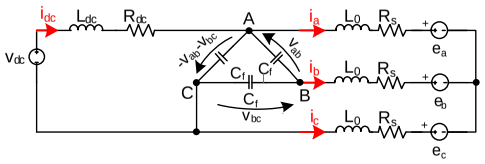
When a CSI is used in motor drive application, the output filter swaps reactive power with the motor. To reduce this effect an additional control loop on the i_d current is implemented to exchange reactive power with the inverter.

The external loop is closed on the electrical speed ω_e. The output of the regulation between the reference $\omega_e^\star$ and ω_e measured represents the reference $i_{dc}^\star$ value. The times of the active and zero states are calculated with (**??**). This control thus determines the i_{dc} value in relation to the load.

The proposed control allows to manage the i_{dc} imposing CCM operations without the use of a front-end converter regulating this current. Without the use of the additional front-end converter there is an intrinsic bond determined by the input-output voltage relationship of the boost converter.

This load-adaptive control of the inductor current effectively reduces the losses at partial load respect to the use of a front-end converter regulating constant DC current. This will be shown through simulations in Section 3.5.

Table 3.2. State space equations of the CSI for one sector under CCM condition

$z : 0 \leq t < t_z$	$a : t_z \leq t < t_z + t_a$	$b : t_z + t_a \leq t < T_s$
		
$\dot{x}_z = A_z x + B_z u$	$\dot{x}_a = A_a x + B_a u$	$\dot{x}_b = A_b x + B_b u$
$A_c = \begin{bmatrix} -\frac{R_{dc}}{L_{dc}} & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -\frac{1}{3C_f} & \frac{1}{3C_f} \\ 0 & 0 & 0 & -\frac{1}{3C_f} & -\frac{2}{3C_f} \\ 0 & \frac{2}{3L_0} & \frac{1}{3L_0} & -\frac{R_s}{L_0} & 0 \\ 0 & -\frac{1}{3L_0} & \frac{1}{3L_0} & 0 & -\frac{R_s}{L_0} \end{bmatrix}$	$A_a = \begin{bmatrix} -\frac{R_{dc}}{L_{dc}} & -\frac{1}{L_{dc}} & 0 & 0 & 0 \\ \frac{2}{3C_f} & 0 & 0 & -\frac{1}{3C_f} & \frac{1}{3C_f} \\ -\frac{1}{3C_f} & 0 & 0 & -\frac{1}{3C_f} & -\frac{2}{3C_f} \\ 0 & \frac{2}{3L_0} & \frac{1}{3L_0} & -\frac{R_s}{L_0} & 0 \\ 0 & -\frac{1}{3L_0} & \frac{1}{3L_0} & 0 & -\frac{R_s}{L_0} \end{bmatrix}$	$A_b = \begin{bmatrix} -\frac{R_{dc}}{L_{dc}} & -\frac{1}{L_{dc}} & -\frac{1}{L_{dc}} & 0 & 0 \\ \frac{1}{3C_f} & 0 & 0 & -\frac{1}{3C_f} & \frac{1}{3C_f} \\ \frac{1}{3C_f} & 0 & 0 & -\frac{1}{3C_f} & -\frac{2}{3C_f} \\ 0 & \frac{2}{3L_0} & \frac{1}{3L_0} & -\frac{R_s}{L_0} & 0 \\ 0 & -\frac{1}{3L_0} & \frac{1}{3L_0} & 0 & -\frac{R_s}{L_0} \end{bmatrix}$
$x = \begin{bmatrix} i_{dc} \\ v_{ab} \\ v_{bc} \\ i_a \\ i_b \end{bmatrix}, \quad B = B_z = B_a = B_b = \begin{bmatrix} \frac{1}{L_{dc}} & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & -\frac{1}{L_0} & 0 \\ 0 & 0 & -\frac{1}{L_0} \end{bmatrix}, \quad u = \begin{bmatrix} v_{dc} \\ e_a \\ e_b \end{bmatrix}, \; T_s = t_z + t_a + t_b.$		

3.4 Stability analysis and robustness

Stability analyses of the CSI converter is addressed following the processes in [63] for a phasor-PWM-based CSI connected to a resistive–inductive load and in [64] for a single phase CSI. In Table 3.2 L_{dc} and R_{dc} represent the DC-link inductor and resistor, C_f represents the ac-side filter capacitor, i_{dc}, v_{dc}, i_a, i_b, v_{ab} and v_{bc} represent the DC-link current and voltage, inverter-side current and voltage, respectively. Considering the schemes shown in Table 1 and using the average method [65], [66], the large signal model can be derived for one sector. The state vector x is given by $\left[i_{dc}, v_{ab}, v_{bc}, i_a, i_b\right]^T$, because v_{ca} and i_c can be written in terms of v_{ab}, v_{bc} and i_a, i_b, respectively.

The back emf terms e_a, e_b and e_c (remembering that $e_c = -e_a - e_b$) are considered as inputs of the system.

There are six distinct state space models, one for each sector (see Fig. **??**), but the averaged matrices obtained for all the sectors in the *dq*-reference frame are the same [63] so it is enough to consider only a single sector of the modulation. In the following subsections the large signal and the small signal models are derived in *dq* reference frame. To study the stability of the linearised model, the small signal model is studied in an equilibrium point x_e, i.e. $\dot{x} = f(x_e, u_e) = 0$.

3.4.1 Large-signal model

The average representation of state matrix A in three phase for a CSI feeding a PMSM results in:

$$\begin{aligned}\overline{A} &= \left[d_z A_z + d_a A_a + d_b A_b\right] \\ &= \begin{bmatrix} -\frac{R_{dc}}{L_{dc}} - \frac{2\sqrt{3}}{3L_{dc}}m - \frac{\sqrt{3}}{3L_{dc}}m & 0 & 0 \\ \frac{\sqrt{3}}{3C_f}m & 0 & 0 & -\frac{1}{3C_f} & \frac{1}{3C_f} \\ 0 & 0 & 0 & -\frac{1}{3C_f} - \frac{2}{3C_f} \\ 0 & \frac{2}{3L_0} & \frac{1}{3L_0} & -\frac{R_s}{L_0} & 0 \\ 0 & -\frac{1}{3L_0} & \frac{1}{3L_0} & 0 & -\frac{R_s}{L_0} \end{bmatrix}\end{aligned} \tag{3.4.1}$$

and in the dq rotating frame (obtained using Clarke and Park transformation) the average model can be written as

$$\begin{aligned}\frac{d}{dt}\begin{bmatrix} i_{dc} \\ v_d \\ v_q \\ i_d \\ i_q \end{bmatrix} &= \begin{bmatrix} -\frac{R_{dc}}{L_{dc}} - \frac{\sqrt{3}}{2L_{dc}}m - \frac{1}{2L_{dc}}m & 0 & 0 \\ \frac{\sqrt{3}}{3C_f}m & 0 & \omega_e & -\frac{1}{2C_f} & \frac{\sqrt{3}}{6C_f} \\ \frac{1}{3C_f}m & -\omega_e & 0 & -\frac{\sqrt{3}}{6C_f} - \frac{1}{2C_f} \\ 0 & \frac{1}{2L_0} & \frac{\sqrt{3}}{6L_0} & -\frac{R_s}{L_0} & 0 \\ 0 & -\frac{\sqrt{3}}{6L_0} & \frac{1}{2L_0} & 0 & -\frac{R_s}{L_0} \end{bmatrix}\begin{bmatrix} i_{dc} \\ v_d \\ v_q \\ i_d \\ i_q \end{bmatrix} \\ &+ \begin{bmatrix} \frac{1}{L_{dc}} & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & -\frac{1}{L_0} & 0 \\ 0 & 0 & -\frac{1}{L_0} \end{bmatrix}\begin{bmatrix} v_{dc} \\ e_d \\ e_q \end{bmatrix}\end{aligned} \tag{3.4.2}$$

3.4.2 Small-signal model

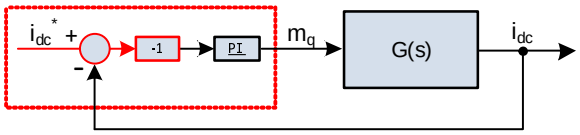


Figure 3.10. Control scheme considered for the stability of the equilibrium point.

In this Section, the small-signal model of the three-phase CSI connected to a PMSM is derived.

In (3.4.2) v_{dc} represents the system input for constant values of m and ω, but in practice, m is used to regulate the output of the current source inverter. This results in the large signal model (3.4.2) to be linearized around a steady-state operating point by defining small perturbations as $x_{dq} = X_{dq} + \delta x_{dq}$, $v_{dc} = V_{dc} + \delta v_{dc}$, $m = M + \delta m$ and $\omega_e = \Omega_e + \delta\omega_e$.

Also, the back emf terms e_d and e_q are substituted by $L_0\omega_e i_q$ and $-L_0\omega_e i_d - \omega_e\lambda_{PM}$. The resulting linearized small-signal model is therefore as given by (6).

$$\frac{d}{dt}\begin{bmatrix}\delta i_{dc}\\ \delta v_d\\ \delta v_q\\ \delta i_d\\ \delta i_q\end{bmatrix} = \begin{bmatrix} -\frac{R_{dc}}{L_{dc}} & -\frac{\sqrt{3}}{2L_{dc}}M & -\frac{1}{2L_{dc}}M & 0 & 0\\ \frac{\sqrt{3}}{3C_f}M & 0 & \Omega_e & -\frac{1}{2C_f} & \frac{\sqrt{3}}{6C_f}\\ \frac{1}{3C_f}M & -\Omega_e & 0 & -\frac{\sqrt{3}}{6C_f} & -\frac{1}{2C_f}\\ 0 & \frac{1}{2L_0} & \frac{\sqrt{3}}{6L_0} & -\frac{R_s}{L_0} & \Omega_e\\ 0 & -\frac{\sqrt{3}}{6L_0} & \frac{1}{2L_0} & -\Omega_e & -\frac{R_s}{L_0}\end{bmatrix}\begin{bmatrix}\delta i_{dc}\\ \delta v_d\\ \delta v_q\\ \delta i_d\\ \delta i_q\end{bmatrix} + \begin{bmatrix} \frac{1}{L_{dc}} & -\frac{\sqrt{3}}{2L_{dc}}V_d - \frac{1}{2L_{dc}}V_q & 0\\ 0 & \frac{\sqrt{3}}{3C_f}MI_{dc} & V_d\\ 0 & \frac{1}{3C_f}I_{dc} & -V_q\\ 0 & 0 & I_d\\ 0 & 0 & -I_q - \frac{\lambda_{PM}}{L_0}\end{bmatrix}\begin{bmatrix}\delta v_{dc}\\ \delta m\\ \delta\omega_e\end{bmatrix} \tag{3.4.3}$$

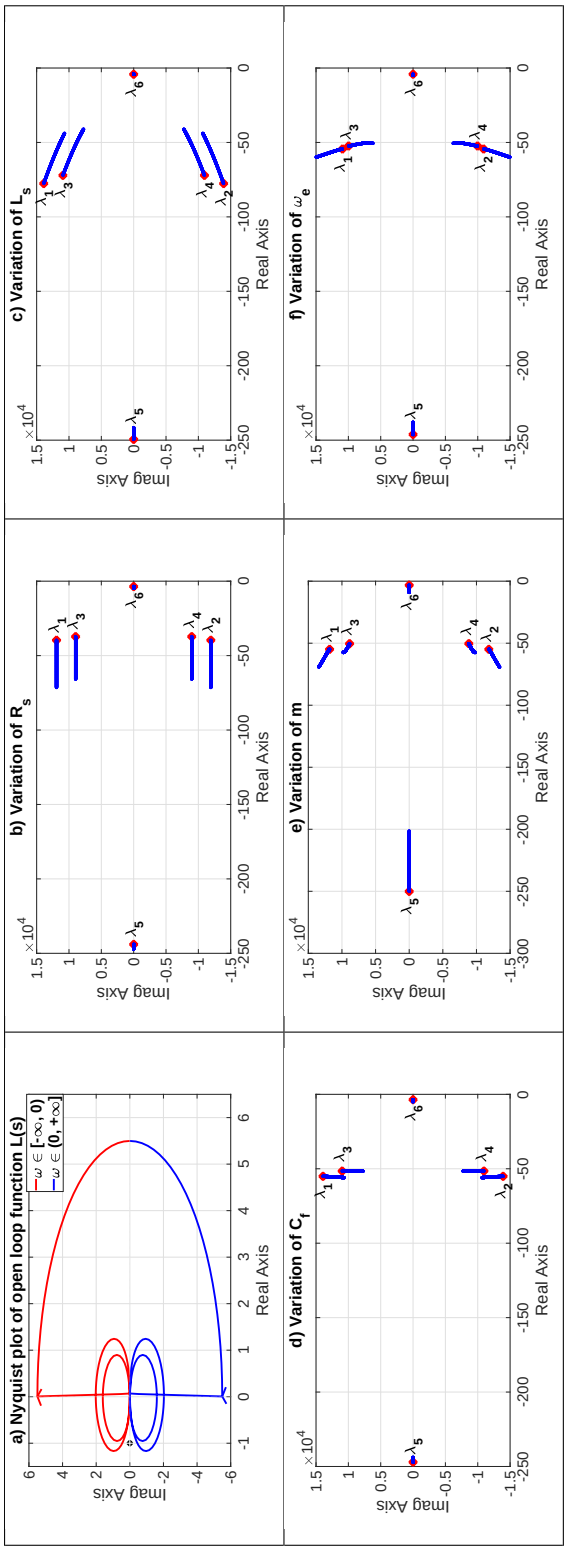


Figure 3.11. a) is the Nyquist plot of the open loop function $L(s)$. b), c), d) are the eigenvalues of the closed loop against variations of R_s, L_s and C_f between -30% and 30%. e), f) are the eigenvalues of m and ω_e between0.1 and $\sqrt{3}/2$ and 300 and 3000 rad/s, respectively. The red symbol represents the lower bound of each plot.

The closed loop control that regulates the error between the reference current $i_{dc}^{\star}$ and the measured i_{dc} with a proportional-integral controller which assure the regulation of the error (see Fig. 3.10), as presented above represent one of the main innovative outputs of this work. The stability proof is made by computing the transfer function $G(s)$ between the input δm and the output i_{dc}.

The open loop function $L(s)$ given by $PI(s)G(s)$ presents poles in the left half plane, i.e. $\mathbb{R}\mathrm{e}\{\lambda_i\} < 0$. This ensures the stability of the closed loop, as it is necessary that the Nyquist diagram of $L(s)$ presents no turns around the point -1. For the stability analysis the Nyquist criterion is preferred to a Bode diagram because the system passes the $0\,dB$ axe multiple times, so the stability isn't regular but conditional. All eigenvalues of the closed loop system are located in the left-half s-plane, indicating an asymptotically stable system. But this does not mean that the system is stable in presence of parameters change, so variation of the eigenvalues must be studied. As shown in Fig. (3.11) the system remains stable in case of perturbations on the parameters R_s, L_s, C_f, m and ω_e.

3.5 Simulation results

Table 3.3. Current Source Inverter Simulation Parameters

Name	Value	Unit
v_{dc}	270	V
i_{dcmax}	140	A
m_{qmax}	0.86	-
ω_{ref}	5150	rad/s
L_{dc}	2	mH
$T_{S-AltPWM}$	50	μs
T_{ov}	1	μs
C	6.6	μF

Table 3.4. PMSMs Electrical Parameters

Parameter	Value
Phase current (rms)	114.3 A
R_s	0.05 Ω
L_0	0.48 mH
k_M	0.2392 Vs/rad
Fundamental freq.	833.3 Hz
Torque ripple	5.48 %
Mechanical power	32.2 kW

To investigate the proposed concept, a full model of the CSI with the proposed current control is built in a Matlab/PLECS environment. The model architecture is shown in Fig.3.12. The main simulation parameters are reported in Table 3.3. A PMSM machine has been considered and its parameters are reported in Table 3.4. Because of the intrinsic boost capability of the CSI, a high-speed machine is used as a reference for the simulation analysis.

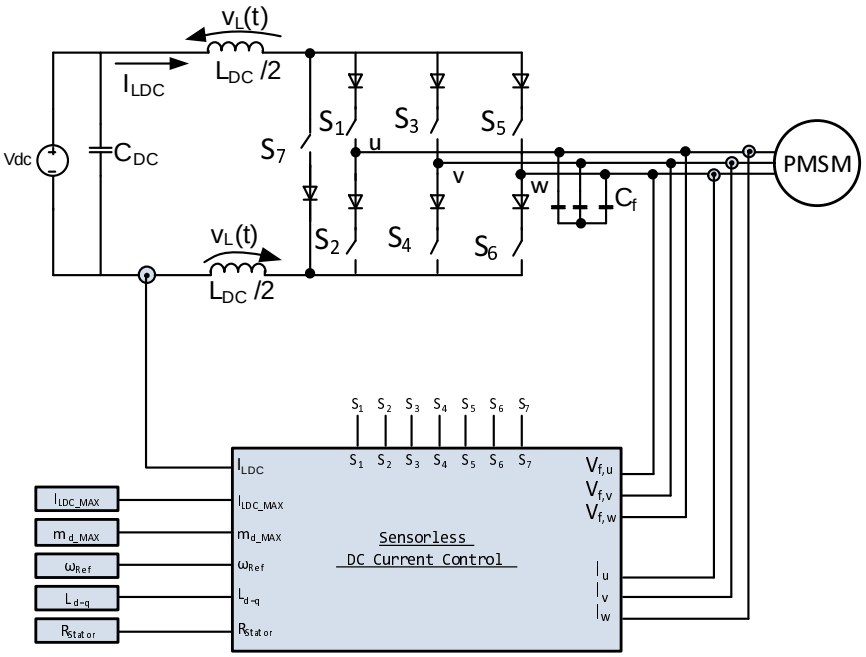


Figure 3.12. Schematic of the Simulation.

The proposed control is first tested with an incremental step condition. Fig.

3.13 plots the command condition and the ensuing results. It shows the reference and measured speed, the input current and the mechanical torque. From Fig. 3.13, the automatic adjustment of the i_{dc} current in relation with the increasing load, can be easily observed. A small speed disturbance visible as an overshoot can also be observed for every load increment. However, this overshoot is immediately regulated, similar to a first order exponential transient, thus highlighting the fast and robust nature of the proposed control scheme. For these simulation tests, the maximum i_{dc} is $i_{dcmax} = 140$ A.

From Fig. 3.13, it is also possible to observe that when the system is in overload condition (Load torque $T_L > 10$ Nm), the i_{dc} never exceeds the i_{dcmax} value. In overload condition, the speed decreases because the limit of the input current effectively acts as an electrical torque limiter, thus causing the motor speed to slow down. Fig. 3.14 shows the system operation during variable speed conditions. The reference and the measured speed are shown as well as the input current. The mechanical torque indicates a constant mechanical load. Due to controller saturation, the speed rises in a linear fashion; i.e. after reaching the target speed, due to the anti-windup implemented in the PI regulators, the current is well regulated to match the increased power condition.

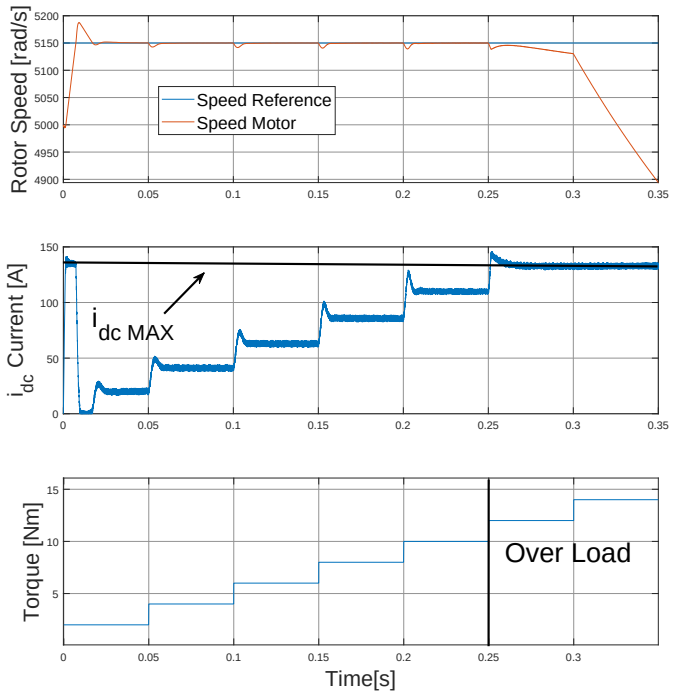


Figure 3.13. Simulation: current control in normal and over-load condition.

To fully understand the advantages of the proposed scheme, a detailed comparison of power losses between a CSI with a chopper front-end stage with a constant i_{dc} current and the CSI with the proposed current control has been done. Considering that losses are highly dependant on the type of switching device technology used, then the models for each configuration were first built with Silicon IGBTs and then also with SiC MOSFETs. Thus two sets of results are achieved from both the traditional and the proposed configurations. The results are compared in Fig.3.15. The choice between these two technologies are a consequence of the 1200V voltage rating. In fact, 1200V Silicon MOSFETs, with an acceptable on-state resistance, are today still not commercially available. If a lower voltage rating was acceptable, the solution of Si MOSFET optimized for conduction losses (i.e., CoolMos technology without fast recovery body diode) could also be considered. In fact, no reverse recovery of the

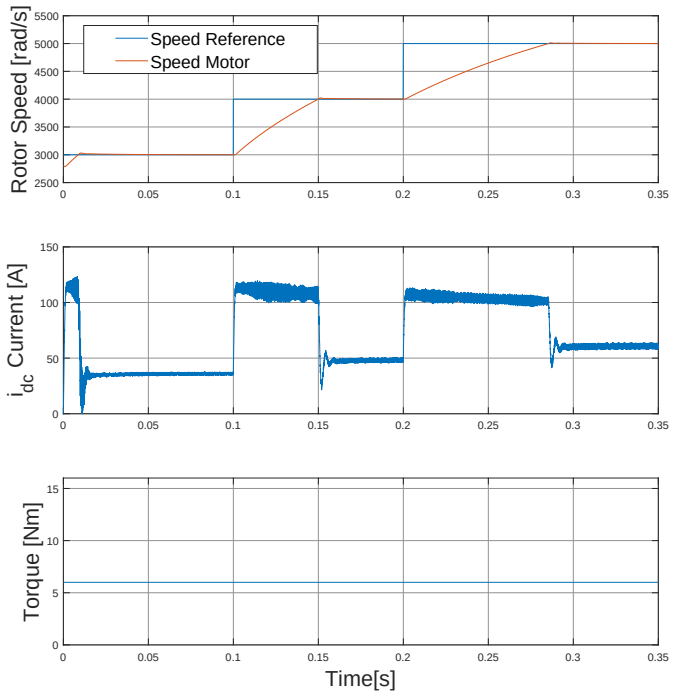


Figure 3.14. Simulation: current control at different speed references.

MOSFET body diode happens in the CSI topology. The configuration with i_{dc} Current control and SiC devices has the lowest power losses.

It should be noted, that the DC chopper would allow to operate the machine even when the back-emf is lower than the DC input voltage. The comparison of Fig. 3.15, therefore, is valid only when the operating speed of the machine is high enough so that the back-emf exceeds the input voltage.

3.6 Experimental results

To validate the proposed control scheme and thus prove that a CSI converter can be used without a pre-conditioning stage, a complete prototype of the CSI7 has been realized. The prototype system has been developed based on SiC devices, as used in the simulation section (Wolfspeed C2M0025120D). A

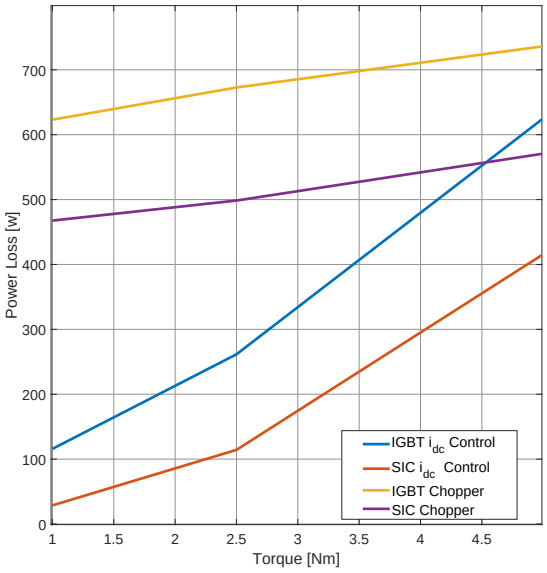


Figure 3.15. Total Power losses comparison between i_{dc} control and Chopper.

commercial TMS320F2812 digital signal controller that implements the modulation strategy and the control with a sampling and switching frequency of 10 kHz was used.

The PE is connected to a PMSM machine and a loading system as shown in Fig. 3.16. A machine on derated power and with limited speed is used, and an input voltage of 28 V as the DC bus is selected. A Digital to Analog Converter (DAC) is used to plot the internal variables of the DSP onto an oscilloscope.

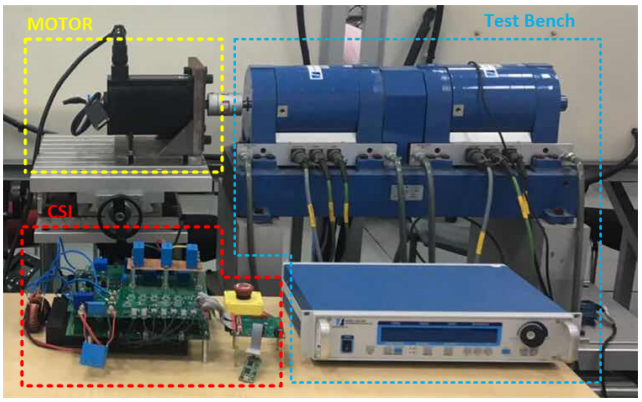


Figure 3.16. CSI7 Inverter prototype with SiC devices and Test Bench.

Having setup the prototype and its test bench, a series of experimental runs were designed aimed to prove the concept of the proposed scheme and also investigate its stability when various operating conditions are considered. The results from these tests are then compared against those achieved from the simulation model, where the same operating conditions as those in Section 3.5 are recreated experimentally.

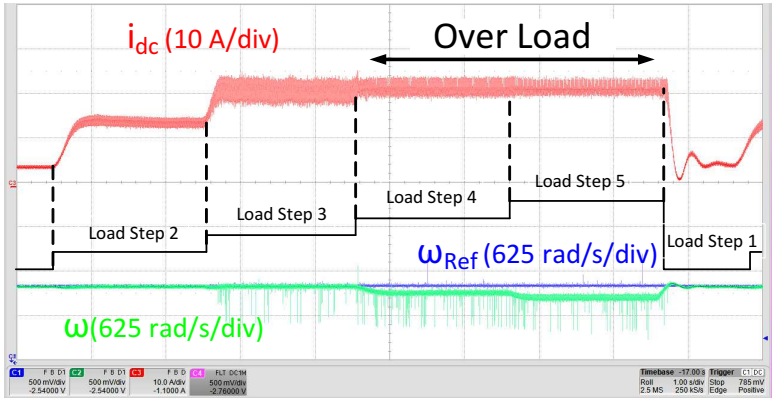


Figure 3.17. Experimental results: current control in normal and over-load condition.

Fig. 3.17 shows the relevant waveforms, when the CSI is driving the test machine at a constant speed. In this case, a load profile similar to Section 3.5 is generated with the load system. The matching to Fig. 3.13 is excellent. It can be observed that for an overload condition, the speed loop cannot track the reference anymore and the measured speed decreases following the mechanical dynamics. Spikes in the DAC channels are caused by disturbances in the measurement due to the switching devices and not by glitches of the control.

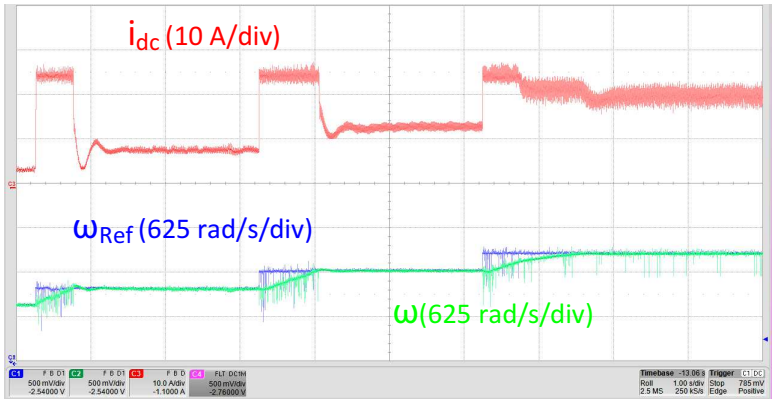


Figure 3.18. Experimental results: current control at different Speed references.

Fig. 3.18 repeats the same condition of Fig. 3.14 where a speed profile is generated. The maximum speed is limited to 2500 rpm due to the bearings of the test machine. It is possible to see that the control is adapting the input current to match the load condition. The maximum input current limits the acceleration, causing the speed to increase linearly.

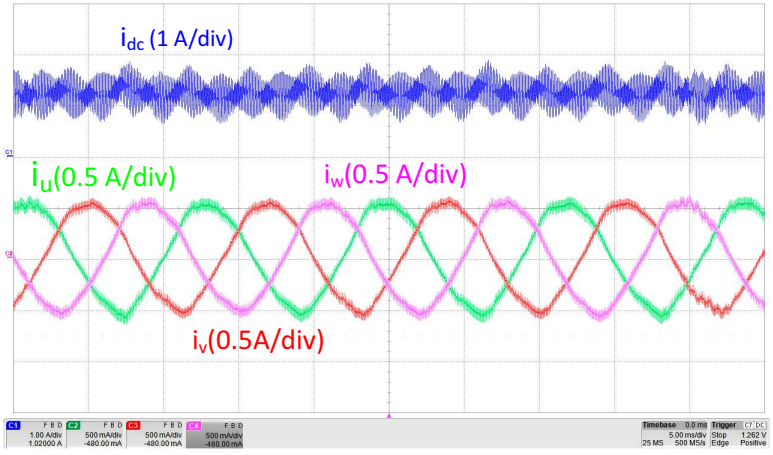


Figure 3.19. Experimental results: three phase currents and i_{dc} in steady - state.

Fig. 3.19 shows the three phase currents i_u, i_v and i_w with the DC Link current i_{dc} in steady - state condition.

All the simulation results and proof-of-concept experiments confirm that the

CSI drive can operate as a single-state solution with intrinsic voltage boost capability. Thus with this work, the historical main drawback or design challenge of CSI converters can be said to have been overcome. Having removed this drawback, then the inherent advantages of a CSI drive can be full exploited. These include:

1. A direct control on the input current of the inverter
2. A direct DC bus connection that allows for an intrinsic boost capability
3. The ability to remove the need for electrolytic capacitors on the DC Link, due to the continuous input current operation.
4. The reducing of dV/dt stresses on the machine windings as everything is current controlled

Apart from all the general advantages given above, in this work it has also been shown how a CSI without the front-end converter can be implemented with the aim of driving a PMSM machine with low power losses thanks to the reduced number of stages and the load-dependent control.

Chapter 4

Conclusion

This thesis has explored in the detail the potential of the Current Source Inverter topology applied to emerging topics in the power electronics industry. Obviously, this CSI is not the same as envisaged decades ago, but it relies on the new technologies as the wide bandgap semiconductors and high computational power of the processors that enable advanced modulation and control.The main achievement of this thesis is to break one of the common biases against the CSI: the low efficiency.

4.1 Conclusion on CSI for renewable energy

The Proposed CSI7 topologies allows for a strong reduction in the conduction losses and enables soft-switching operation of all the full-bridge devices, allowing to achieve very high efficiencies with a single-stage power converter. The topology finds its application especially in those areas where an intrinsic voltage boosting is envisaged, i.e., the renewable energy sources.
Considering the European scenario, with a predominance of small photovoltaic systems instead of small wind turbines, the work of this thesis is also well inserted into the industrial context. To this purpose, one of the main issues

of the small photovoltaic system is the ground leakage current that originates from the parasitic capacitance of the photovoltaic panels. A thorough study of the common-mode circuit of different CSI configurations allowed to state that the CSI7 topology with a modified output filter allows in a simple, lightweight and cost-effective way to strongly reduce the ground leakage current, making the CSI7 topology ready for an industrial utilization.

4.2 Conclusion on CSI in Motor Drive applications

The second part of the thesis has explored the usage of the CSI for motor drives application. Differently from the established state of the art, where the CSI is always used with a converter front-end that regulates the inductor current, this thesis proposes to use a single-stage CSI to control at the same time the output current and the inductor current. The advantages of such approach are the increase of efficiency due to a reduced number of conversion stages, and the improvement of power density and reliability as a consequence of the reduced component count. The challenge is that the modulation must be properly managed to keep the inductor current within the operational limit while performing the main task of the motor current control. A modified control scheme was therefore proposed, showing that a single-stage CSI variable speed drive is possible as long as the steady state value of the motor back electromotive forces is higher than the DC link voltage. In fact, the CSI still behaves as a boost converter.

Further exploring the joint design of converter and electric machine, the last part of the thesis addresses a high-speed drives for aerospace applications. Several designs for different combination of converter and machines are analyzed, and the result is that the CSI, thanks to its intrinsic voltage boost capabil-

ity, allows for the optimal design of the electric machine, making it the ideal candidate for high-power density high-speed applications. The main aim of this second part of the thesis was to prove how a PEC technology that has always been "brushed off" by the electric drives community, in some particular applications, might represent the optimal design choice at system level. A technology that in the past had the voltage boosting as its only benefit can have his rebirth in a scenario where the higher voltage design of an electric machine implies benefits in the system power density. Obviously, the technology development that allows better devices with bidirectional voltage blocking capability and optimized topologies are concurrent factors that contributed to reduce the gap respect to VSI based solutions. Once the benefits at machine level are achieved, the other characteristic of low output voltage THD and dv/dt can make the CSI as the true winner, due to the lower stress on the machine and the absence of output filter. With an eye to the future of transportation electrification, in particular in the aerospace sector, it is necessary to "combine the efforts" between machines and power electronics designers for proposing efficient and optimised drive solutions. This work thus aims in "raising awareness" on how the converter choice can strongly influence various aspects of an electric machine design. The selected case-study is purposely chosen for further outlining that, when an integrated design is carried out, a system-level optimum can be achieved. For large commercial aircraft, it is still unthinkable to replace Jet-A fuel for propulsion purposes. Current energy-storage devices represent the main bottleneck, as their energy density is still c.a. ten times less than the (minimum) required level. Nonetheless, if electrical machines are to be adopted as primary power system (i.e. propulsion), their design is not going to be a trivial process. Within 10 to 15 years, electric motors for regional aircraft propulsion, will be demanded to develop 2-5 MW of power and to be controlled by power electronics converters. Among all the "conventional" de-

sign challenges, they will need to feature an outstanding reliability, as a single failure might be catastrophic. An even higher challenge is posed by the move towards "high-voltage" systems for aerospace (1-3 kV), as this will save considerable weight and increase range and/or payload capability. Nonetheless, the harsh aerospace environment (low pressure and wide temperature range) implies a physics of failure-oriented design for the whole electric drive, which is reached by introducing reliability aspects as primary design requirement.

4.3 Further research

The Further research directions that could stem from this thesis are:

1. Integration of the magnetic components into the PCB to realize more compact design (planar magnetics).

2. Critical reliability evaluation of the whole system composed of high-speed machine and power electronics, considering the lower voltage stress of the winding insulation.

3. Optimized controls of both machine and CSI to take the full advantage of the voltage boosting capabilities of the CSI.

4. New semiconductor technologies (normally-on GaN, reverse blocking GaN).

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