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On the Impact of OFF-State Stress on Dynamic R_{ON} of On-Wafer 100-V p-GaN HEMTs by Emulating Monolithically Integrated Half-Bridge Operation

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Abstract

This paper presents the electrical characterization of the on-resistance (R_{ON}) of on-wafer 100-V p-GaN power High-Electron Mobility Transistor (HEMTs). This study assesses device degradation in the context of a monolithically integrated half-bridge circuit, considering both Low-Side (LS) and High-Side (HS) configurations. Since on-wafer samples have been characterized, a custom experimental setup was developed to emulate stress conditions subjected by the devices in the half-bridge circuit. A periodic signal (T = 10 µs, T_{ON} = 2 µs) switching from the OFF- to ON-state was applied for a cumulative duration of 1000 s. Different OFF-state stress conditions were applied by varying the gate-source OFF voltage ($V_{GS,OFF}$) between 0 V and −10 V. The on-resistance exhibited a positive drift over time for devices in either LS and HS configuration, with the latter showing a more pronounced degradation. Measurements at higher temperatures (up to 90 °C) were carried out to characterize the dynamics of the physical mechanism behind the degradation effects. We identified hole emission from C-related acceptor traps in the buffer as the main mechanism for the observed degradation, which is present in both HS and LS configuration. The additional degradation observed in the HS case was attributed to the back-gating effect, stemming from the non-null body-to-source voltage. Furthermore, we found that a more negative $V_{GS,OFF}$ further increases R_{ON} degradation, likely related to the higher electric field near the gate contact that enhances hole emission from C-related acceptor traps.

Keywords: p-GaN HEMTs; OFF-state stress; dynamic R_{ON}; carbon doping; half-bridge

1. Introduction

The Gallium Nitride (GaN) High Electron Mobility Transistor (HEMT) is leading the next generation of power switches due to its high frequency and high power capability [1]. More specifically, GaN-on-Si is a particularly interesting platform thanks to its potential for monolithic integration [2]. Despite being already commercialized, GaN-on-Si power devices are still far from reaching their maximum theoretical performance due to, amongst other, trapping effects occurring during device operation [3]. So far device-level characterization has been extensively conducted, allowing for a deep understanding on

how the trapping mechanisms work in this type of devices [4], [5], [6], [7], [8], [9], [10], [11], [12], [13], [14]. However, trap dynamics characterization under realistic circuit operating conditions is far less investigated. For example, in monolithically-integrated half-bridge circuits, the High side (HS) and Low Side (LS) devices experience different degradation levels in terms of both on-resistance (R_{ON}) and threshold voltage (V_{TH}), due to the non-null source-to-body voltage present in HS device [15], [16], [17]. The goal of this paper is to analyze the effect of OFF-state stress on the device performance from the trapping point of view. We find that the core mechanism causing the dispersion of device performance is the hole emission from C-related acceptor traps inside the buffer layer. This mechanism is common for both HS and LS. The additional degradation experienced by the HS device is explained as being due to a purely electrostatic phenomenon due to the so-called back-gating effect. This conclusion is further confirmed by the fact that the time constants and the activation energies (E_A 's) extracted from the HS and LS transient are essentially the same. Moreover, we find that the negative OFF-state gate voltage enhances the degradation caused by the high drain voltage, and this effect can be explained with the accumulation of negative charges in the AlGaN barrier that deplete the 2-DEG (two dimensional electron gas), thus increasing the magnitude of the observed dispersion [18], [19].

The paper is organized as follow. In section II the custom experimental setup and the Device Under Test (DUT) are presented. In section III the experimental results are presented, along with a discussion about the physical interpretation of the findings. Section IV draws the conclusions.

2. Experimental Setup

Figure 1 shows the cross-section of the DUT, which is a 100-V p-GaN HEMT. The L_G is lower than 1 μm and the L_{GD} is lower than 3 μm, allowing a relatively low voltage range operation (for comparison, the 650-V p-GaN technology typically involves L_{GD} longer than 15 μm). As customary for GaN power HEMTs, the buffer is C-doped to obtain a semi-insulating layer with a C concentration between $5x10^{18}$ and $5x10^{19}$. The p-GaN region in the gate stack is used to deplete the 2-DEG under the gate at V_{GS} = 0 V and thus achieve normally-off operation, i.e., V_{TH} > 0 V. The circuit employed for the electrical characterization is shown in Figure 2. The drain voltage is supplied by a pair of isolated DC/DC converters that allow to generate a 50 V isolated voltage. The bulk of the device is connected either to ground or to the negative terminal of the V_D for emulating respectively the LS and HS configuration. The only difference between LS and HS is the source-to-body voltage that is 0 V for the LS, while in HS a non-null V_{SB} is present. This mimics the additional voltage stress experienced by the high side device of an integrated half-bridge structure. To improve the Digital Store Oscilloscope (DSO) resolution we use the clamping circuit shown in Figure 2(b). The clamping circuit allows the V_{DS} to be measured to rise as long as $V_{DS}<V_Z$. When V_{DS} reaches the level set by the Zener diode (~ 4 V), diodes D1 and D2 start to conduct and prevent V_{DS} from rising further. Effectively, the circuit clamps the maximum level of the V_{DS} measured by the DSO [20]. This circuit is required only for improving the resolution of the voltage signal measured by the DSO, while the DUT experiences the full 50-V signal as set by the DC/DC converters.

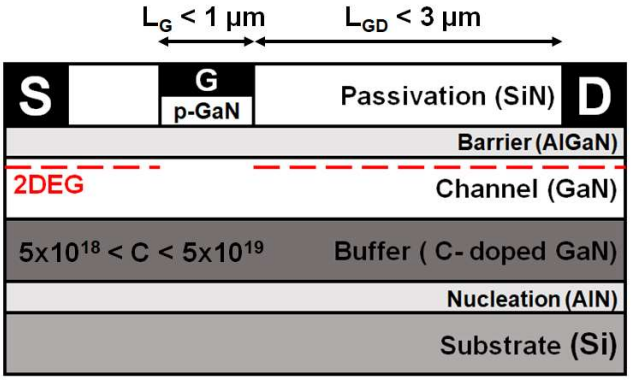


Figure 1. Schematic view of the cross section of the DUT. The p-GaN under the gate creates an effective 'p-i-n' junction towards the source, that depletes the 2DEG at V_{GS} = 0 V and thus allows a normally-off operation (i.e., V_T > 0 V). The Gate-Drain distance is such that the 100-V range operation can be withstood and the Carbon concentration in the buffer layer is between 5x10[18] and 5x10[19] to obtain a semi insulating layer.

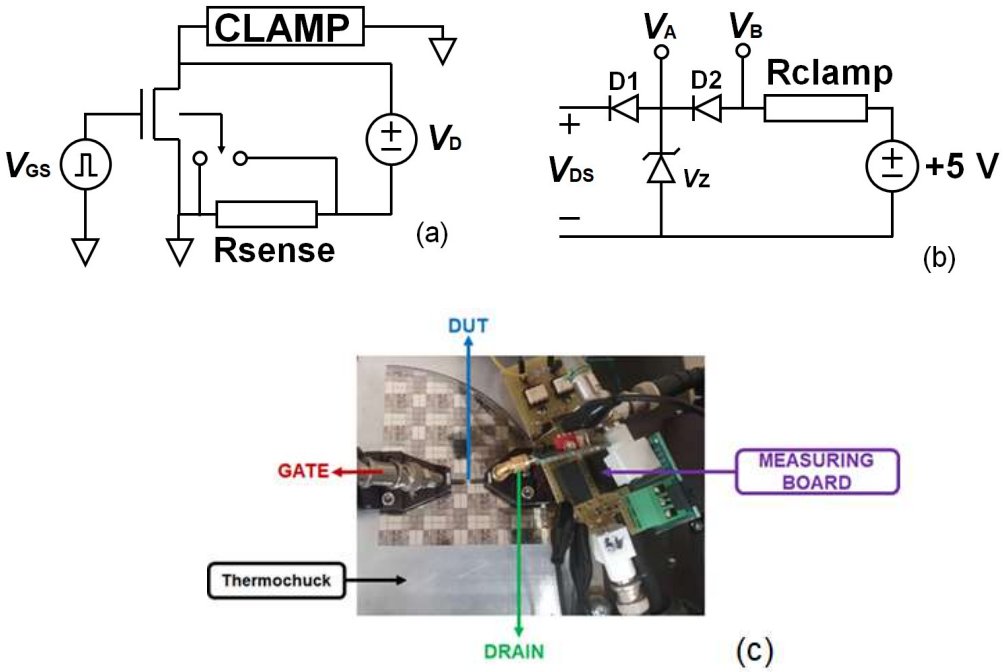


Figure 2. The measuring board (a) used for the measurement, V_D is provide by means of a DC/DC isolated converters. The switch is connected either to ground (LS) or to the negative pin of the V_D (HS). The clamping circuit (b) is used to block the rise of the V_{DS} to be able to have a more precise measure with the DSO. We calculate the real $V_{DS,ON}$ with the voltage V_A and V_B ($V_{DS,ON} = 2 \times V_A - V_B$). In panel c a picture of the measurement setup used in this paper is shown for reference.

The typical DC output (I_D-V_{DS}) and transfer (I_D,I_G-V_{GS}) characteristic are shown in Figure 3. From there curves we can extract the threshold voltage and the static on-resistance that are respectively $V_{TH} \approx 2$ V and $R_{ON} \approx 20$ Ω. More details on the contact resistance and the device structure can be found in [21].

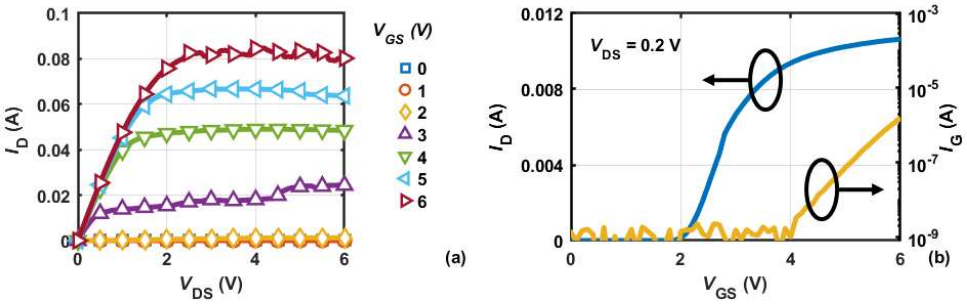


Figure 3. Typical output (a) and transfer (b) DC characteristics of the DUT. From these measurements we can extract the static value of the on-resistance (R_{ON} ≈ 20 Ω) and the threshold voltage (V_{TH} ≈ 2 V), respectively.

The gate of the DUT is driven with a pulsed signal from a waveform generator that switches the device between $V_{GS,ON}$ (6 V) and $V_{GS,OFF}$ (0;-2;-5;-8;-10 V). The drain voltage applied to the device is V_{DS} = 50 V during the OFF-state and ~ 200 mV during the ON-state, The $V_{DS,OFF}$ has been chosen as 50 V to ensure a test condition comparable with the real application of a GaN HEMTs (e.g. 48 V DC/DC converter). The switching period is T = 10 µs with a T_{ON} = 2 µs. The R_{ON} measure is performed by extracting the current during the ON-state. The total time taken by the experiment is 1000 s. Before the beginning of each measurement, the DUT is biased in the ON-state with low V_{DS} (~ 200 mV) and V_{SB} = 0 V for 100 s to guarantee a common stress-free initial condition for both LS and HS configuration. Figure 4 shows the first period of the stress cycle to illustrate the setup.

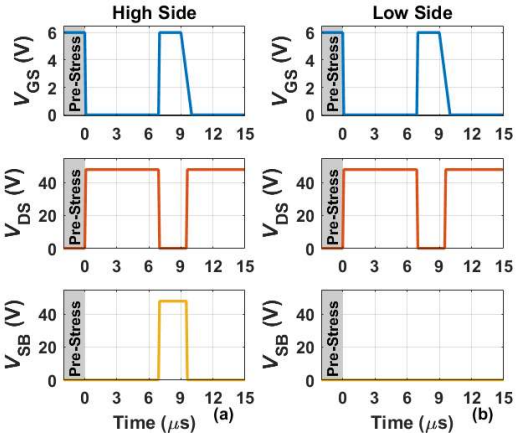


Figure 4. The first waveform of the stress period. In LS (b) the V_{DS} switch between high and low accordingly to the value of the V_{GS} and the V_{SB} is always zero, regardless of the device condition. In HS (a) the V_{DS} behave like in LS, but the V_{SB} goes high during the T_{ON}, giving an additional stress component.

3. Experimental Results

Figure 5 shows the normalized dynamic on-resistance ($R_{ON}/R_{ON,0}$) for $V_{GS,OFF}$ varying from 0 V to -10 V for both LS and HS. The $R_{ON,0}$ is taken as the measurement of the first stress pulse. The baseplate temperature for this experiment was set to 60 °C. We can see that for both HS and LS configuration increasing the negative $V_{GS,OFF}$ causes an increased magnitude of the degradation. More specifically, degradation increases from ~20 % at 0 V to ~55% at -10 V (LS) and from ~65 % at 0 V to ~120% at -10 V (HS). Interestingly, we find that while the OFF-state gate voltage has a significant effect on the magnitude of the degradation, it does not appear to have significant effect on the time constant of the transient. This is discussed further when presenting the data at different temperatures.

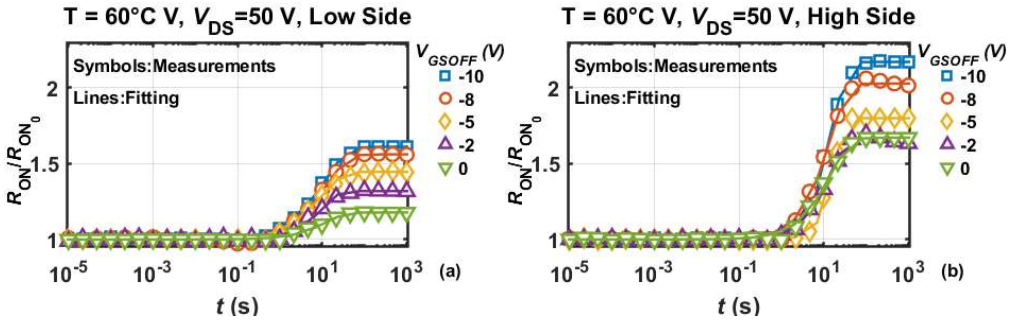
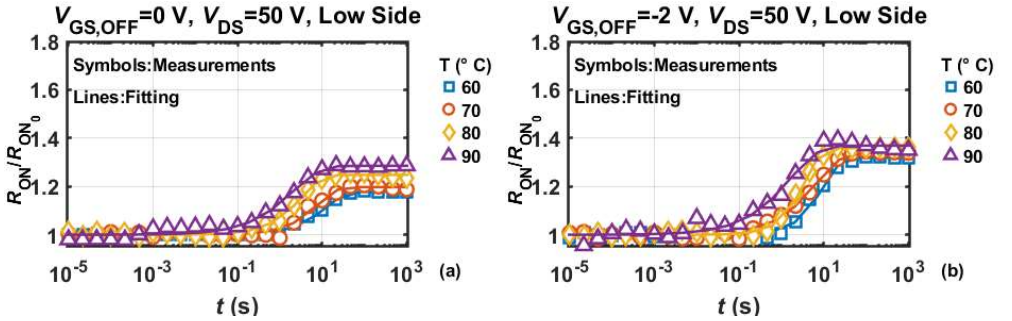


Figure 5. The transient for different $V_{GS,OFF}$ in LS (a) and HS (b). An higher OFF-state gate voltage (in absolute value) increase the degradation suffer from the device. While the OFF-state gate voltage has a strong effect on the magnitude of the degradation it appears to have no significant effect on the time constant of the transient.

Stress measurements have been carried out at different temperatures (60 °C to 90 °C with ΔT = 10 °C) for each of the $V_{GS,OFF}$ (from 0 V to -10 V). In Figure 6 are shown the transients at the different conditions for the LS device. As it can be seen, for $V_{GS,OFF}$ = 0 V the maximum degradation increases from ~17% at 60 °C to 28% at 90 °C. It is noticeable that the increasing temperature has not only the effect of increasing the amplitude of the dynamic on-resistance, but also to accelerate it. Figure 7 shows the results of the characterization on the HS device. Similar considerations as those observed for the LS device can be drawn, with the main difference being the increased degradation of the HS device. The degradation at $V_{GS,OFF}$ = 0 V increases from ~65 % (at 60 °C) to ~80% (at 90 °C). The temperature accelerates the transient in a manner similar to what occurs in the LS configuration. Figure 8 shows the Arrhenius plot constructed by using the time constants (τ) extracted from the temperature transients, the exact values of the τ's can be found in table I and II. It can be seen how the extract τ's for HS and LS at each $V_{GS,OFF}$ are essentially the same, indicating that the main mechanism responsible for the degradation is the same, specifically hole emission from C_N state in buffer. In figure 9 the dynamic has been normalized between 0 and 1 to highlight the independence of the time constant from the conditions (LS or HS) and the OFF-state gate voltage applied. As observed in our previous works [4], [22], hole emission increases the negative charge due to ionized acceptor traps in the buffer, thus reducing the 2-DEG concentration. The activation energy extracted (0.53 eV) is slightly lower to the one normally extracted for the C-related acceptor traps inside buffer layer, i.e., 0.9 eV above the valence band [23], [24], [25], [26], [27]. However it might be possible that field-enhancement mechanisms such as the Poole-Frenkel effect, that cause a lowering of the energy barrier for carrier emission at high V_{DS} voltage, explain the lower E_A's extracted from the data [23], [28], [29].



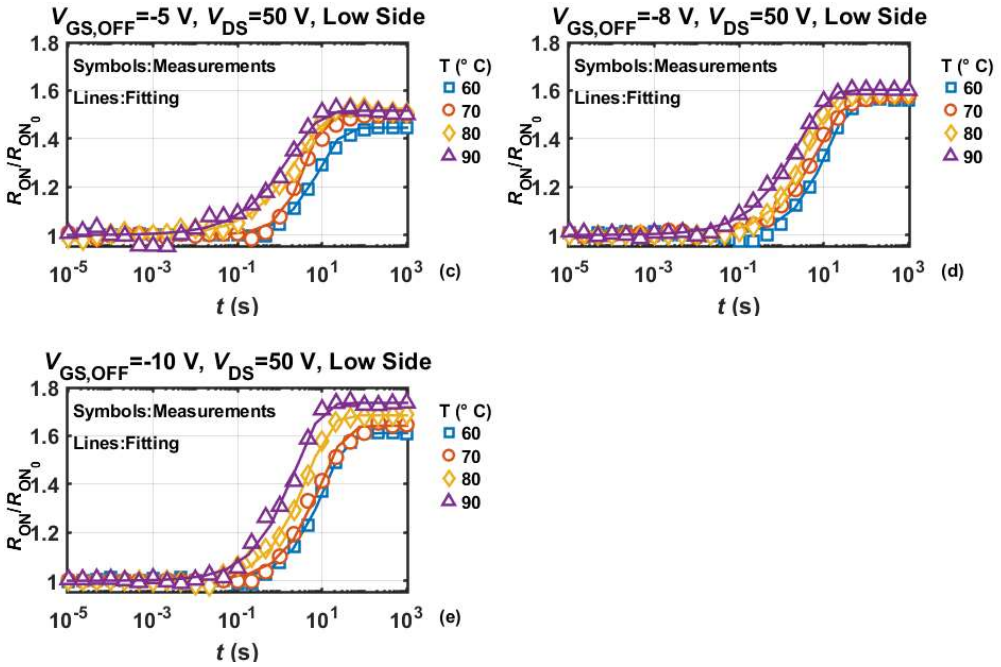
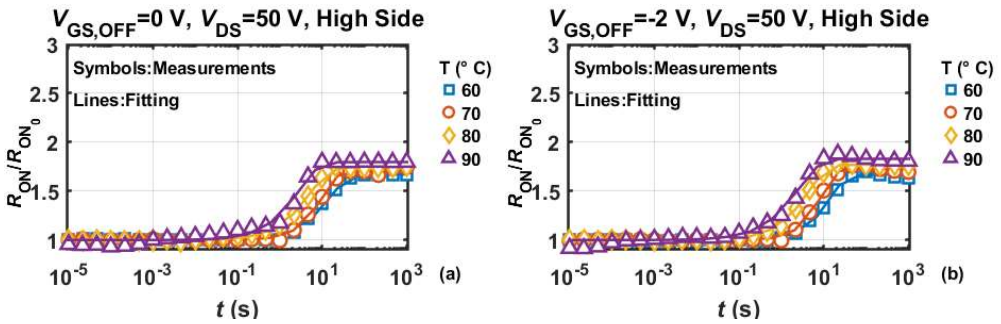


Figure 6. Temperature transient for $V_{GS,OFF}$ varying from 0 to -10 (a-e) for LS configuration . We can observe that regardless of the OFF-state gate voltage applied, the increasing temperature enhance the magnitude of the degradation and accelerate it.

The increased magnitude of the degradation in HS can be attributed to the back-gating effect, that is present when the substrate and the source are at a different potential. Under this condition, the 2-DEG is more depleted compared to the condition where the $V_{SB} = 0$ due to the higher relative shift between E_C and E_F. Moreover, the negative substrate potential promotes the hole emission from C_N states resulting in a larger amplitude of the R_{ON} dynamic. Nevertheless, the dynamics governed by the trapping process is the same for both LS and HS devices [17], [23], [30], [31].

Concerning the increase in degradation magnitude observed when a negative $V_{GS,OFF}$ is applied, could be attributed the enhancing of the vertical electric field under the gate during the OFF-state. The band bending induced by the field enhance the hole emission from the C-related acceptor traps located inside the buffer layer. As a consequence an higher number of holes are emitted from such traps, this results in a buffer layer that becomes even more negatively charged respect to the condition with a $V_{GS,OFF} = 0$,resulting in a stronger depletion of the 2DEG and thus an higher amplitude of the dynamic on-resistance. In figure 10 a sketch of the energy band illustrates this point.



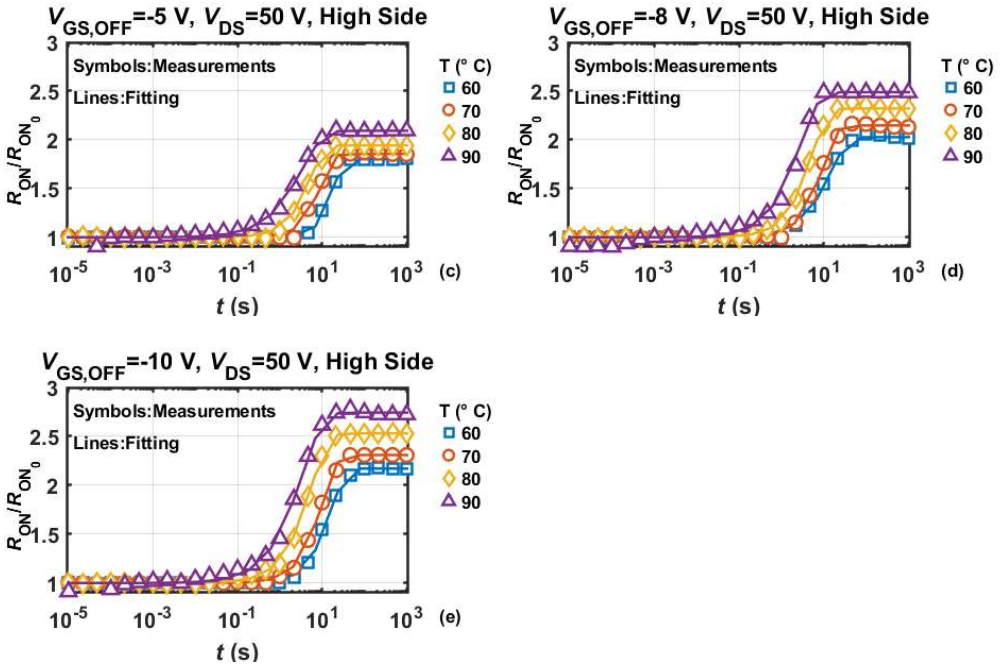


Figure 7. Temperature transient for $V_{GS,OFF}$ varying from 0 to -10 (a-e) for HS configuration. We can observe that regardless of the OFF-state gate voltage applied, the increasing temperature enhance the magnitude of the degradation and accelerate it.

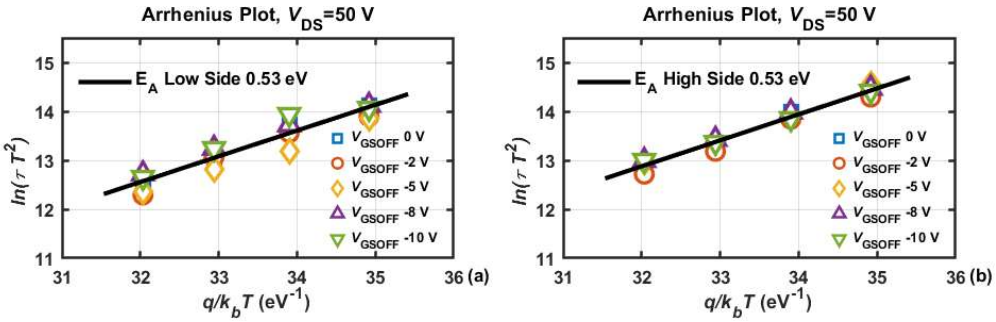


Figure 8. Arrhenius plot extracted from the time constant (τ's) of the transient at different temperatures and $V_{GS,OFF}$. We can see that both HS and LS are comparable in terms of τ's and activation energy. This means that the root cause responsible for the degradation in both cases is the same (i.e. C_N states inside buffer layer).

Table I. Time constant for LS measurements

LOW SIDE					
Tau (τ)	V_{GS} = 0 V	V_{GS} = -2 V	V_{GS} = -5 V	V_{GS} = -8 V	V_{GS} = -10 V
T = 60 °C	*12.2425 s*	*9.7503 s*	*9.3168 s*	*12.2731 s*	*11.5096 s*
T = 70 °C	*7.7952 s*	*6.6061 s*	*4.5267 s*	*7.7675 s*	*9.5766 s*
T = 80 °C	*3.3383 s*	*3.8005 s*	*2.9578 s*	*4.5387 s*	*4.5094 s*
T = 90 °C	*2.0492 s*	*1.6519 s*	*1.7821 s*	*2.5488 s*	*2.3630 s*

Table II. Time constant for HS measurements

HIGH SIDE					
Tau (τ)	V_{GS} = 0 V	V_{GS} = -2 V	V_{GS} = -5 V	V_{GS} = -8 V	V_{GS} = -10 V
T = 60 °C	*14.9764 s*	*14.5044 s*	*19.0595 s*	*17.4038 s*	*16.3329 s*
T = 70 °C	*10.0116 s*	*8.7010 s*	*9.3086 s*	*10.0694 s*	*8.7972 s*
T = 80 °C	*5.1196 s*	*4.2657 s*	*5.1934 s*	*5.4441 s*	*5.1049 s*
T = 90 °C	*2.7645 s*	*2.5311 s*	*3.2619 s*	*3.3459 s*	*3.3459 s*

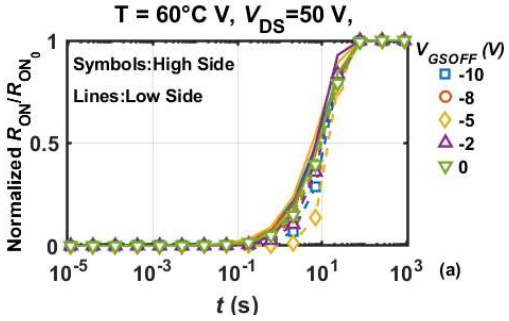


Figure 9. Dynamic on-resistance normalize between 0 and 1 for a baseplate temperature of 60 °C. This graph clearly shows the independence of the dynamic from the condition (LS and HS) and from the OFF-state gate voltage.

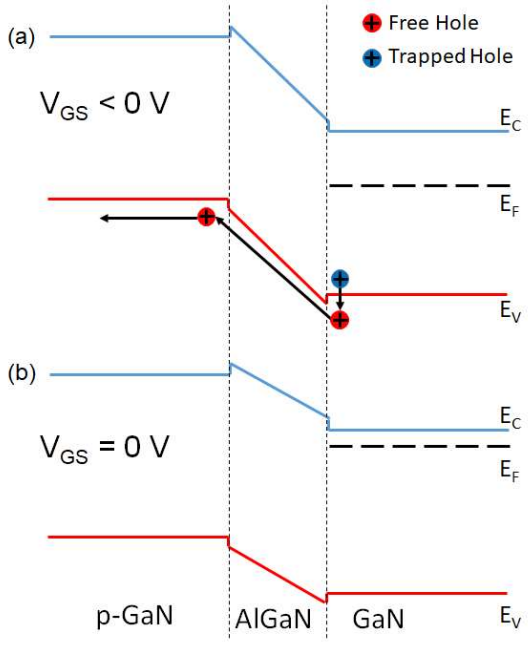


Figure 10. Sketch of the energy band in OFF-state when the V_{GS} is lower than 0 (a). When the negative V_{GS} is applied, the vertical field applied promotes the hole emission from the C-related acceptor traps inside the buffer that are attracted by the negative potential applied to the gate contact. In the panel b the equilibrium condition is shown as a reference

4. Conclusions

In this paper, we characterized the dynamic on-resistance of a on-wafer 100- V p-GaN HEMTs by means of a custom measurement setup able to replicate low- and high-

side biasing conditions of devices to be employed in monolithically integrated half-bridge circuits. Particularly, the setup allows considering the non-null source-to-body voltage experienced by the HS device during operation. The root cause for R_{ON} degradation in both LS and HS is found to be the hole emission from C_N states inside buffer layer, as confirmed by the extracted activation energies that are compatible with C-related acceptor traps. The additional degradation experienced by the device in HS (with respect to the LS case) is due to the negative bias applied between the substrate and the source, which causes an electrostatic back-gating effect. Finally, it was found that increasing the magnitude of the negative gate voltage applied during OFF-state stress further increases dynamic R_{ON}, in both LS and HS cases. This was attributed to the higher electric field near the gate contact that enhances hole emission from C-related acceptor traps thus leading to a larger dynamic R_{ON} variation.

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