US 20240313102A1

(19) United States
(12) Patent Application Publication
MICCOLI et al.
(10) Pub. No.: US 2024/0313102 A1
(43) Pub. Date: Sep. 19, 2024

(54) NORMALLY-OFF HETEROJUNCTION INTEGRATED DEVICE AND METHOD FOR MANUFACTURING AN INTEGRATED DEVICE

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(21) Appl. No.: **18/596,536**

(22) Filed: **Mar. 5, 2024**

(30) **Foreign Application Priority Data**

Mar. 13, 2023 (IT) 102023000004668

Publication Classification

(51) **Int. Cl.**

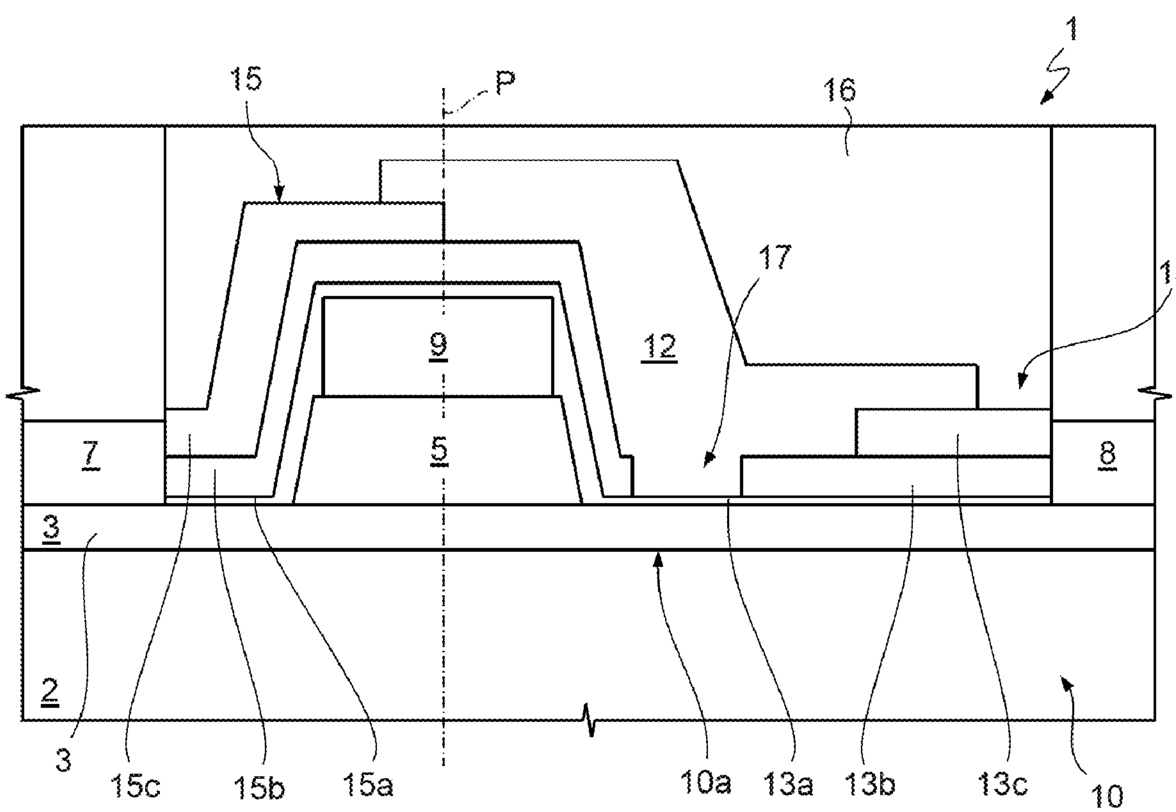
H01L 29/778	(2006.01)
H01L 29/20	(2006.01)
H01L 29/40	(2006.01)
H01L 29/423	(2006.01)
H01L 29/66	(2006.01)

(52) **U.S. Cl.**

CPC ***H01L 29/7786*** (2013.01); ***H01L 29/2003*** (2013.01); ***H01L 29/402*** (2013.01); ***H01L 29/42316*** (2013.01); ***H01L 29/66462*** (2013.01)

(57) **ABSTRACT**

An integrated power device includes a heterostructure, having a channel layer and a barrier layer, a source contact, a drain contact, and a gate region, arranged on the barrier layer between the source contact and the drain contact. An insulating field structure is arranged on the barrier layer between the gate region and the drain contact. A field plate extends over the insulating field structure. The insulating field structure includes a first dielectric region made of a first dielectric material on the barrier layer and a second dielectric region made of a second dielectric material, selectively etchable with respect to the first dielectric material on the first dielectric region. On a side of the insulating field structure towards the gate region, the field plate is in contact with the first dielectric region.



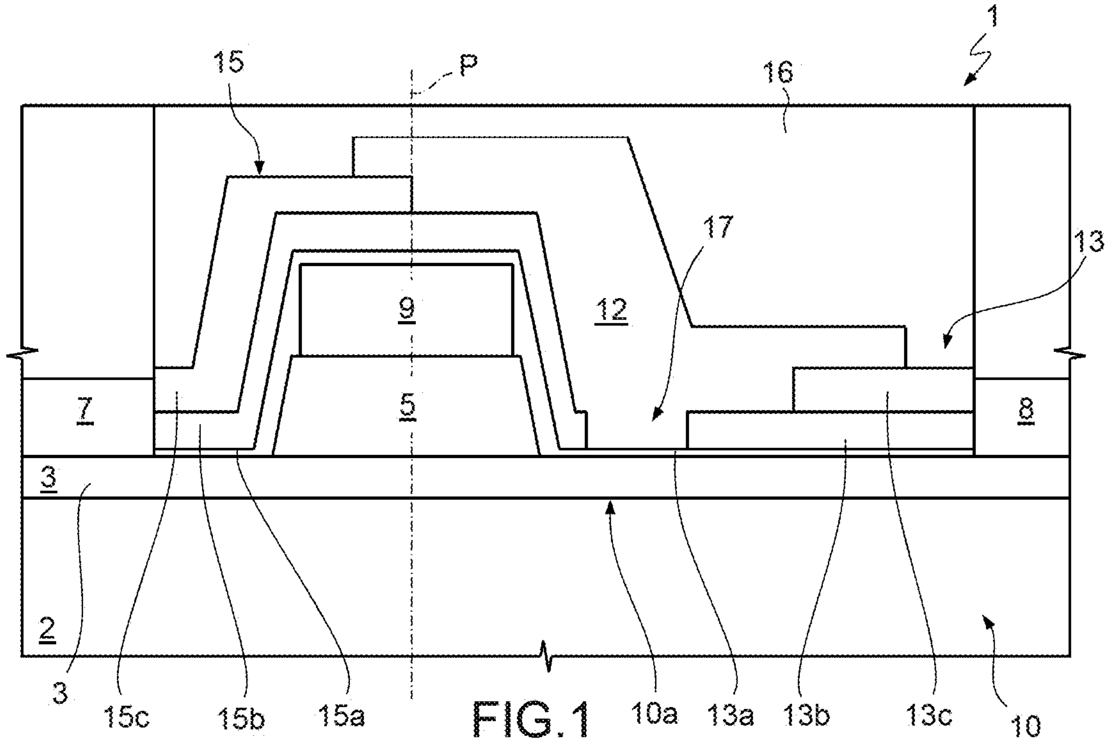

1
15
P
16
17
13
9
12
5
7
8
3
2
3
15c
15b
15a
10a
13a
13b
13c
10

FIG.1

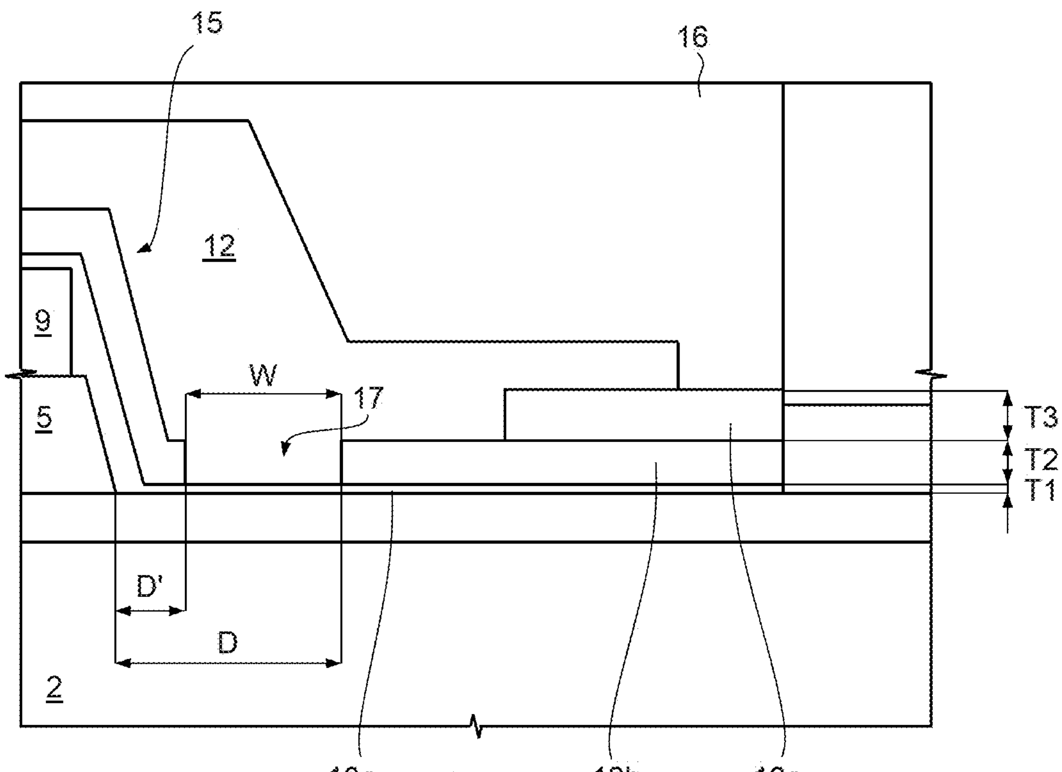

15
16
12
9
W
17
5
T3
T2
T1
D'
D
2
13a
13b
13c

FIG.2

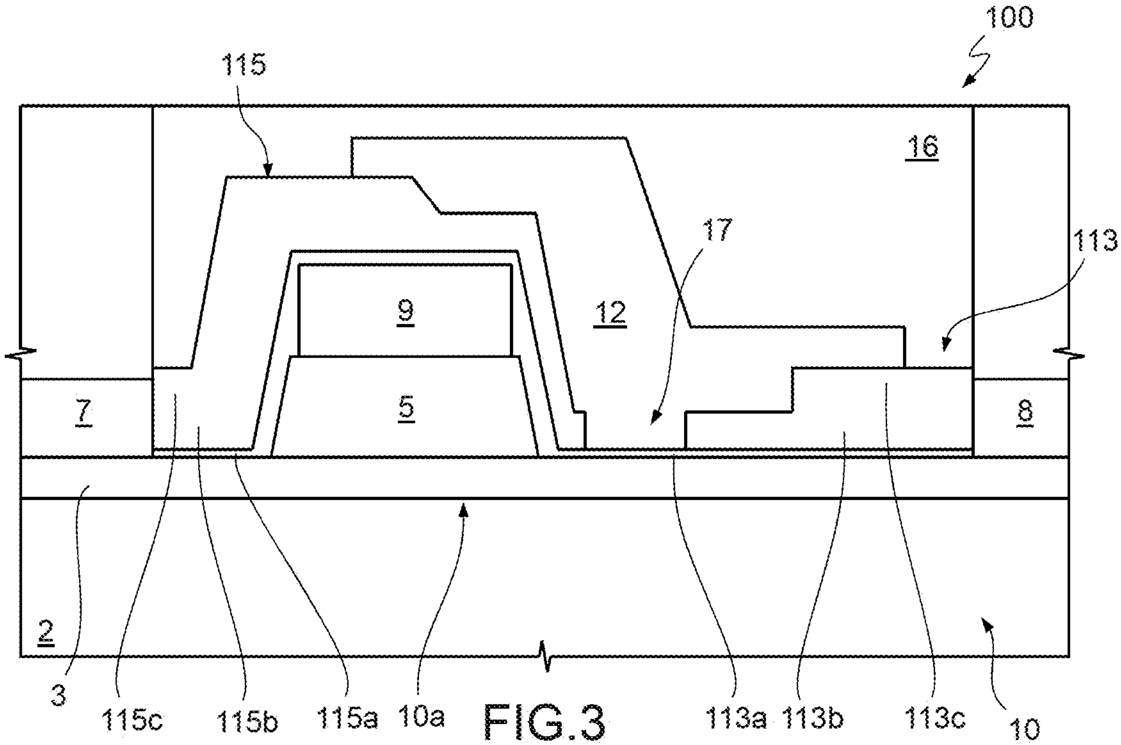

100
115
16
17
113
9
12
5
7
8
2
3
115c
115b
115a
10a
113a
113b
113c
10

FIG.3

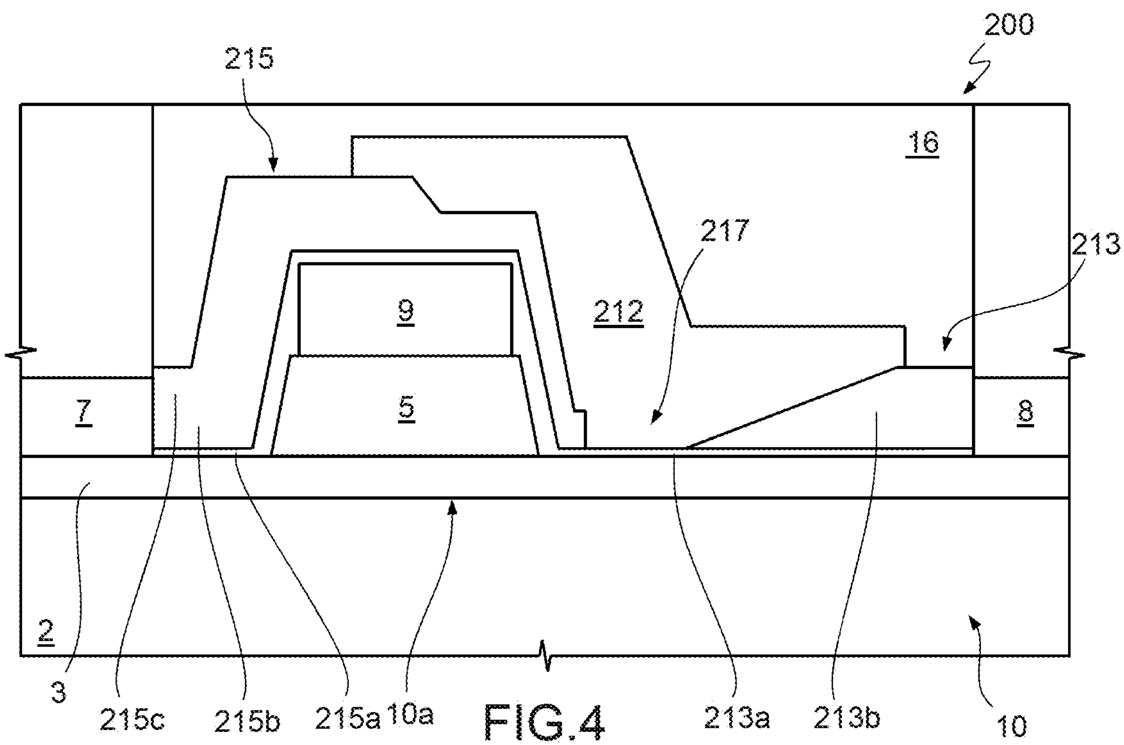

200
215
16
217
213
9
212
5
7
8
2
3
215c
215b
215a
10a
213a
213b
10

FIG.4

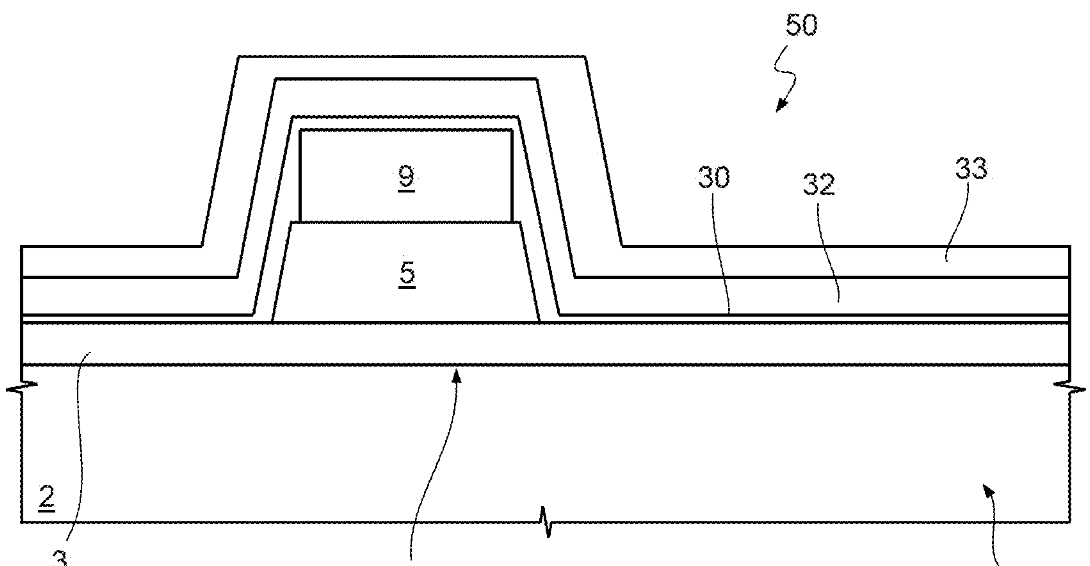


FIG.5

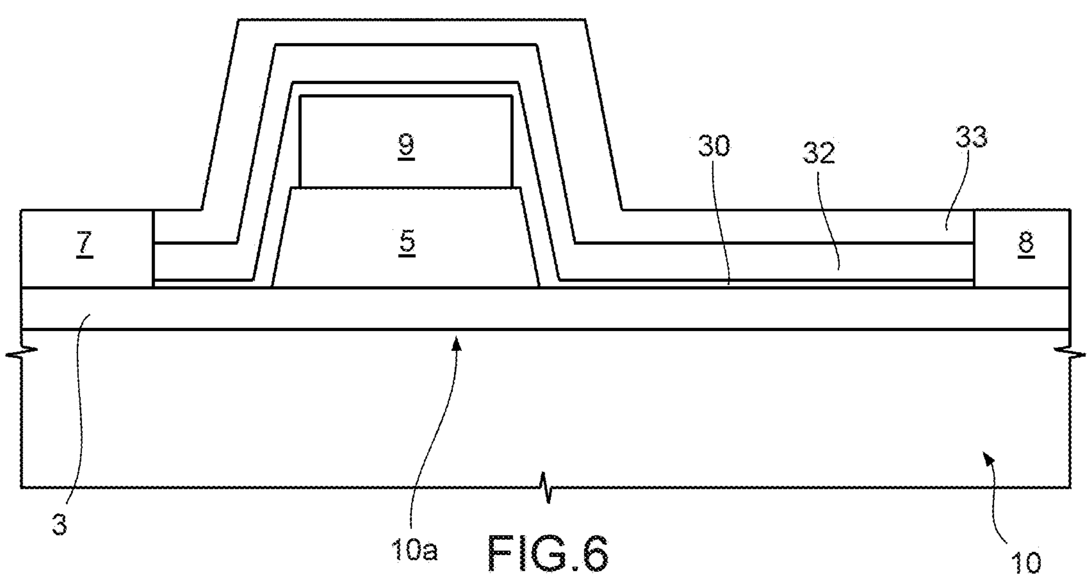


FIG.6

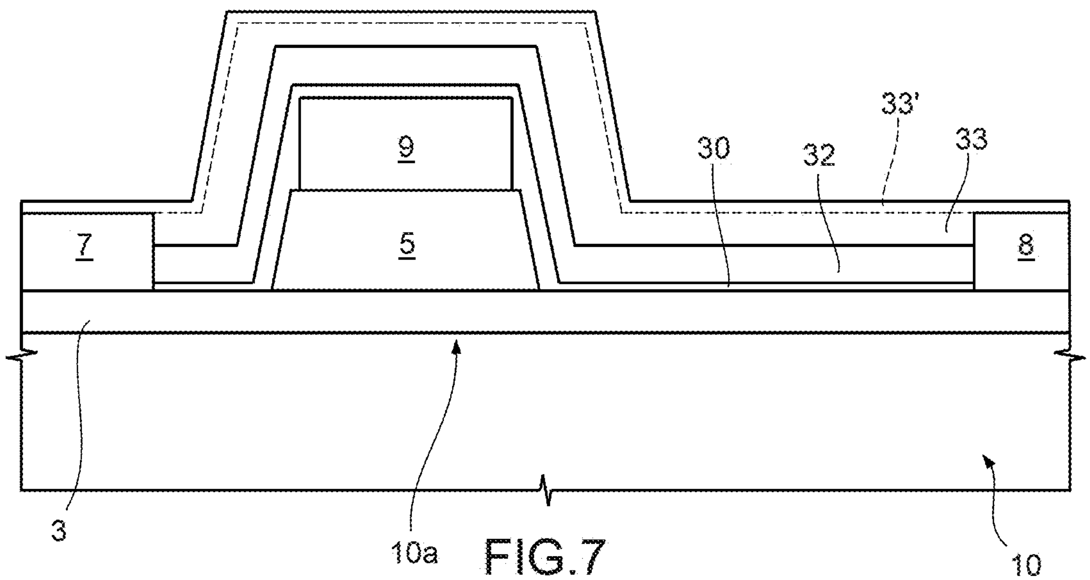


FIG.7

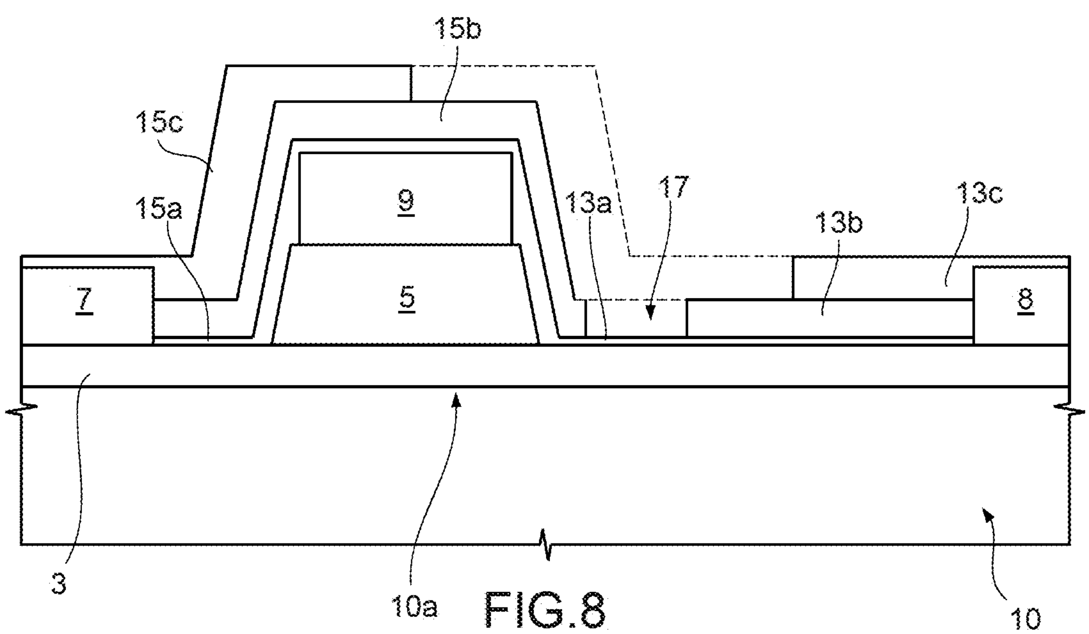


FIG.8

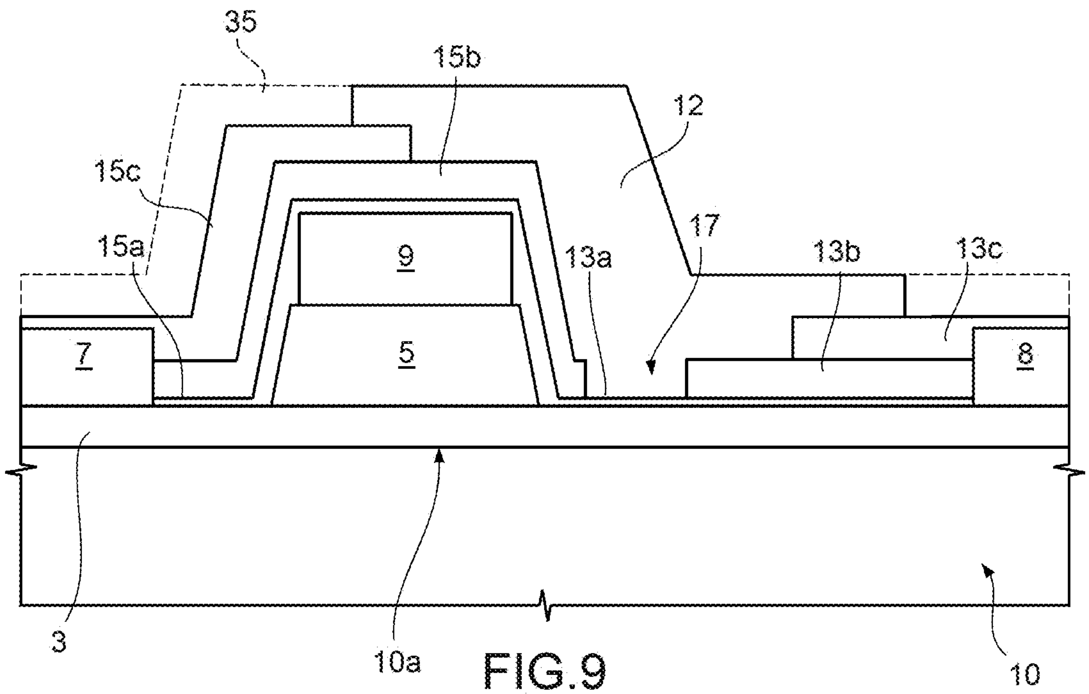


FIG.9

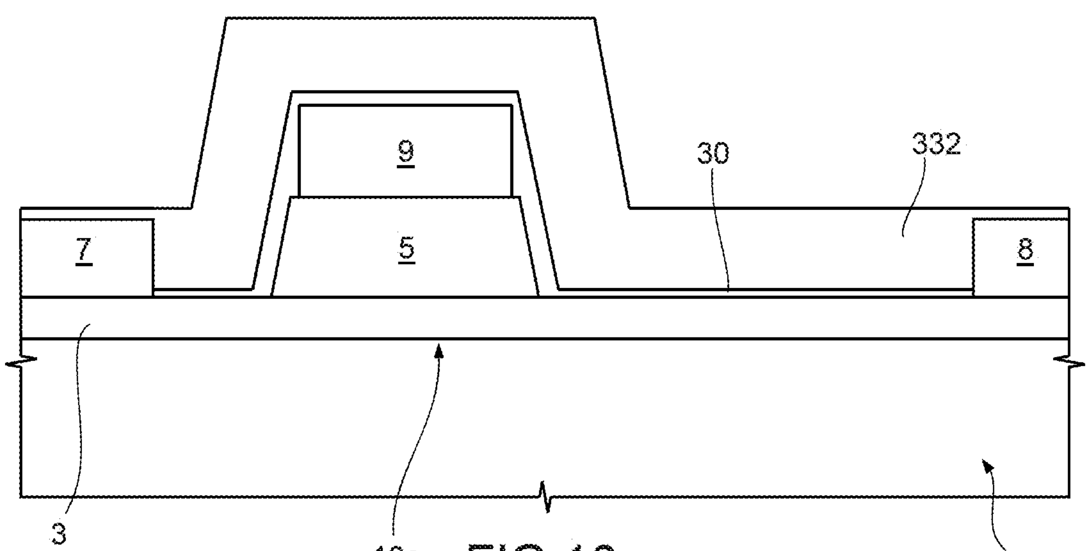


FIG.10

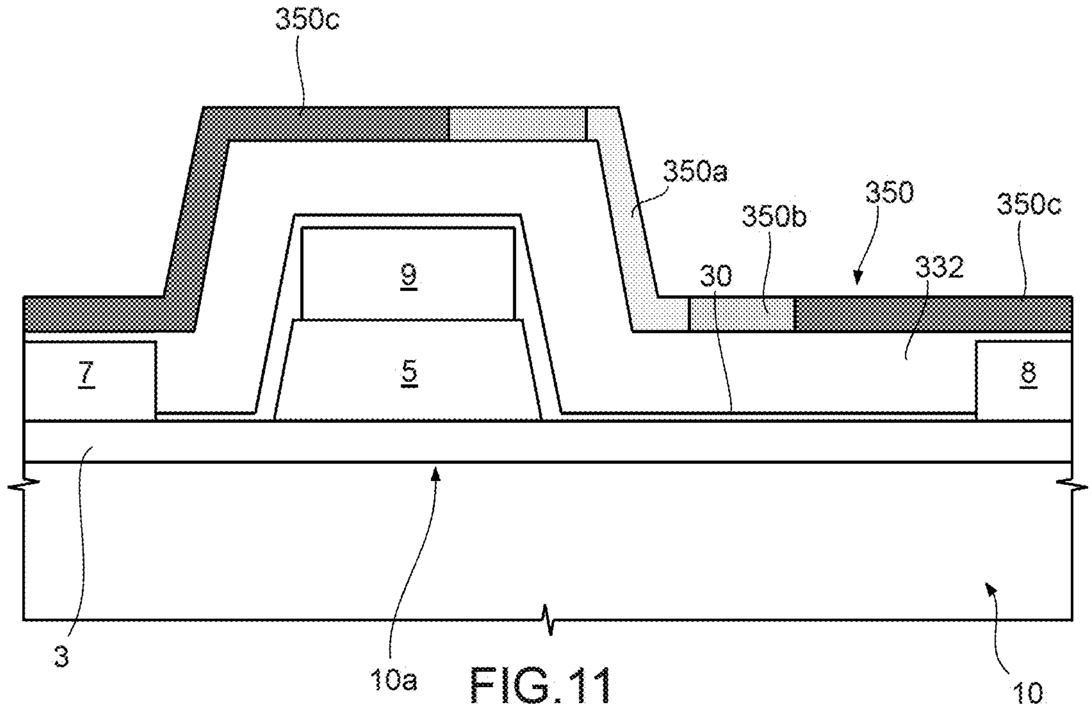

350c
350a
350
350b
350c
30
332
9
7
5
8
3
10a
10

FIG.11

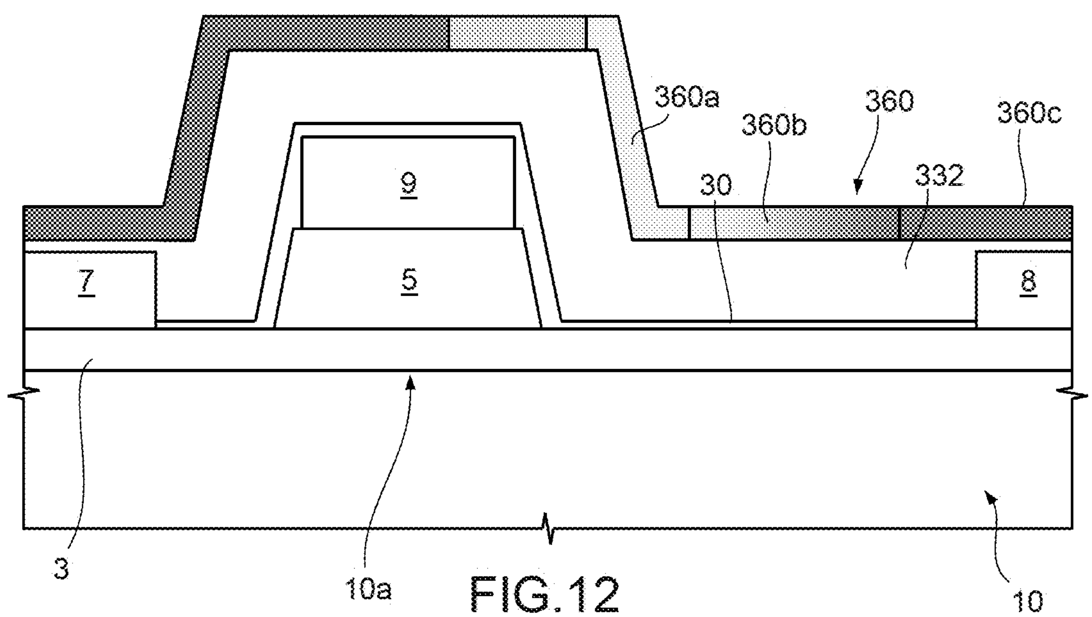

360a
360
360b
360c
30
332
9
7
5
8
3
10a
10

FIG.12

NORMALLY-OFF HETEROJUNCTION INTEGRATED DEVICE AND METHOD FOR MANUFACTURING AN INTEGRATED DEVICE

BACKGROUND

Technical Field

[0001] The present disclosure relates to a normally-off heterojunction integrated device and to a method for manufacturing an integrated device.

Description of the Related Art

[0002] As is known, heterostructures comprise contiguous layers or regions of materials, generally semiconductor materials, that have different bandgaps and define heterojunctions at the respective interfaces, where, on the basis of the physical and structural properties of the materials constituting the heterojunction, a two-dimensional electron gas (2DEG) may be formed. Some heterostructures are of great interest in the manufacture of field-effect transistors owing both to their breakdown resistance and to the density and mobility of the charge carriers in the proximity of the heterojunctions. For instance, AlGaN/GaN (aluminum and gallium nitride/gallium nitride) heterostructures are increasingly used for producing high-electron-mobility transistors (HEMTs) for high-power and high-frequency applications. The two-dimensional electron gas is in fact formed in an intrinsic region of the material having the narrower bandgap.

[0003] AlGaN/GaN HEMTs are in general of the normally on type, but, to guarantee proper operation and simplify the driving circuits, in many practical applications it is convenient to use also AlGaN/GaN HEMTs of the normally-off type. Different techniques are known for manufacturing normally-off AlGaN/GaN HEMTs. Amongst these, the so-called "p-GaN gate" technique is used on a commercial scale and entails formation of a p-doped GaN region on an AlGaN/GaN heterostructure, which comprises a GaN channel layer and an AlGaN barrier layer that define a heterojunction. The p-doped GaN region, or p-GaN gate region, is formed between the heterostructure and the gate electrode.

BRIEF SUMMARY

[0004] The solution is functionally correct, since it defines to all effects normally-off HEMTs; however, the performance may not be satisfactory, in particular in terms of maximum operating frequency. The limits are mainly due to the gate-to-drain capacitance and to the charge that it is consequently necessary to remove or inject for completing switching of the devices. There is therefore felt the need for devices of the normally-off type that will have a higher switching speed and will thus be usable for applications at higher frequencies.

[0005] The aim of the present disclosure is to provide an integrated power device and a method for manufacturing an integrated power device that will enable the limitations described above to be overcome or at least attenuated.

[0006] According to the present disclosure, an integrated device and a method for manufacturing an integrated device are provided, as defined in claims **1** and **12**, respectively.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

[0007] For a better understanding of the disclosure, some embodiments thereof will now be described, purely by way of not limiting example and with reference to the attached drawings, wherein:

[0008] FIG. **1** is a cross-sectional view through an integrated device according to one embodiment of the present disclosure;

[0009] FIG. **2** shows an enlarged detail of the device of FIG. **1**;

[0010] FIG. **3** is a cross-sectional view through an integrated device according to a different embodiment of the present disclosure;

[0011] FIG. **4** is a cross-sectional view through an integrated device according to a further embodiment of the present disclosure;

[0012] FIGS. **5-8** are cross-sectional views through a semiconductor wafer in successive steps of a method for manufacturing an integrated device according to an embodiment of the present disclosure;

[0013] FIG. **9** shows a cross-sectional view through a semiconductor wafer in a step of a method for manufacturing an integrated device according to a different embodiment of the present disclosure;

[0014] FIGS. **10** and **11** show a cross-sectional view through a semiconductor wafer in successive steps of a method for manufacturing an integrated device according to a further embodiment of the present disclosure; and

[0015] FIG. **12** shows a cross-sectional view through a semiconductor wafer in a step of a method for manufacturing an integrated device according to a further embodiment of the present disclosure.

DETAILED DESCRIPTION

[0016] With reference to FIGS. **1** and **2**, an integrated power device **1** is an embodiment of the present disclosure. The device **1** is a heterojunction integrated device of the normally-off type, in particular a HEMT (High-Electron-Mobility Transistor), and comprises a channel layer **2**, a barrier layer **3**, a gate region **5**, a source contact **7**, a drain contact **8**, and a gate contact **9**. The source contact **7** and the drain contact **8** may or may not be recessed with respect to the barrier layer **3**.

[0017] The channel layer **2** and the barrier layer **3** are made of respective semiconductor materials with different bandgaps and form a heterostructure **10**, with a heterojunction **10*a*** at a common interface. For instance, the channel layer **2** is of intrinsic gallium nitride (GaN), whereas the barrier layer **3** is of aluminum and gallium nitride (AlGaN) and has a conductivity of an N type. A two-dimensional electron gas (2DEG) is formed in a channel region of the channel layer **2** at the heterojunction **10**, between the source contact **7** and the drain contact **8**.

[0018] In addition to the channel layer **2** and the barrier layer **3**, the integrated device **1** may comprise other layers belonging or connected to the heterostructure **10**, amongst which, not necessarily and in a non-limiting way: a substrate having the function of mechanical support and/or electrical functions, for example of silicon or silicon carbide (SiC); a buffer layer between the substrate and the channel layer **2**; a spacer layer, for example of aluminum nitride (AlN), between the channel layer **2** and the barrier layer **3**; and a cap layer, for example of GaN, on the channel layer **3**.

[0019] The gate region **5** is formed in contact with the barrier layer **3** between the source contact **7** and the drain contact **8** and, in some embodiments, is of the same material forming the channel layer **2** (GaN) doped so as to have a conductivity opposite to that of the barrier layer **3**, in particular a conductivity of a P type in the example of FIG. **1**. The gate contact **9** extends over the gate region **5**.

[0020] A field plate **12** is connected (in a way not illustrated in FIG. **1**) to the source contact **7** and extends over the barrier layer **3** between the gate region **5** and the drain contact **8** and in part also over the gate region **5** and the gate contact **9**. An insulating field structure **13** separates the field plate **12** from the barrier layer **3** between the drain contact **8** and the gate region **5**. An insulating gate structure **15** separates the field plate **12** from the gate region **5** and from the gate contact **9**, as well as from the barrier layer **3** between the source contact **7** and the gate region **5**. A protective layer **16** of dielectric material, for example silicon oxide, coats the field plate **12**, the insulating field structure **13**, and the insulating gate structure **15**, and receives a source terminal **7***a*, a drain terminal **8***a*, and a gate terminal (not illustrated in FIG. **1**), which extend, respectively, as far as the source contact **7**, the drain contact **8**, and the gate contact **9**.

[0021] The insulating field structure **13** has variable a thickness in the embodiment of FIG. **1** increasing in stepwise fashion from the gate region **5** to the drain contact **8**. In greater detail, the insulating field structure **13** comprises a first dielectric region **13***a*, a second dielectric region **13***b*, and a third dielectric region **13***c*, which are stacked on top of one another and extend to different extents from the drain contact **8** towards the gate region **5**.

[0022] In some embodiments, the first dielectric region **13***a*, the second dielectric region **13***b*, and the third dielectric region **13***c* are portions of layers of a first dielectric material, a second dielectric material, and a third dielectric material, respectively, which are distinct from one another and each of which is selectively etchable with respect to the materials of the contiguous portions of the insulating field structure **13**. In particular, the first dielectric region **13***a*, the second dielectric region **13***b*, and the third dielectric region **13***c* may be of aluminum oxide (Al_2O_3), silicon oxide, and silicon nitride, respectively.

[0023] The first dielectric region **13***a* extends over the barrier layer **3** from the gate contact **8** as far as the gate region **5**, where it connects up to the insulating gate structure **15**, and has a first thickness T**1** not greater than 10 nm and for example comprised between 3 nm and 5 nm.

[0024] The second dielectric region **13***b* extends over the first dielectric region **13***a* from the gate contact **8**, up to a distance D, to the gate region **5** in such a way that a window **17** having a width W is defined between the second dielectric region **13***b* and the insulating gate structure **15**. The window **17** is occupied by a portion of the field plate **12** that is in contact with the first dielectric region **13***a*. In one embodiment, the distance D is, for example, 300 nm and the width W is, for example, 100 nm. The distance D and the width W may be selected in such a way that the margin of the window **17** opposite to the second dielectric region **13***b* will be at a desired distance from the gate region **5** of generally less than 200 nm. For instance, with the values indicated above (D=300 nm, W=200 nm), the window **17** is arranged at 100 nm from the gate region **5**.

[0025] The second dielectric region **13***b* has a second thickness T**2** not greater than 100 nm and comprised, for example, between 30 nm and 50 nm. In one embodiment, the second thickness T**2** is ten times greater than the first thickness T**1**.

[0026] The third dielectric region **13***c* extends over the second dielectric region **13***b* from the gate contact **8**, is shorter than the second dielectric region **13***b* so as to form a step, and is in part coated by the field plate **12**. The third dielectric region **13***b* has a third thickness T**3** not greater than 500 nm and comprised, for example, between 100 nm and 150 nm. In some embodiments, the third thickness T**3** is three times greater than the second thickness T**2**.

[0027] The field plate **12** consequently has three levels, corresponding to the first dielectric region **13***a*, the second dielectric region **13***b*, and the third dielectric region **13***c*, at respective distances T**1**, T**1**+T**2**, and T**1**+T**2**+T**3** from the surface of the barrier layer **3**.

[0028] In some embodiments, the insulating gate structure **15** comprises a first portion **15***a*, a second portion **15***b*, and a third portion **15***c*, which may be parts of the same layers of which the first dielectric region **13***a*, the second dielectric region **13***b*, and the third dielectric region **13***c*, respectively, are made and are thus of the same materials and have the same thicknesses. In practice, a first layer that forms the first dielectric region **13***a* of the insulating field structure **13** and the first portion **15***a* of the insulating gate structure **15** extend continuously between the source contact **7** and the drain contact **8**, coating the barrier layer **3**, the gate region **5**, and the gate contact **9**. A second layer forms the second dielectric region **13***b* of the insulating field structure **13** and the second portion **15***b* of the insulating gate structure **15**, which coats the gate region **5** and the gate contact **9** and extends as far as the window **17**, where the second layer is interrupted. The second portion **15***b* of the insulating gate structure **15** delimits the window **17** on the side towards the gate region **5**.

[0029] A third layer forms the third dielectric region **13***c* of the insulating field structure **13** and the third portion **15***c* of the insulating gate structure **15**, which extends from the source contact until it partially coats the gate region **5** and the gate contact **9**. For instance, the third portion **15***c* of the insulating gate structure **15** extends as far as a median plane P of the gate region **5** and of the gate contact **9**, perpendicular to the surface of the barrier layer **3**.

[0030] According to a different embodiment (illustrated in FIG. **3**), where parts that are the same as the ones already illustrated are designated by the same reference numbers, in an integrated device **100** an insulating field structure **113** and an insulating gate structure **115** have the same morphology and dimensions as the insulating field structure **13** and the insulating gate structure **15**, respectively, of FIG. **1**. In this case, however, the first dielectric region **113***a* of the insulating field structure **113** is made of a first material, for example aluminum oxide, whereas the second region **113***b* and the third region **113***c* of the insulating field structure **113** are both made of a second material, selectively etchable with respect to the first material, for example silicon oxide or silicon nitride. Likewise, the first portion **115***a* of the insulating gate structure **115** is made of the first material, whereas the second portion **115***b* and the third portion **115***c* are both made of the same material.

[0031] FIG. **4** shows an integrated device **200** according to a different embodiment of the present disclosure. The integrated device **200** comprises the channel layer **2** and the barrier layer **3**, which form: the heterostructure **10** and the heterojunction **10***a*; the gate region **5** with doping of a type opposite to that of the barrier layer **3**; the source contact **7**; the drain contact **8**; and the gate contact **9**. The integrated device **200** further comprises a field plate **212**, an insulating field structure **213**, and an insulating gate structure **215**. The insulating field structure **213** separates the field plate **212** from the barrier layer **3** between the drain contact **8** and the gate region **5**. The insulating gate structure **215** separates the field plate **212** from the gate region **5** and from the gate contact **9**, as well as from the barrier layer **3** between the source contact **7** and the gate region **5**.

[0032] The insulating field structure **213** has a thickness that for a stretch is constant, in the proximity of the gate region **5**, and for another stretch is variable in a ramp-wise fashion as far as the drain contact **8**. In greater detail, the insulating field structure **213** comprises a first dielectric region **213***a* and a second dielectric region **213***b*.

[0033] The first dielectric region **213***a* extends over the barrier layer **3** from the gate contact **8** as far as the gate region **5**, where it connects up to the insulating gate structure **215**. The first dielectric region **213***a* is made of a first material, for example aluminum oxide, and has a first constant thickness T**1** not greater than 10 nm, for example comprised between 3 nm and 5 nm.

[0034] The second dielectric region **213***b* is made of a second material, selectively etchable with respect to the material of the first dielectric region **213***a* and extends over the first dielectric region **213***a* forming an up-ramp that starts at a distance D from the gate region **5** and extends as far as the gate contact **8**. A window **217** of width W is consequently defined between the insulating gate structure **215** and the start of the ramp of the second dielectric region **213***b*. The field plate **212** thus contacts the first dielectric region **213***a* through the window **217**. The distance D and the width W are, for example, 300 nm and 100 nm, respectively. At the end of the ramp, the second dielectric region **213***b* reaches a second maximum thickness T**2'** not greater than 100 nm and comprised, for example, between 30 nm and 50 nm. At this point, the thickness of the dielectric field region **213** is thus T**1**+T**2'**.

[0035] The field plate **212** has a level corresponding to the first dielectric region **213***a* and in contact therewith and an inclined surface matching the ramp formed by the second dielectric region **213***b*.

[0036] In one embodiment, the insulating gate structure **215** comprises a first portion **215***a* and a second portion **215***b*, which may be parts of the same layers from which the first dielectric region **213***a* and the second dielectric region **213***b*, respectively, are formed. A first layer that forms the first dielectric region **213***a* of the insulating field structure **213** and the first portion **215***a* of the insulating gate structure **215** extends continuously between the source contact **7** and the drain contact **8**, coating the barrier layer **3**, the gate region **5** and the gate contact **9**. A second layer forms the second dielectric region **213***b* of the insulating field structure **213** and the second portion **215***b* of the insulating gate structure **215**, which coats the gate region **5** and the gate contact **9** and extends as far as the window **17**, where the second layer is interrupted. The second portion **215***b* of the insulating gate structure **215** delimits the window **17** on the side towards the gate region **5**.

[0037] With reference to FIGS. **5**-**9**, in a method for manufacturing the integrated device **1** according to an embodiment of the present disclosure, in a semiconductor wafer **50** the heterostructure **10** is initially made, and the gate region **5** and the gate contact **9** are formed on the heterostructure **10**. Then, a first dielectric layer **30**, a second dielectric layer **32**, and a third dielectric layer **33** are laid in succession on the heterostructure **10** and on the gate region **5**, coating both of these.

[0038] The first dielectric layer **30** is made of the first material, for example aluminum oxide, and has the first thickness T**1**. The second dielectric layer **32** is made of the second material, for example silicon oxide, and has the second thickness T**2**. The third dielectric layer **33** is made of the third material, for example silicon nitride, and in one embodiment has a thickness that is less than the third thickness T**3**.

[0039] The first dielectric layer **30** defines the first dielectric region **13***a* of the insulating field structure **13** and the first portion **15***a* of the insulating gate structure **15**.

[0040] Next (FIG. **6**), the source contact **7** and the drain contact **8** are formed. For this purpose, the first dielectric layer **30**, the second dielectric layer **32**, and the third dielectric layer **33** are etched using a same mask, and an operation of metal sputtering is carried out, followed by an annealing step.

[0041] The third dielectric layer **33** is then increased as far as the third desired thickness T**3**, which is obtained with a further deposition of the third material. The increase of the third dielectric layer **33** due to the further deposition is designated by **33'** in FIG. **7**. In this step, the source contact **7** and the drain contact **8** are coated so as to be kept separated from one another during subsequent formation of the field plate **12**.

[0042] The third dielectric layer **33** and the second dielectric layer **32** are then selectively etched in succession, in the order illustrated in FIG. **8**. For the etching operations respective masks are used, which are not illustrated for reasons of simplicity. The etches stop automatically on the underlying layers, given that the materials selected are selectively etchable. In particular, from the third dielectric layer **33** the third dielectric region **13***c* of the insulating field structure **13** and the third portion **15***c* of the insulating source structure **15** are obtained. In the second dielectric layer **32** the window **17** is opened, thus separating the second dielectric region **13***b* of the insulating gate structure **13** from the second portion **15***b* of the insulating source structure **15** and exposing the first dielectric region **13***a*.

[0043] A metal layer **35** is then formed by metal evaporation and subsequently patterned using a further mask (not illustrated) to form the field plate **12** (FIG. **9**). During this step, the source contact **7** and the gate contact **8** are coated and protected by a portion of the third dielectric layer **33** obtained during the deposition to enable increase to the third thickness T**3**.

[0044] Final machining steps are then carried out, amongst which the step of laying the protective layer **16** and the step of providing the source terminal **7***a* and the drain terminal **8***a*. The integrated device **1** of FIG. **1** is thus obtained.

[0045] According to variants not illustrated of the method, the third dielectric layer **33** and the second dielectric layer **32** are selectively etched in succession, in that order, prior to formation of the source contact **7** and the drain contact **8**, to define the insulating field structure **13** (third dielectric region

13*c* and second dielectric region **13***b*) and the insulating source structure **15**. In particular, according to one embodiment, after etching of the third dielectric layer **33** and the second dielectric layer **32**, contact windows are opened for the source contact **7** and the drain contact **8**, and a metal layer is laid by sputtering and subsequently defined to form simultaneously the source contact **7**, the drain contact **8**, and the field plate **13**. Alternatively, first the metal layer is formed by sputtering, then contact windows are opened for the source contact **7** and the drain contact **8**, and the metal layer is patterned to form the insulating field structure **13**, and finally the source contact **7** and the drain contact **8** are formed by metal evaporation.

[0046] According to a different embodiment of the method according to the disclosure (FIG. **10**), the heterostructure **10** and the gate region **5** are initially formed. Then, the first dielectric layer **30** and a second dielectric layer **332**, for example, of silicon oxide, are laid in succession in order on the heterostructure **10** and on the gate region **5**, thus coating both. The first dielectric layer **30** and the second dielectric layer **332** are then patterned to open contact windows, where the source contact **7** and the drain contact **8** are formed. The second dielectric layer **332** may be brought to the final desired thickness by a further deposition of the second dielectric material, which also covers the source contact **7** and the drain contact **8**.

[0047] With reference to FIG. **11**, the second layer **332** is then defined to form the insulating field structure using a "greyscale" lithographic technique, which makes it possible to obtain differentiated densities of photoresist from a single layer (see, for example, Yu Pang, Yi Shu, Mohammad Shavetipur, Xucfeng Wang, Mohammad Ali Mohammad, Yi Yang, Haiming Zhao, Ningqin Deng, Roya Maboudian, and Tian-Ling Ren, "3D Stretchable Arch ribbon Array Fabricated via Grayscale Lithography", Scientific Reports, volume 6, Article number: 28552 (2016)). In practice, exploiting the diffraction through a mask with variable density and/or aperture widths, a photoresist layer is exposed and impressed in a differentiated way. In areas with higher densities and/or aperture widths, the photoresist is more exposed and a lower final density is obtained; instead, in areas with lower densities and/or aperture widths, the photoresist is exposed to a lesser extent, and a final higher density is obtained. In FIG. **11** and in the subsequent FIG. **12**, the variable density of the photoresist layer is represented by different shades of grey: corresponding to regions with higher density is a darker shade of grey, and corresponding to regions with lower density is a lighter shade of grey.

[0048] Consequently, to obtain the integrated device **100** of FIG. **3** it is possible to use a protective photoresist layer **350** (FIG. **11**) having a portion **350***a* with minimum density, a portion **350***b* with intermediate density, and a portion **350***c* with maximum density on the first dielectric region **113***a*, the second region **113***b*, and the third region **113***c*, respectively, of the insulating field structure **113**.

[0049] To obtain, instead, the integrated device **200** of FIG. **3** it is possible to use a protective photoresist layer **360** (FIG. **12**) having a portion **360***a* with minimum density, a portion **360***b* with linearly variable density, and a portion **360***c* with maximum density on the first dielectric region **213***a* and the second region **213***b*, respectively, of the insulating field structure **213**. The density of the portion **360***b* varies between the minimum density of the portion **360***a* and the maximum density of the portion **360***c*.

[0050] The disclosure advantageously enables improvement of the performance of integrated power devices, in particular of HEMTs of the normally-off type. More precisely, the use of materials that may be selectively etched with respect to one another for producing the insulating field structure enables control of the thickness of the first portion of the insulating field structure with a precision of the order of nanometers. The limit of precision is in fact determined by the processes of deposition with which it is possible to form layers having a thickness of even very few atoms. Etching of the overlying structures stops automatically owing to the selectivity of the materials, without any need for fine time control, and the thickness of the underlying layer, in particular of the first portion of the insulating field structure, is not involved. In this way, in the proximity of the gate region, the field plate may be reduced to just a few nanometers from the barrier layer, i.e., a distance equal to the thickness of just the first portion of the insulating field structure. This makes it possible to reduce drastically the gate-to-drain capacitance and, consequently, the accumulated charge, to the benefit of performance of the integrated device. As the distance from the gate region increases, the thickness of the insulating field structure may increase according to the design preferences so as to maintain the breakdown resistance. Also the profile of the insulating field structure may be chosen according to the design preferences, for example stepwise or rampwise. Advantageously, the thickness of the insulating field structure has at least an intermediate value between a minimum value in the proximity of the gate region and a maximum value at the drain terminal.

[0051] Finally, it is evident that modifications and variations may be made to the integrated device and to the method described herein, without thereby departing from the scope of the present disclosure, as defined in the annexed claims.

[0052] For instance, the insulating field structure may have a greater number of steps (four or more) according to the design preferences.

[0053] An integrated power device may be summarized as including: a heterostructure (**10**), including a channel layer (**2**) and a barrier layer (**3**); a source contact (**7**), a drain contact (**8**) and a gate region (**5**), wherein the gate region (**5**) is arranged on the barrier layer (**3**) between the source contact (**7**) and the drain contact (**8**); an insulating field structure (**13**) arranged on the barrier layer (**3**) between the gate region (**5**) and the drain contact (**8**); and a field plate (**12**) on the insulating field structure (**13**), wherein the insulating field structure (**13**; **113**; **213**) includes a first dielectric region (**13***a*; **113***a*; **213***a*) of a first dielectric material on the barrier layer (**3**) and a second dielectric region (**13***b*; **113***b*; **213***b*) of a second dielectric material, selectively etchable with respect to the first dielectric material on the first dielectric region (**13***a*; **113***a*; **213***a*); and wherein, on a side of the insulating field structure (**13**; **113**; **213**) towards the gate region (**5**), the field plate (**12**) is in contact with the first dielectric region (**13***a*; **113***a*; **213***a*).

[0054] A window (**17**; **217**) may be defined between the insulating gate structure (**15**) and the second dielectric region (**13***b*; **113***b*; **213***b*) and the field plate (**12**) may be in contact with the first dielectric region (**13***a*; **113***a*; **213***a*) in the window (**17**; **217**).

[0055] The window (**17**) may be arranged at a distance (D') from the gate region (**5**) of less than 200 nm.

[0056] The first dielectric region (**13***a*; **113***a*; **213***a*) may have a first thickness (T1) of less than 10 nm, for example between 3 nm and 5 nm.

[0057] The insulating field structure (**13**; **113**; **213**) may have a minimum thickness, corresponding to the first thickness (T**1**) of the first dielectric region (**13***a*; **113***a*; **213***a*), on the side of the insulating field structure (**13**; **113**; **213**) towards the gate region (**5**), a maximum thickness (T**1**+T**2**+T**3**; T**1**+T**2**') on a side of the insulating field structure (**13**; **113**; **213**) towards the drain terminal (**3**), and an intermediate thickness (T**1**+T**2**) between the side towards the gate region (**5**) and the side towards the drain terminal (**3**) of the insulating field structure (**13**; **113**; **213**).

[0058] The insulating field structure (**13**; **113**) may have a stepwise profile and may include a third dielectric region (**13***c*; **113***c*) on the second dielectric region (**13***b*; **113***b*).

[0059] The second dielectric region (**13***b*; **113***b*) may have a second thickness (T**2**) not greater than 100 nm, for example between 30 nm and 50 nm, and the third dielectric region (**13***c*; **113***c*) may have a third thickness (T**3**) not greater than 500 nm, for example between 100 nm and 150 nm.

[0060] The third dielectric region (**13***c*) may be made of a third dielectric material, selectively etchable with respect to the second dielectric material.

[0061] The first dielectric region (**13***a*), the second dielectric region (**13***b*), and the third dielectric region (**13***c*) may be made of aluminum oxide, silicon oxide, and silicon nitride, respectively.

[0062] The second dielectric region (**213***b*) of the insulating field structure (**213**) may have a rampwise profile.

[0063] The barrier layer (**3**) may have a first conductivity type and the gate region (**5**) may have a second conductivity type, opposite to the first conductivity type.

[0064] A method for manufacturing an integrated power device, may be summarized as including: forming a heterostructure (**10**), including a channel layer (**2**) and a barrier layer (**3**); on the barrier layer (**3**), forming a source contact (**7**), a drain contact (**8**), and a gate region (**5**) between the source contact (**7**) and the drain contact (**8**); forming an insulating field structure (**13**) on the barrier layer (**3**) between the gate region (**5**) and the drain contact; and forming a field plate (**12**) on the insulating field structure (**13**); wherein forming the insulating field structure (**13**; **113**; **213**) includes: forming a first dielectric layer (**30**) of a first dielectric material on the barrier layer (**3**); forming a second dielectric layer (**32**; **332**) of a second dielectric material, selectively etchable with respect to the first dielectric material on the first dielectric region (**13***a*; **113***a*; **213***a*); selectively etching the second dielectric layer (**32**; **332**) on a side of the insulating field structure (**13**; **113**; **213**) towards the gate region (**5**) so as to expose a portion of the first dielectric layer (**30**) at the gate region (**5**); and wherein the field plate (**12**) is in contact with the first dielectric region (**13***a*; **113***a*; **213***a*) where the first dielectric region (**13***a*; **113***a*; **213***a*) has been exposed.

[0065] Selectively etching may include defining a window (**17**; **217**) between the insulating gate structure (**15**) and the second dielectric region (**13***b*; **113***b*; **213***b*) and the field plate (**12**) may be in contact with the first dielectric region (**13***a*; **113***a*; **213***a*) in the window (**17**; **217**).

[0066] Forming the insulating field structure (**13**) may include: forming a third dielectric layer (**33**) of a third dielectric material, selectively etchable with respect to the second dielectric material on the second dielectric layer (**13***b*); and selectively etching the third dielectric material (**33**) so as to expose the second dielectric layer (**32**) between the window (**17**; **217**) and the drain contact (**8**) and define a stepwise profile of the insulating field structure (**13**).

[0067] Forming the insulating field structure (**113**; **213**) may include patterning the second layer (**332**) with a greyscale lithographic technique so as to define a stepwise or rampwise profile of the insulating field structure (**113**; **213**).

[0068] The various embodiments described above can be combined to provide further embodiments. Aspects of the embodiments can be modified, if necessary to employ concepts of the various patents, applications and publications to provide yet further embodiments.

[0069] These and other changes can be made to the embodiments in light of the above-detailed description. In general, in the following claims, the terms used should not be construed to limit the claims to the specific embodiments disclosed in the specification and the claims, but should be construed to include all possible embodiments along with the full scope of equivalents to which such claims are entitled. Accordingly, the claims are not limited by the disclosure.

1. An integrated power device comprising:
a heterostructure, including a channel layer and a barrier layer;
a source contact, a drain contact and a gate region, wherein the gate region is on the barrier layer between the source contact and the drain contact, the gate region having a top side, a first lateral side, and a second lateral side;
an insulating field structure on the barrier layer between the gate region and the drain contact; and
a field plate on the insulating field structure,
wherein the insulating field structure comprises a first dielectric region of a first dielectric material on the barrier layer and a second dielectric region of a second dielectric material, selectively etchable with respect to the first dielectric material on the first dielectric region;
wherein, on a side of the insulating field structure towards the gate region, the field plate is in contact with the first dielectric region; and
wherein the field plate overlaps the first lateral side of the gate region, partially overlaps the top side of the gate region, and does not overlap the second lateral side of the gate region.

2. The device according to claim **1**, comprising an insulating gate structure between the field plate and the gate region, wherein a window is between the insulating gate structure and the second dielectric region and the field plate is in contact with the first dielectric region in the window.

3. The device according to claim **2**, wherein the window is at a distance from the gate region of less than 200 nm.

4. The device according to claim **1**, wherein the first dielectric region has a first thickness of less than 10 nm.

5. The device according to claim **1**, wherein the insulating field structure has a minimum thickness, corresponding to the first thickness of the first dielectric region, on the side of the insulating field structure towards the gate region, a maximum thickness on a side of the insulating field structure towards the drain terminal, and an intermediate thickness between the side towards the gate region and the side towards the drain terminal of the insulating field structure.

6. The device according to claim **5**, wherein the insulating field structure has a stepwise profile and comprises a third dielectric region on the second dielectric region.

7. The device according to claim **6**, wherein the second dielectric region has a second thickness between 30 nm and 50 nm, and wherein the third dielectric region has a third thickness between 100 nm and 150 nm.

8. The device according to claim **6**, wherein the third dielectric region is made of a third dielectric material, selectively etchable with respect to the second dielectric material.

9. The device according to claim **6**, wherein the first dielectric region, the second dielectric region, and the third dielectric region are made of aluminum oxide, silicon oxide, and silicon nitride, respectively.

10. The device according to claim **1**, wherein the second dielectric region of the insulating field structure has a rampwise profile.

11. The device according to claim **1**, wherein the barrier layer has a first conductivity type and the gate region has a second conductivity type, opposite to the first conductivity type.

12. A method for manufacturing an integrated power device, comprising:

forming a heterostructure, including a channel layer and a barrier layer;

on the barrier layer, forming a source contact, a drain contact, and a gate region between the source contact and the drain contact, the gate region having a top side, a first lateral side, and a second lateral side;

forming an insulating field structure on the barrier layer between the gate region and the drain contact; and

forming a field plate on the insulating field structure;

wherein forming the insulating field structure comprises:

forming a first dielectric layer of a first dielectric material on the barrier layer;

forming a second dielectric layer of a second dielectric material, selectively etchable with respect to the first dielectric material on the first dielectric region;

selectively etching the second dielectric layer on a side of the insulating field structure towards the gate region so as to expose a portion of the first dielectric layer at the gate region;

wherein the field plate is in contact with the first dielectric region where the first dielectric region has been exposed; and

wherein the field plate overlaps the first lateral side of the gate region, partially overlaps the top side of the gate region, and does not overlap the second lateral side of the gate region.

13. The method according to claim **12**, comprising forming an insulating gate structure between the field plate and the gate region; wherein selectively etching comprises defining a window between the insulating gate structure and the second dielectric region and wherein the field plate is in contact with the first dielectric region in the window.

14. The method according to claim **13**, wherein forming the insulating field structure comprises:

forming a third dielectric layer of a third dielectric material, selectively etchable with respect to the second dielectric material on the second dielectric layer; and

selectively etching the third dielectric material so as to expose the second dielectric layer between the window and the drain contact and define a stepwise profile of the insulating field structure.

15. The method according to claim **13**, wherein forming the insulating field structure comprises patterning the second layer to define a stepwise profile of the insulating field structure.

16. The method according to claim **13**, wherein forming the insulating field structure comprises patterning the second layer to define a rampwise profile of the insulating field structure.

17. A HEMT transistor comprising:

a heterostructure having a first surface;

a source terminal on the first surface;

a drain terminal on the first surface;

a gate region on the first surface between the source terminal and the drain terminal, the gate region having a top side, a first lateral side facing the drain terminal, and a second lateral side facing the source terminal;

a first dielectric layer between the source terminal and drain terminal, on the gate region and the first surface;

a first insulating structure on the first dielectric layer and in contact with the drain terminal;

a second insulating structure on the first dielectric layer and in contact with the source terminal, the first insulating structure not in contact with the second insulating structure; and

a field plate of conductive material between the gate region and the drain terminal, on the first insulating structure, partially on the second insulating structure, and partially overlapping the gate region.

18. The HEMT transistor of claim **17**, wherein the second insulating structure comprises:

a first portion overlapping the top side, the first lateral side, and the second lateral side of the gate region; and

a second portion overlapping the first lateral side of the gate region, partially overlapping the top side of the gate region, but not overlapping the second lateral side of the gate region.

19. The HEMT transistor of claim **18**, wherein the first portion and the second portion of the second insulating structure are made of different materials.

20. The HEMT transistor of claim **17**, wherein the field plate is electrically coupled to the source terminal.

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