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Wide-bandgap based power converters for improved efficiency and reliability

Candidato: Mattia Vogni

Relatore: Prof. Claudio Bianchini

Coordinatore del Corso di Dottorato: Prof. Luigi Rovati

One of the ways of stopping science would be only to do experiments in the region where you know the law. But experimenters search most diligently, and with the greatest effort, in exactly those places where it seems most likely that we can prove our theories wrong. In other words, we are trying to prove ourselves wrong as quickly as possible, because only in that way can we find progress.

Richard P. Feynman

Sommario

Il settore dell'elettronica di potenza e degli azionamenti elettrici è oggi orientato verso soluzioni sempre più compatte, efficienti e affidabili. Con la progressiva diffusione dei transistor a banda larga (Wide-BandGap, WBG) sul mercato, tale tendenza sta incontrando un'ulteriore accelerazione. È ormai comprovato che questi semiconduttori offrono prestazioni superiori rispetto alle tradizionali controparti in silicio. I dispositivi in carburo di silicio (SiC) e nitruro di gallio (GaN) presentano elementi parassiti reattivi di piccola entità e possono pertanto operare a frequenze di commutazione più elevate, consentendo una significativa riduzione del volume e del peso dei convertitori. Se in ambiti quali la difesa, la conversione statica ad alta efficienza e, più in generale, le applicazioni orientate alle prestazioni, tali tecnologie rappresentano già una realtà consolidata, nei settori industriale e automobilistico il costo costituisce ancora il principale ostacolo alla loro diffusione su larga scala. In questi contesti, una progettazione preliminare accurata e dettagliata risulta imprescindibile. Ne consegue la necessità di disporre di un modello preciso e rapido per la stima delle perdite di potenza nei transistor WBG, al fine di effettuare un confronto appropriato tra le diverse soluzioni tecniche, per poi.

In questo contesto, il presente lavoro introduce i concetti fondamentali e gli sviluppi più recenti relativi ai dispositivi WBG, per poi concentrarsi sull'elaborazione di un modello delle perdite di potenza, utilizzato per la stima dell'efficienza dei convertitori analizzati e sviluppati nel corso della tesi. In particolare, vengono esaminati convertitori basati su tecnologia SiC, tra cui inverter fotovoltaici e a sorgente di corrente destinati sia ad applicazioni nel campo delle energie rinnovabili sia a contesti industriali, oltre a un convertitore risonante impiegato per caricabatterie di bordo per veicoli elettrici. Gli elementi di novità del lavoro comprendono strategie di controllo innovative e nuove tecniche di modulazione, accompagnate da un'analisi originale e dettagliata dell'impatto di tali azionamenti sulle perdite del motore in un sistema di accumulo di energia a volano (Flywheel Energy Storage System). In tal modo, la ricerca qui presentata affronta in maniera organica lo studio dei convertitori basati su dispositivi WBG, con l'obiettivo di migliorarne l'efficienza e l'affidabilità complessiva.

Abstract

The world of power electronics and electric drives is nowadays leading towards more compact, efficient, and reliable solutions. With the penetration of wide-bandgap transistors in the market, this tendency is speeding up. These semiconductors have already been proven to be more efficient than their Silicon counterparts. Silicon Carbide, SiC, and Gallium Nitride, GaN devices have smaller parasitic reactive elements, and therefore they can be operated at higher switching frequencies, significantly reducing the volume and weight of the converter. While for defense, high-efficient static conversion and any other performance-oriented applications they are the present, for industrial and automotive drives, the cost remains the main obstacle to their diffusion. In these cases, a correct and detailed preliminary design is mandatory. A precise and fast power losses model for these WBG transistors becomes necessary to make a proper comparison of the solution.

This work introduces the basic concepts and newest developments on WBG devices, then proceeds with the development of the power losses model, which will be used throughout the whole thesis for the efficiency estimation of converters which have been studied and developed subsequently. In the thesis, converters with SiC technology are dissected: especially photovoltaic and current source inverters for both renewable and industrial applications, as well as a resonant converter for on-board battery charger. The elements of novelty include innovative control strategies and new modulation techniques with a new insight on the impact of these drives on the motor losses for a Flywheel Energy Storage System application. In this way, the research on converters with WBG devices for improved efficiency and reliability is addressed in this thesis.

Acknowledgments

I am deeply grateful to my Ph.D. supervisor, Prof. Claudio Bianchini, for giving me the opportunity to follow this path. I would also like to thank my colleagues at Raw Power, from your expertise I have learned so much. At the same time, I would like to thank Prof. Davide Barater and Prof. Giovanni Franceschini, who have been my supervisors for the first year.

A special thanks goes to Prof. Alessandro Chini for his support and valuable help in the work presented in the first chapter, as well as to the SiCTech Induction crew — especially Dr. Juan Luis Bellido Ruiz — without whom the experimental tests of the last chapter would not have been possible.

I also wish to thank the "Politecnico di Torino", in particular Dr. Fausto Stella and Prof. Paolo Pescetto, for their collaboration and assistance.

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Contents

Introduction

0.1 Motivation and structure of the thesis

The author received a research grant from the European project YESvGaN, whose objectives are listed in this first introduction chapter and especially in 0.2. Because the aim of the project was the development of vertical GaN transistor on Silicon substrate for high voltage (up to 1200 V) power converters, the thesis title and research project followed consequently: "Wide-bandgap based power converters for improved efficiency and reliability". Mainly two chapters were dedicated to the project, chapter 1 and chapter 2. None of them includes the development of vertical GaN based-board: due to the ambitious goal and regardless the incredible work of the other partners, it was not possible to manufacture and characterize these transistors up to 1200 V, neither up to 100 V; thus, they have been found unsuitable for any high power density application in this early stage of the project. Moreover, the development and simulation of a digital-twin as well as a benchmark prototype with SiC transistors was an active goal for both Raw Power S.r.l. and UNIMORE as partners of the project and since vGaNs were meant to completely substitute the known lateral devices, such as HEMTs, the comparison with these counterparts was outside the scope of the project. For these main reasons, the author dedicated its research work to converters based on SiC technology. Here, a summary of the topics developed in each chapter is given.

- **Chapter 1**, entitled "Switching Loss Model for SiC MOSFETs Based on Datasheet Parameters" deals with a fast and accurate switching losses model for SiC MOSFETs based on the available data of the manufacturer. This first chapter provides a novel numerical-analytical model which accounts for all the important aspects of the switching transition, making assumptions for secondary or third order effects that does not impact the efficiency calculation. A complete set of experimental tests was carried out to validate the model, and a comparison with existing ones in the literature was made. The first chapter is also the basis for the others, since the same model applied to different parts was used to evaluate the efficiency of the power converters studied here in these three years.

- **Chapter 2**, entitled "Three-phase SiC Photovoltaic Inverter" deals with the development of a three-phase DC Bus board for a photovoltaic inverter. As the first chapter, this work was part of the YESvGaN project.

- **Chapter 3**, entitled "Current Source Inverter Drive of an Ironless Motor for Flywheel Batteries" proposes to drive an ironless motor for a Flywheel Energy Storage System (FESS) application with a current source inverter and compares the results of the study with a traditional voltage source inverter drive. Comparison was made in simulations employing SiC-base inverters and the same part numbers. The results showed similar efficiency with the exclusion of parasitic components. Then, a complete and detailed experimental analysis was made on the motor side to highlight the advantage of the unconventional drive. Experimental techniques were also used to validate a fast and accurate AC loss model for this motor.

- **Chapter 4**, entitled "Extended Flux-Weakening Control Technique with a Current Source Inverter" contains an extended flux-weakening control technique of an interior permanent magnet machine fed by a current source inverter. As in the previous chapter, architectures are compared in simulation, and the benefits of the current source inverter are explained. In the chapter, a specific type of space-vector modulation is employed and discussed to reduce the well-known resonance problem of these drives. Experimental validations remain a future development.

- **Chapter 5**, entitled "Innovative Asymmetric Modulation for a Resonant Dual Active Bridge" proposes a new modulation pattern for an on-board charger application. This work is supported by analytical dissertation, simulation, HIL test for the control of the converter, and experimental tests on the hardware. Two additional modulation techniques were developed and compared with the novel one that shows the benefits of the proposed modulation.

- **Conclusions** summarize the work done and provide a list of published papers and those which have been submitted and are currently being reviewed.

To improve readability, bibliography is reported at the end of each chapter.

0.2 Introduction to the YESvGaN project

This thesis was developed concurrently with the European project YESvGaN, of which both UNIMORE and Raw Power S.r.l. are partners. The author is a PhD candidate at UNIMORE and was a collaborator of this company. His research grant was funded by the European project YESvGaN, therefore, this paragraph briefly explains the main objectives of the project. Regarding the contribution to the project, Chapter 1 was the main innovative contribution. For the project itself, also a prototype of a PV inverter was developed, a brief description of it is given in Chapter 2. This paragraph represents an introduction to the framework of the YESvGaN project.

The worldwide spread of electric energy systems, referring to electric energy transportation or electric vehicles (EV), hybrid electric vehicles (HEV) or household appliances or industrial electric drives, is concurrent with the diffusion of power electronic converters. Converters are the key to generate and transform electrical energy, and switching devices represent their main core, both structurally and economically. Today silicon (Si) power semiconductors, especially insulated gate bipolar transistors (IGBTs), are the most used due to their low cost and high power ratings; however, more efficient devices already exist in the market, such as Silicon Carbide (SiC) MOSFETs or Gallium Nitride (GaN) transistors. Both SiC and GaN are termed wide band-gap (WBG) materials, and they have enormous potential in terms of enhancing the efficiency of power converters and reducing passive component volumes due to their high switching frequency capabilities. They are thought to be interesting, especially for efficiency driven applications with more than one conversion stage, such as uninterruptible power supplies (UPS), power factor correction (PFC) boost, traction, and photovoltaic inverters, as they allow reducing losses and saving energy. However, WBG market penetration is still limited; see Fig. 0.1. In fact, existing GaNs, such as High Electron Mobility Transistors (HEMTs) are adopted under 1 kW, since their later structure is not suitable for high power applications even if they are manufactured at costs comparable to Si transistors. On the other hand, SiC devices can serve high power ratings and reach a high blocking voltage, 1200 V and sustain high currents, 100 A while still maintaining low conduction losses, but they are manufactured on native SiC substrates of limited size, which significantly increase their costs. Therefore, they are used mainly on 150 kW.

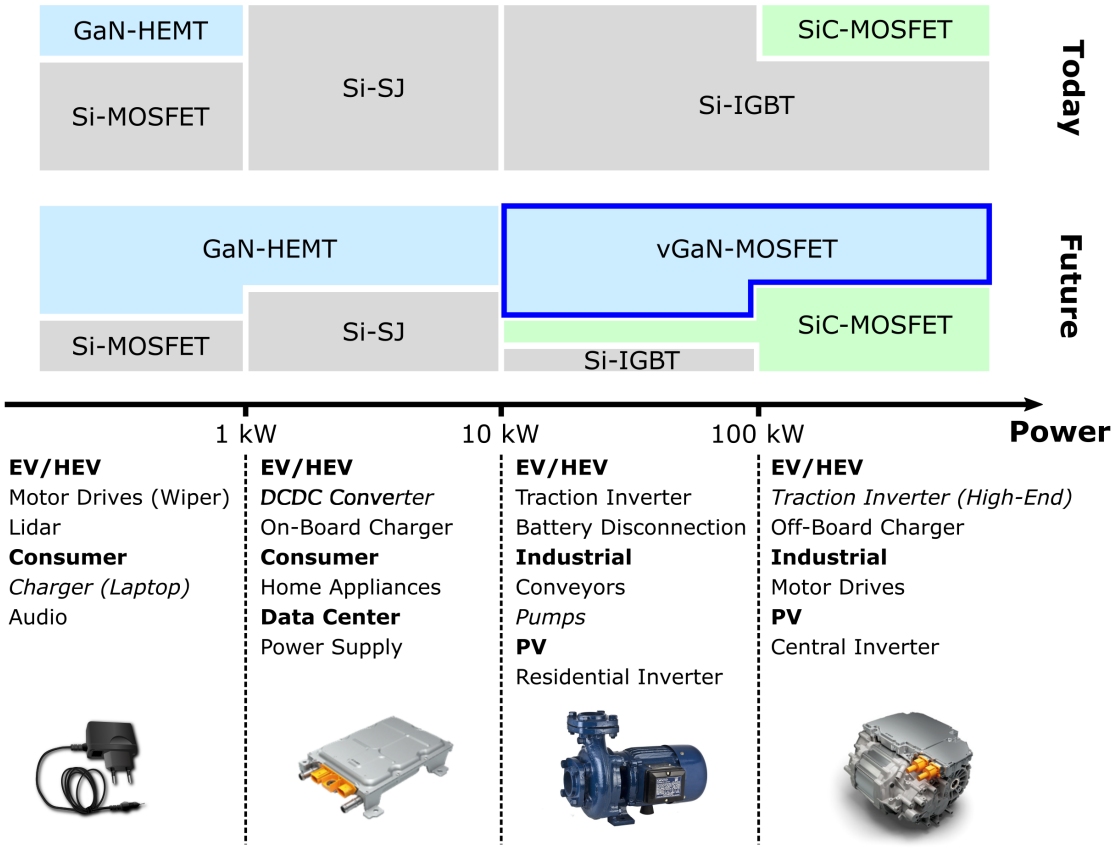

Figure 0.1: Application fields of power transistors.

The YESvGaN project aims to fill the market gap, between $50 - 150$ kW, introducing a new class of vertical GaN (vGaN) MOSFETs, called vertical membrane transistors, with high power ratings, similar to SiC MOSFETs, at Silicon cost. The affordability of these novel transistors should be reached by employing heteroepitaxial GaN layers on a low-cost substrate such as silicon or sapphire. The idea is also to increase the substrate size, up to 300 mm, to reduce the cost per chip area compared to SiC devices. In fact, WBG substrates are really expensive and responsible for the 50 % of the total chip cost; therefore, the YESvGaN approach would drastically reduce their cost, with the possibility to reduce their price on the market as well. Moreover, the substrate will be then removed locally and the active layers will then be contacted electrically, this would lead to a low resistance and a high blocking voltage: the vertical structure is suitable for high currents flowing, see Fig. 0.2.

The YESvGaN project is not limited to the realization of vGaN chips, but extends its objectives to their testing and applicability on real converters. The main goal of the project is the development of a new type of GaN-based power transistors on silicon or sapphire substrates,

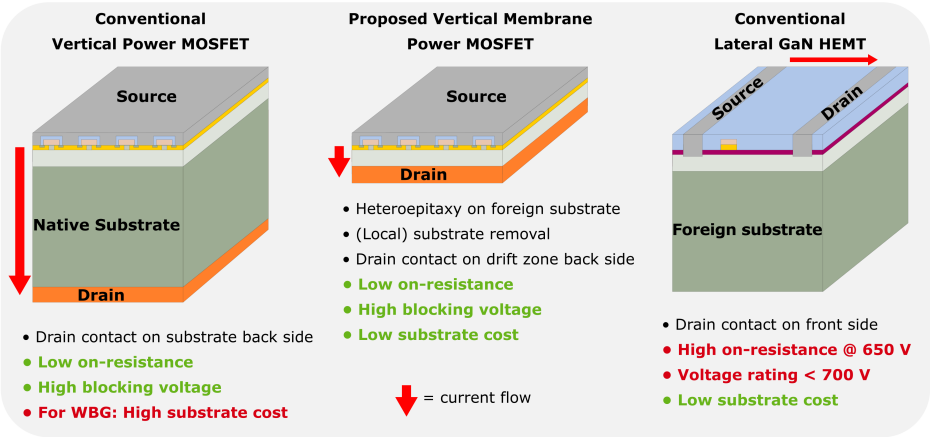

Figure 0.2: Comparison between vertical power MOSFET, conventional GaN HEMT and proposed vGaN structures.

with high voltage, 1.2 kV, and high current, 100 A ratings at low cost. These GaN could be a powerful replacement for existing IGBTs, primarily due to these advantages:

- With respect to IGBTs, they are unipolar devices and therefore can avoid a forward voltage drop of a bipolar transistor.
- Reduced switching losses because they are the majority carrier devices and avoids high reverse recovery losses, for example.
- Reduced conduction losses, due to the properties of the WBG material.
- Higher switching frequency capabilities, which allows to reduce the volume and weight of passive components in power converters, inductors, and capacitors.
- Extension of the EV/HEV range per KWh equal battery capacity.
- Lower heat generation in power modules and energy savings due to very high efficiency.

Especially in grid connected applications, such as PV inverters or UPS in data centers, they would allow energy savings due to increased efficiencies, above 98 % for the whole converter, and would also allow reducing the complexity of the architectures. The same consideration on efficiency combined with affordable cost, similar to that for Si transistors, should be made on traction inverters for power train applications in compact cars, where the price of the power converters is the main drive. At the same time, in power modules, employed in industry applications, cheap transistors are needed, and vGaN could be an innovative solution. For EV/HEV chargers, they would allow reducing the overall volume and cost of the structure, since SiC transistors are usually not an option, and Si IGBTs have limited switching frequencies, which are the main cause of critical requirements on the volume. Furthermore, the development

of a new technology would allow the European position on the market to be strengthened since the supply of WBG substrates, such as those for SiC MOSFETs, comes from foreign countries, especially the US. The YESvGaN solution could be a way to open new business branches in this vision. Since the intent is clear, in the following chapter, the main objectives of the project will be defined along with their main challenges.

0.3 Project objectives

The main objectives of the YESvGaN project are listed below and also represent the respective work packages (WP).

1. Development of vertical drift epitaxy that allows $600-1200$ V blocking voltage on low-cost substrates.
2. Development of the vertical transistor itself and its process technology, aiming to achieve $600-1200$ V breakdown voltage and < 4 mΩ cm^2 at a cost of 0.06 €/mm^2.
3. Development of membrane process technology, allowing parasitic resistance below 0.5 mΩ cm^2.
4. Development of advanced interconnection technology for vGaN and evaluation of its reliability.
5. Understanding performance limitations, degradation, and failure mechanism in particular.
6. Test of vGaN power transistors mounted on demonstrators, such as EV chargers or PV inverters with high power ratings and verifying the improved efficiency. The final goal is to provide datasheets of their static and dynamic behavior.

Raw Power S.r.l. and UNIMORE are both part of WP6 and therefore it treat the application side of the project. These two represent just a small part of the 23 partners: Robert Bosch GmbH (Coordinator, Germany), AIXTRON SE (Germany), Aurel S.p.A. (Italy), Centre National de la Recherche Scientifique (CNRS) / IEMN (France), EV Group (EVG) (Austria), Ferdinand-Braun Institut gGmbH (FBH) (Germany), Fraunhofer-Gesellschaft (IISB) (Germany), Finepower GmbH (Germany), Ion Beam Services (IBS) (France), IUNET – Consorzio Nazionale Interuniversitario per la Nanoelettronica (Italy), NanoWired GmbH (Germany), Raw Power Srl (Italy), SiCtech INDUCTION (Smart Induction Converter Technologies S.L.) (Spain), Siltronic AG (Germany), Soitec Belgium NV (Belgium), STMicroelectronics (Tours) SAS (France), Ghent University (Belgium), Lunds Universitet (University of Lund) (Sweden),

University of Valencia (Universitat de València) (Spain), X-FAB Dresden GmbH & Co. KG (Germany), X-FAB Global Services GmbH (Germany), Materials Center Leoben Forschung GmbH (MCL) (Austria) and HexaGAM AB (Sweden).

The following subsections are about the main challenges of each WP and their objectives.

0.3.1 GaN epitaxy for up to 1200 V low-cost substrates

One of the most challenging part of developing a low-cost substrate that enables 1200 V is the possibility of finding a trade-off between a high blocking voltage and low conduction losses for the device. That is more challenging for vGaN than for GaN HEMTs, since these lasts have a thinner epitaxy, instead a thicker epitaxy requires accommodating the bow induced by the lattice mismatch between GaN and substrate during growth. The process requires homogeneous doping at low concentration in order to grow thick GaN transistors on Si. Firstly, 200 mm wafer will be used, then 300 mm ones. In the end, a specific attention should be made on low defect density and layers reformation to reach high blocking voltages. As it can be seen in Fig. 0.3, the conventional GaN on Si HEMT epitaxy is different from the proposed one. Specifically, the vertical structure do not require an insulating GaN layer of $1-2$ µm, instead a thick $6-10$ µm GaN epitaxy with low and controlled n-doping and low defect concentration in order to achieve high blocking voltage and low conduction losses. The buffer layer AlGaN or GaN is mandatory to enable crystalline growth with low number of defects. Moreover, between Si and GaN, a strong lattice mismatch due to different coefficients of thermal expansion creates a bow, that explain the need for a buffer layer. The main challenge lies in the optimization of the buffer layer for a thick GaN epi.

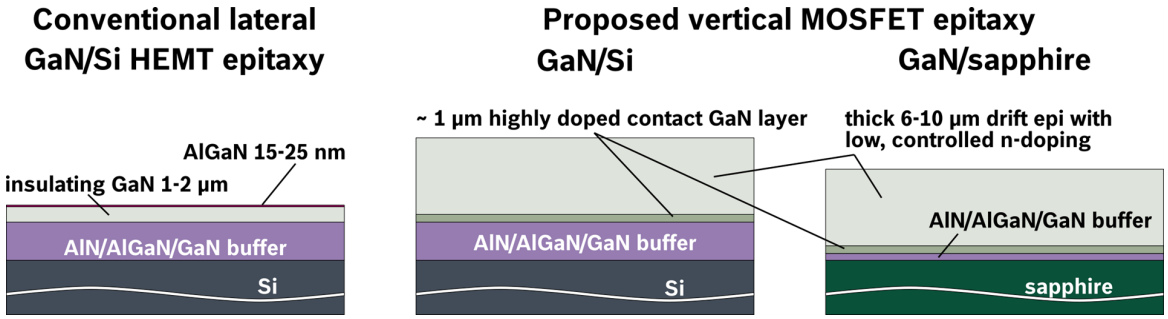

Figure 0.3: Comparison between epitaxy layers in HEMTs and proposed structure.

Not only silicon but also sapphire is interesting because even though it limits the diameter substrates to 100 mm, it offers a lower lattice mismatch to GaN. Anyway, a correct design of the buffer layer is necessary, because the bow generates cracks in the epi and that becomes even

more difficult, considering that carbon acts as a trap center for the donors. In addition, the dislocation density in the drift layer should be minimized because it could create alternative paths for leakage currents with a consequent need to lower the blocking voltage. The substrate of a wide 300 mm diameter, if Si is addressed, requires a MOVCD reactor compatible with crystal growth in Si, which would be useful for all WBG technologies. If a sapphire substrate is explored, its removal becomes necessary because of the low conductivity of the substrate that makes it unfitting for power semiconductors.

0.3.2 Development of low-cost vertical GaN transistor technology

As already explained in the previous sections, vertical structures offer higher power density capabilities. Lateral HEMTs would require a very large chip area in order to increase the blocking voltage, since this variable is dependent to the length of the drift region, which is oriented horizontally. Even admitting the larger chip area of the drift region, the on-resistance, R_{on}, would increase drastically as a consequence. On the other hand, a vertical structure with the thickness of the drift region can be increased while maintaining the same R_{on}. Moreover, a vertical voltage drop over the buffer layer and the insulating layer of HEMTs causes premature failure due to the generation of dislocations. That is why HEMTs are usually de-rated. Furthermore, HEMTs exhibit very low short circuit withstand time (SCWT), < 500 ns, [1], which would require the implementation of expensive and chip-near short circuit protection. Especially for high voltage applications of traction inverters, where the DC-link is between $400 - 800$ V, SiC remains the only WBG solution, considering existing technologies. Most of these traction applications are driven by efficiency; instead, for the majority of electric cars with a lower DC-link voltage, cost becomes the drive of the application and since SiC MOSFETs require high temperature processes to be produced over a small wafer of 150 mm, GaN on Si becomes interesting. The reduction in cost is proportional to the reduction in the substrate; see Fig. 0.4. The development of vGaNs instead of SiC would be beneficial to the Independence by non-European suppliers, too. Because different WBG substrates such as GaN are even more expensive and not available in relevant sizes, vertical structures remain the best option. It has been demonstrated that a higher switching speed can be achieved, compared to SiC transistors [2]. This makes vGaN very interesting for high power density applications. Furthermore, avalanche problems have never been observed on vGaN and some results from the state of the art, [3], [4], seem promising in terms of blocking voltage and R_{on}.

Attention must be paid to the space charge limited current, which is an induced leakage current

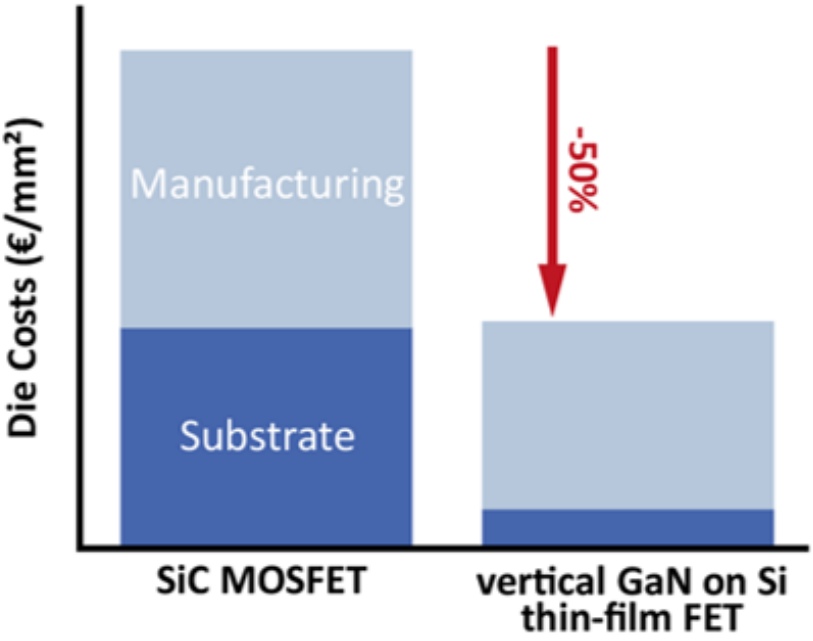

Figure 0.4: Die-cost reduction awaited with the YESvGaN technology.

and is the main cause of breakdown. Because the GaN epi is thick, it should have the lowest possible defects concentration. The main defects formation process must be considered. Different MOSFETs architectures can be explored, even FinFET with a sapphire substrate with the new YESvGaN technology, see Fig. 0.5. Development of new processes, such as Mg-implantation for p-doping should be explored.

0.3.3 Membrane power transistor technology

Because lattice and thermal mismatch exist in heteroepitaxial vGaN transistors grown on Si or sapphire and these substrates have higher resistance and low conductivity, the currents are also allowed to flow vertically. The final result is a thin semiconductor membrane directly connected to the drain metal: challenges arise in terms of safe handling of thin fragile transistors and proper backside metallization. The semiconductor should have negligible parasitic resistance from the backside contact. These parts of the project take care of developing a proper contact and metallization to achieve optimum current flow and low parasitic resistance as well as the development of a proper laser lift-off technology to remove the substrate. Even though silicon and sapphire techniques to substrate removal are well-known, they have never been applied to a vGaN, so they represent a term of innovation. At the same time, the proper geometry for the backside structure must be found.

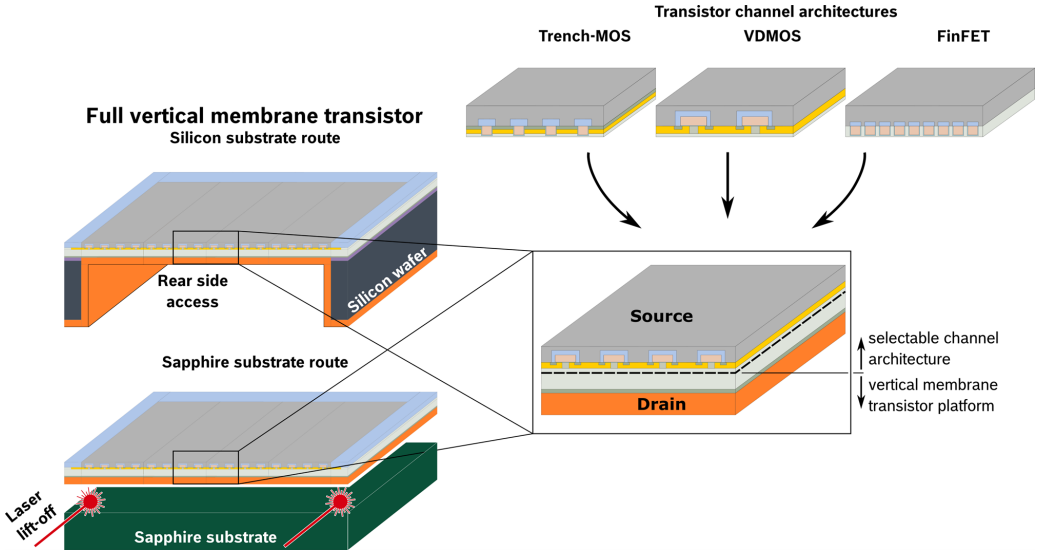

Figure 0.5: Possible structures of FETs with YESvGaN approach.

0.3.4 Assembly and interconnection technology for membrane GaN power devices

Regarding the assembly and interconnection technologies (AIT) for new vGaNs, it is required to enable robust module designs for vertical GaN transistors with a thickness of 10 µm and the development of thermal and thermo-mechanical simulation models for vGaNs. Lifetime and test results on these devices should also be made. Proper AIT technology is necessary to properly exploit the high temperatures of the WBG materials. In fact, GaN is stable above 250 °C: at this temperature it is more likely that the bonding wires melt. AIT should suit the application and particularly allow a reliable heat dissipation, that avoids excessive temperatures for the components, the insulation materials and the interconnection layers. Considering also the increased switching frequency, it is important to ensure reliability: electro-thermal simulations as well as the analysis of the heat flow through the chip or the wafer should be carried out. Also, for this package, a trade-off between AIT cost and their effectiveness should be found: a well-established technology such as Al thick wire bonding is not suitable for thin membranes, since they would be damaged, but new AIT methods should account for high-volume manufacturing of the chips. For both GaN in Si and GaN in sapphire, several bonding techniques with limited pressure and temperature should be explored to preserve the membranes. Nano-wired technologies are among the promising ones. The silver metallization of the two parts that should be bonded would allow a reduced particle contamination, since, differently from silver sintering, there would not be Ag paste between the soldered parts, see Fig. 0.6.

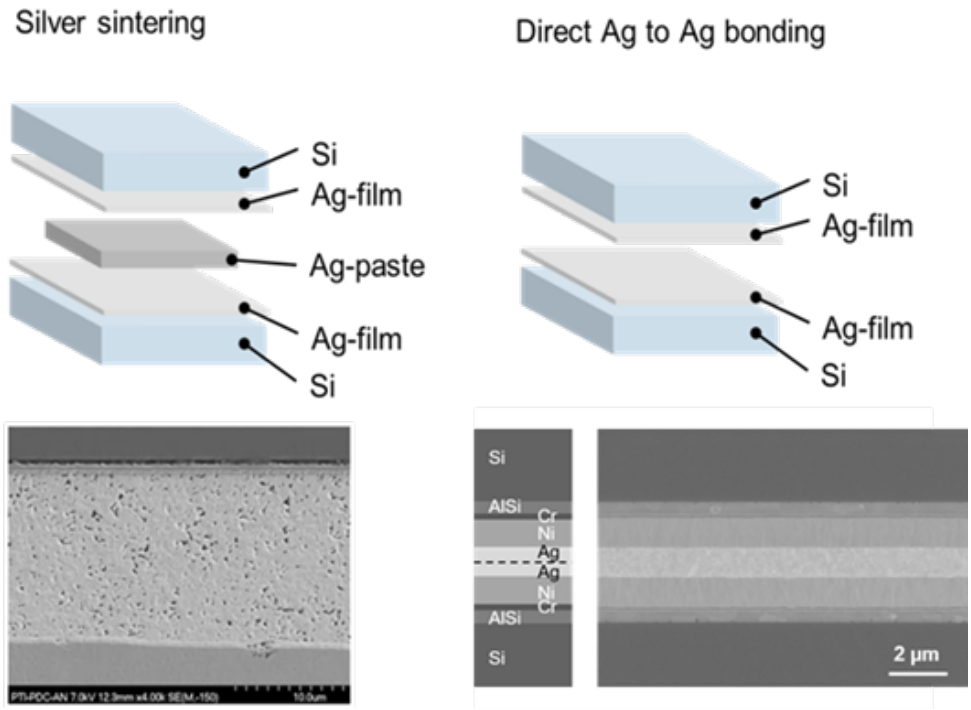

Figure 0.6: Difference between the Ag sintering (left) and the direct Ag-Ag bond (right).

The AIT also includes research on ceramic embedding to exploit the high temperature capabilities of GaNs. The final issue of this WP is the matching between simulations and measurements of R_{th} and Z_{th} throughout active and passive thermal cycling tests. The chips should also pass thermal shock tests.

0.3.5 Realization of demonstrators for power electronic systems with vGaN

The realization of demonstrators with vGaN is part of the duty of WP6, which Raw Power and UNIMORE are part of. Since the aim of the project is to establish the whole value chain for vGaN transistors, the development of high-efficiency WBG power modules is an important task in the project. vGaN is expected to substitute SiC MOSFETs in high voltage applications when high switching frequencies are required to lower the volume of the passive components, because the supply of the silicon or sapphire substrate would be easier and cheaper than that of existing WBG devices. Some fields of applications are more interesting than others, such as:

- Three-phase PFC converters.
- PV inverters.
- Resonant converter with soft switching commutation.

- On-board and off-board chargers.

Demonstrators of those kind should be built with vGaNs. The reason of interest for PV inverters with vGaN is more strategic and mission related than technical. One of the partners (Raw Power S.r.l.) wanted to explore a branch of power electronics different from the industrial, and the project itself had a preference for an environmental approach. Before the realization of power converters, simulation on different environments, such as PLECS, for example, would be essential to compare existing technologies (Si or SiC) with the new vGaNs. The same comparisons should be made by testing the converters directly. The devices themselves should be tested to obtain the static and dynamic characterization of these devices and publish preliminary datasheets. For sure, a lateral research on the gate drivers that need to adapt to very high switching speed and to the new devices will be useful in the future. Test efficiencies should be performed to prove the benefits of adopting GaNs instead of SiC in the end. Apart from the aforementioned problem of the adaptation of the gate drive circuitry, it should be pointed out that the usage of WBG components would require the adaptation of the whole system. In fact, GaN MOSFETs are capable of a very high switching frequency, which is reduced in many traction applications to ensure safe operation and reduce EMC irradiation. Especially motor insulation suffers high dv/dt. Future developments will account a better immunity to this phenomena. At the same time, faster computational micro controllers will be necessary or different type of control supported by FPGA would be necessary to fully exploit vGaNs. The advantages of employing WBG devices would be in lowering the volume and weight of passive components, such as inductors and capacitors, and the volume of some systems, such as DC chargers (increase of the power density). Furthermore, energy savings in all infrastructures, due to higher efficiency, would also be a benefit. Moreover, due to the low reverse recovery time, [5], even lower than existing SiC Schottky diodes, vGaN modules can be applied to electric drives, where reverse conduction is needed, both for inverters and DC/DC converter. The increase in power density is expected to be very significant. The first move in the project has been the realization of a digital-twin of an all-SiC half-bridge module, and its efficiency characterization in order to have a benchmark for comparison with vGaN was not available until this day. The project ended in October 2024 and the last achievement was the realization of a low voltage (100 V) buck converter demonstrator with vGaNs. Although the first samples of vGaNs on a Si substrate were produced, it was not possible to overcome or compensate for the generation of defects and operate the devices at the aimed voltages (800-1200 V).

0.4 References

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1. Switching Loss Model for SiC MOSFETs Based on Datasheet Parameters

1.1 Introduction

1.1.1 Motivation

As mentioned in the previous chapter, the YESvGaN project aimed to develop a new class of vertical GaN devices at the cost of traditional silicon devices. Raw Power and UNIMORE were responsible for the conceptualization and testing of the power converter that employs these WBG devices. At the same time, it was equally important to compare their performances with more widespread SiC devices.The idea of developing a switching losses model for SiC MOSFETs was born from these concepts and laid the foundations for this work. Industries could also benefit from an accurate losses model for WBG transistors, since it would allow predicting the converter efficiency under different operating conditions and making a first thermal design of the heat sink. It is worth stating that although this work was perpetuated within the YESvGaN project, this chapter is an original contribution of the author and the research group he belonged to at the University of Modena and Reggio-Emilia. However, the design of the all-SiC half-bridge board was made by Raw Power S.r.l. and Aurel S.p.a.. The first company gently borrowed the instrumentation for the measurements and supported the tests.

Generally, it can be stated that advanced modeling and simulation of electrical equipment is a key issue in the development and design of high-efficiency power converters for industrial and automotive applications. The constant growing interest in SiC-based devices is a natural result of their better merit figures compared to traditional Si-based solutions [1]–[3]. The adoption of SiC devices typically allows for a significant increase in both efficiency and power density because of their faster switching times and reduced conduction losses. Moreover, they can also operate at higher temperatures [4]. Even though the advantage on the performance side is clear and sound, the increase in power density provokes a rise of the thermal stress on SiC MOSFETs, which leads to a decrease in system MTTF (Mean Time To Failure) without appropriate monitoring of losses and device temperature. Since the junction temperature and

its fluctuation are responsible for the thermal aging and failure of the transistors, it is essential to monitor this physical quantity. A virtual sensor, especially, allows to estimate the junction temperature both online under a real operating condition and offline if the converter/inverter behavior and load profile are known beforehand, avoiding the need for thermocouples. These sensors are also less reliable in high-end applications with bare-die components, since they cannot be placed on the devices, but close to them. Because the temperature depends on the thermal chain between the device and the ambient temperature and on the power dissipated, a proper estimation of the transistor losses represents the first and most important step of the lifetime evaluation. Afterwards, several lifetime models and procedures already exist in the literature for traditional IGBT devices [5]–[7]. Similarly, some were developed for SiC MOSFETs: authors of [8] presented a great overview of the state-of-the-art. Considering also that in high power applications, an error of 1% on the efficiency estimation could significantly impact the heat sink design and the online evaluation of the thermal status, the importance of estimating the power losses of a SiC MOSFET becomes evident.

1.1.2 Overview of the topic

In this framework, the evaluation of the switching losses remains the most challenging task. Therefore, in recent years, several authors have focused their efforts on the development of a model that could estimate them [9]–[24]. An old and well-established model such as the one presented in [9] is very easy to understand and implement; however, it lacks precision due to the strong approximations made on the gate-drain capacitance and on constant rise and fall times. Others, such as those in [10], [11] and [12] are very complete but require preliminary measurements to derive the dynamic characteristics. Some take into account the effects of the short-channel and the drain-induced lowering barrier (DIBL), but they require a single-pulse test to obtain the saturation characteristic [11], [12]. Although this approach is formally correct, it requires a dedicated setup for parameter extraction and additional time, which may be very impactful for several companies approaching a SiC power converter design. The authors of [13] made a great effort in the analytical derivation of the turn-on losses. However, even though turn-on losses are predominant, turn-off losses are not negligible. Other articles focused on the influence of a single parameter on switching losses, charge and discharge C_{oss} in this case, which is relevant for the computations E_{on} and E_{off}, but introduces a further level of complexity, which is secondary in the total computations E_{tot}, [14]. Some numerical analytical models based on datasheet parameters already exist in the literature, [15] and [16]. They are

either mathematically challenging [15], or they make strong assumptions about the equivalent transconductance and capacitance [16]. In both cases, it is not clear how to estimate the parasitic inductances without doing any measurement. These models work well with discrete SiC devices in very standard packages, in this way these lumped parameters can be assumed from similar part numbers, but for bare-die components or non-standard packages, additional measures would be mandatory. The authors of [17] focused on reverse-recovery estimation, but their method also requires preliminary measurements. The same goes for [18], who adapted the model for a specific condition (quasi-zero turn-off losses). Moreover, their procedure also requires one to perform previous measurements. Some papers make a strong assumption on the temperature independence and also require us to compute some dynamic characteristic [20]. The works in [10]–[18], [20] are all num-analytical models (NAMs) as the one presented in this chapter; in addition to them, full-analytical models (FAMs) exist, [19], [21]–[24]. Other research that supposed linearized waveforms, especially the first two, also made the assumption of constant transconductance [19], [22], and [21]. The most complete FAM in the literature is the one derived by Hu and Biela in [23] and [24]. However, the mathematical complexity is extremely challenging and even though they provide good accuracy, they make step-wise approximations and the temperature independency assumption of the E_{on} and E_{off} losses. These assumptions become relevant as the switching frequency increases. In this chapter, a new NAM model is therefore presented, entirely based on the datasheet parameters, to estimate the switching losses of an all-SiC, SiC MOSFETs, and SiC Schottky diodes in antiparallel, application. This model is based on an iterative method, which can be solved in any language of common use: C++, MATLAB, Python, etc... This model considers all the possible information which are provided by the manufacturer: non-linear capacitance, channel-modulation mode, dependency of t_{ri} and t_{fi} on the load current. Nevertheless, this approach aims to be easy implemented by any company or research group, following the trend of a more efficient and widespread electric vehicle drive design and of a development of renewable energy systems with better performances. Moreover, none of the aforementioned model was validated considering the efficiency computation and the measurement uncertainty, which makes this work innovative in the literature perspective.

1.1.3 Chapter structure

In subsection 1.2 the SiC MOSFET switching losses model is explained in comparison with a simplified reference model, [9], one analytical model of similar complexity, [16] and a FAM model

[24]. Proceeding in subsection 1.3 the setup for the experiments is presented. In subsection 1.4 a digression on the expanded uncertainty evaluation is carried out: that is a needed premise to compare the measured efficiency with the one obtained in simulation. In the same subsection, results are resumed and compared with the aforementioned models. Finally, some conclusions and future development hints are given in subsections 1.6 and 1.7.

1.2 SiC MOSFETs switching losses evaluation

1.2.1 Introduction to the analysis

In this subsection, after presenting the well-known half-bridge architecture and its main parasitic components,a brief overview of the state-of-the-art of SiC switching losses estimation is presented. Then, the proposed model is detailed and shown in comparison with three existing ones: the simplified reference model found in [9], a NAM of similar complexity in [16] and a FAM in [24]. Afterwards, a paragraph is dedicated to the universality of the model and, the end of the subsection treats the junction temperature estimation based on the proposed model.

1.2.2 Half-bridge architecture and lumped parasitic parameters

The architecture under study consists of a half-bridge with two SiC MOSFETs and two SiC Schottky diodes in anti-parallel. The same architecture is tested in subsection 1.3. The electric model including all parasitic components is drawn in Figure 1.1 and is common throughout the subsection. Regarding the parameters: R_G should be intended as the sum of the external and internal gate resistance, further in this subsection $R_{G,on}$, total gate resistance during turn-on and $R_{G,off}$, total gate resistance during turn-off, are distinguished; L_s and L_d are the parasitic inductance of the source and drain, respectively; C_{GS}, C_{GD} and C_{DS} are the capacitance of the gate source, gate drain and drain source, respectively. V_{DC} is the DC Bus supply voltage and V_{dr} is the high-level voltage gate supply, off-state 0 V are applied to the control pins.

1.2.3 Overview of SiC switching losses models

As mentioned in the Introduction, several authors tried to model the switching losses in the past years, some of them also proved good compliance with the experimental tests, which had always consisted of a Double Pulse Test (DPT). However, each of them lacks either accuracy or results in excessive complexity. Moreover, most of them require some preliminary tests for

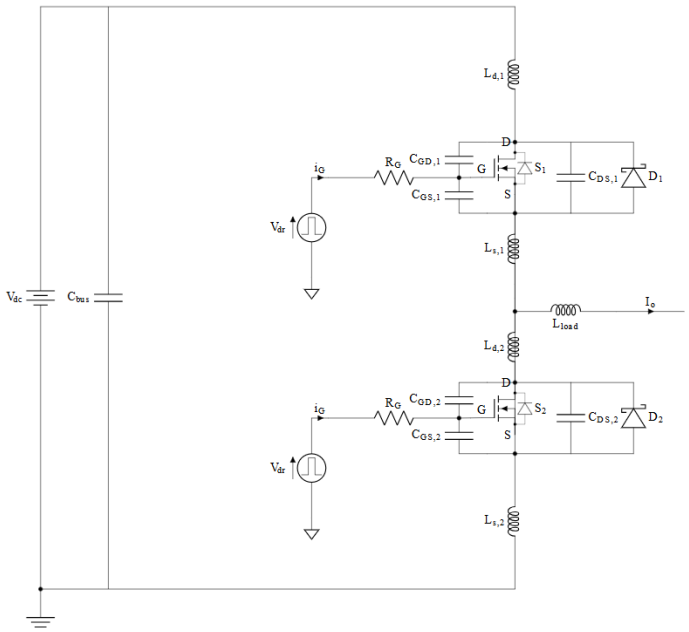


Figure 1.1: SiC MOSFET electric model with parasitic.

parameter extraction. It is believed instead, that a trade-off between accuracy and ease of application should be found for a switching losses model. Here, a brief summary of each model problem is done and the synthesis can be found in Table 1.1. The simplified model in [9] is better detailed later on in this subsection, since it will be used as one of the benchmarks in subsection 1.4: it consists of a well-established, but very raw model: C_{GD} is approximated as a step function and current rise and fall times are considered independent from the load current. The work in [10] presented a good summary of several factors influencing the switching loss mechanism; however, it demands to measure the dynamic characteristic of the MOSFET parasitic capacitances. Moreover, several variables, which are changed on purpose in the analysis are normally parameter of the already existing power board, such as the loop inductance L_{loop}. Other parameters are difficult to estimate: parasitic inductances L_s and L_d cannot be easily computed, usually a DPT is required or a very accurate LTSpice model, provided by the manufacturer. In most cases, this is not possible without building a dedicated setup. Furthermore, an error of 5% on the total energy losses is significant: especially at high switching frequencies, it leads to significant deviation on the efficiency estimation. The paper in [11] shows better accuracy, but maintains the same problem of the dynamic characterization of Q_{gd}, gate-drain charge, and of the transfer characteristic of the device, resulting in time and practical effort. Another research found in literature is very accurate but presents the same problem of previous characterization, [12]. In [13], a great insight on the energy turn-on losses computation is given,

but even if they represent the predominant part, the turn-off losses are not negligible. On the contrary, other works focus on the charge and discharge of the output capacitance C_{oss}, [14], which is a real physical phenomenon, but does not allow to better estimate the total losses, since the energy absorbed in one switching transient,E_{oss}, is then returned in the other: aiming to estimate the efficiency, this sophistication can be neglected. Authors of [15] and [16], which is detailed later on, provided a NAM based on datasheet parameters, even though the estimation of L_s and L_d and its difficulty are not well delved. First one showed a great accuracy, but high mathematically complexity. The work of [16] lacks a bit in accuracy, even though more understandable. On the opposite some models require preliminary tests to extract the lumped parameters, even though accurate [17]. Authors of [18] gave an interesting insight on the switching losses in the quasi-ZTL (zero turn-off losses) condition, but remained very specific and needs preliminary tests for the dynamic C_{GD} curve extraction. The exact same problem can be addressed to [20], where authors made the temperature independency assumption in addition. Full-analytical models as [19], [22] and [21] supposed linearized waveforms. These assumptions, added to a constant transconductance supposition allow faster evaluation, but reduce the models accuracy. Finally, Hu and Biela developed a FAM in [23] and refined it in [24] which is quiet accurate and based on datasheet parameters, even though it makes strong assumptions such as the temperature independency and the equivalent capacitance approximation. To reduce the computational effort, which is a goal for the models of this kind, it solves all the differential equations in a closed form, leading to a very challenging and almost prohibitive complexity. Also, this model is briefly described later on in the subsection.

Table 1.1: Overview of the state-of-the-art switching loss models.

Model	**Advantages**	**Drawbacks**
[9]	Very simple to implement	Very inaccurate
[10]	Formally complete	Discrete accuracy and preliminary tests
[11], [12]	Accurate	Dynamic MOSFET characterization
[13]	Detailed	Lack of E_{off} losses
[14], [15], [17]	Accurate and complete	Complex and preliminary tests
[18],[20]	Specific	Dynamic C_{GD} extraction
[16],[19],[22],[21]	Based on datasheet parameters	g_m and C_{GD} approximation, discrete accuracy
[23], [24]	Accurate and based on datasheet parameters	Extremely complex, step approximation of the capacitance and temperature independency

1.2.4 Simplified Reference Model

First, the simple model proposed in [9], based on the parameters of the data sheet, is taken into account. This model gives a rough estimation of the switching losses: in fact, it assumes a linear approximation for both voltage and current during turn-on and turn-off transients. During the current rise time t_{ri}, the gate source voltage v_{GS} increases linearly from the threshold voltage, V_{th}, to the Miller plateau voltage V_{mil}, which is considered constant and equal to the typical value reported in the data sheet. The same happens during t_{ri} in the turn-off transient: v_{GS} decreases linearly from V_{mil} to V_{th}. The model assumes that both the rising time of the curret, t_{ri} and the falling time of the current, t_{fi}, are constant and equal to their typical values, which can be found in the datasheet. The voltage fall time, during the turn-on transient, t_{fu}, is the time required to discharge C_{GD}. The discharging process starts when the drain-source voltage v_{DS} equals the supply voltage V_{DC} and ends when the MOSFET is conducting, i.e. when v_{DS} reaches the drain-source voltage of the MOSFET in the on-state $V_{DS,on} = R_{DS,on} \cdot i_D$, where $R_{DS,on}$ is the device on-resistance. At the beginning of t_{fu}, the voltage across C_{GD} is $V_{DC} - V_{mil}$ and at the end is $V_{DS,on} - V_{mil}$, therefore it is possible to consider the discharge of the capacitance at the constant current $I_{G,on}$ provided by the gate driver. This statement is not an assumption, since v_{GS} is clamped to V_{mil} over the period of time. The time t_{fu} could be estimated as in (1.1).

$$t_{fu} = \frac{\Delta V \cdot C_{GD}}{I_{G,on}} = (V_{DC} - V_{DS,on}) R_{G,on} \cdot \frac{C_{GD}}{V_{dr} - V_{mil}} \tag{1.1}$$

where V_{dr} is the voltage applied by the gate driver. One of the main issues is the value assumed by C_{GD} or C_{rss}, reverse transfer capacitance. Since this capacitance depends on the voltage from the drain-source, v_{DS}, the authors of [9] suggest a zero-hold interpolation based on two points: the first at $V_{DS,on}$ and the second at V_{DC} for the (C_{rss}-v_{DS}) curve found in the data sheet. A falling time is correlated with both C_{rss} values. The mean value between the two falling times is t_{fu}. Therefore, the switching losses E_{on} can be calculated as the area of a triangle, as can be seen in (1.2).

$$E_{on} = \frac{1}{2} V_{DC} I_0 \cdot (t_{ri} + t_{fu}) \tag{1.2}$$

where I_0 is the load current. A very similar approach is used to evaluate the voltage rise time t_{ru} and therefore to calculate the turn-off losses E_{off}, with two differences: the voltage applied by the gate driver is 0 V and the total resistance of the gate $R_{G,off}$ is generally different from $R_{G,on}$. The strongest approximation of this method is that of C_{GD} or C_{rss} and is well described by Fig. 1.2.

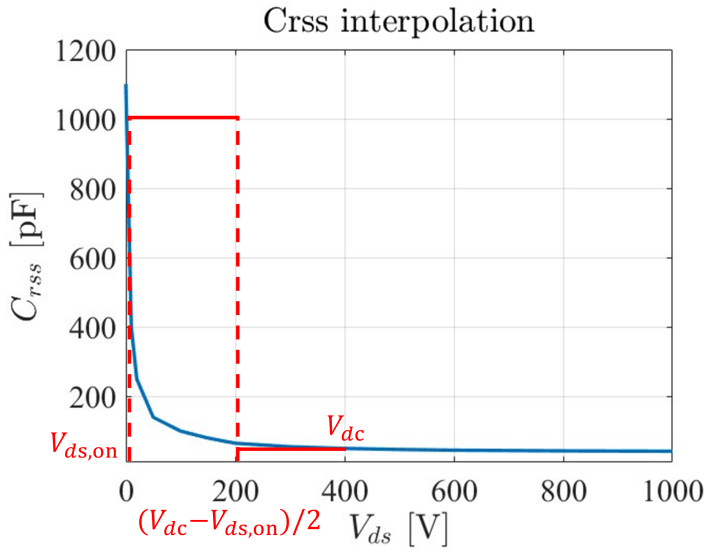


Figure 1.2: Approximation of C_{rss} [9].

As can be seen in subsection 1.4, the Infineon model leads to a significant overestimation of the switching losses. Although very simple, it lacks precision. The following subsection summarizes the num-analytical model of Christen and Biela [16].

1.2.5 Existing analytical model of similar complexity

In this subsection the steps employed by authors of [16] to evaluate E_{on} are briefly resumed, E_{off} are calculated in a similar way. Firstly, the input capacitance $C_{iss} = C_{GS} + C_{GD}$, the output capacitance $C_{oss} = C_{DS} + C_{GD}$, and the reverse-transfer capacitance $C_{rss} = C_{GD}$ are considered fixed at an equivalent value, calculated through the integral of each respective curve. Capacitances are then derived from algebraic operations of the three above. From $C_{oss,eq}$ an equivalent value is derived for the charge stored in C_{oss}, $Q_{oss,eq}$. Because C_{rss} plays an important role in the voltage switching transients, it is believed that this approximation is the main cause of the deviation with respect to experimental results, which can be appreciated in subection 1.4. Then, a second-order equation, if parasitic inductances L_s and L_d are considered, or a first-order equation, if not, is solved through a numerical method, for example the Newton-

Raphson method, in order to obtain a value for I_{oss}. I_{oss} is the current needed to charge C_{oss} during the current rise. A value for the transconductance g_m is then found [25].

Consider that I_{oss} is negative during turn-on and positive during turn-off, which means that the actual current flowing in the channel during the voltage drop is greater than the load current and vice versa during the voltage rise, [26]. Thus, the current rise-time t_{ri} and the voltage fall-time t_{fu} are calculated through (1.3).

$$\begin{cases} t_{fu} = -\frac{Q_{oss,eq}}{I_{oss}} \\ t_{ri} = -\ln\left(1 - \frac{Io}{g_m(V_{dr}-V_{th})}\right)(C_{GS}R_{G,on} + L_s g_m) \end{cases} \tag{1.3}$$

Finally, if the reverse-recovery phenomenon is neglected, E_{on} are calculated as in (1.4). A similar approach is followed for E_{off} losses.

$$E_{on} = \frac{1}{2}t_{ri}V_{DS,0}I_0 + \frac{1}{2}t_{fu}V_{DS,0}(I_0 - 2I_{oss}) \tag{1.4}$$

where $V_{DS,0} = V_{DC} - L_d(I_0/t_{ri})$ if parasitic inductances are considered, here $L_d = 0$. This model is implemented in MATLAB as the proposed one.

1.2.6 Fully Analytical Model

A merit of a fully analytical model is the computational time, that is reduced significantly, usually at the expense of the accuracy. However, very recently a fast and accurate FAM was developed by Hu and Biela, [23]-[24] at the expense of the complexity. Solving the equations of the switching transients in closed-form is mathematically challenging and even if the algorithm is provided, the implementation remains difficult. Moreover, its performances are inferior, even if slightly, to the proposed model. Switching intervals of turn-on and turn-off are divided in 6 parts and for each of these a contribution to the total losses is computed [24]. The model was always implemented in MATLAB, as the proposed one in the next subsection.

1.2.7 Proposed analytical model

1.2.7.1 Assumption of the proposed analytical model

This subsection delves into the proposed model, starting from its assumptions, which are only the necessary hypotheses to implement a fully-based datasheet model. Then its merits will be manifested. Here is the list of the three assumptions.

1. *Parasitic inductances L_d and L_s are neglected.* Because bare-die components are employed, typical inductance values of a standard package cannot be used. The overall inductance of the half-bridge could be estimated, but its distribution in all parasitic inductances is rather challenging. Considering that the PCB layout is executed trying to minimize these inductances as much as possible and that the highest switching frequency at which the half-bridge is tested is 80 kHz, it is assumed that they do not play a significant role. By the way, parasitic inductances mainly cause voltage overshoot during turn-off and voltage undershoot during turn-on [16]. If packages inductances are available they could be integrated in the model easily, if not consider that the switching delay caused by these inductances is only relevant for high switching frequencies: both t_{ri} and t_{fi} are affected in this case. Estimating the parasitic inductances due to the PCB layout would require separate simulations in Ansys, for example, which are out of the scope of this work. If external inductances are supposed to be symmetric and it is considered that $L_s = L_d$ include parasitic inductances due to the MOSFET package and due to the layout of the board, then t_{fi} and t_{ri} cannot be calculated from datasheet curves. Instead, for each I_0 load current value, these parameters would assume the following expression.

$$\begin{cases} t_{ri} = -\ln\left(1 - \frac{Io}{g_m(V_{dr}-V_{th})}\right)(C_{GS}R_{G,on} + L_s g_m) \\ t_{fi} = -\ln\left(\frac{V_{th}+V_{dr}}{V_{mil}+V_{dr}}\right)\cdot(C_{GS}R_{G,off} + L_s g_m) \end{cases} \tag{1.5}$$

   where C_{GS} is the weighted average value over the switching voltage range and g_m is the transconductance found in the datasheet.

2. *Reverse-recovery losses are neglected.* SiC Schottky diodes are placed in anti-parallel to the SiC MOSFETs and since they manifest a very low reverse-recovery peak current, I_{rr}, the assumption is acceptable. The omission of the reverse-recovery losses is compelling if SiC Schottky diodes are employed in anti-parallel SiC MOSFETs. If, instead, body-

diodes of the SiC MOSFET were used, these losses should be considered. In this case, works in [16] and [17] propose an effective way to compute the reverse-recovery losses. In particular, in [16] a set of formulae is derived from the physical model presented in [27], which could be numerically solved with the Newton-Raphson method. Energy loss due to reverse-recovery of the diode can be added to the losses which are computed with the proposed model.

3. *Drain-induced Barrier Lowering (DIBL) and short channel effect are neglected.* In the switching process and especially during current rise or fall, depending on which transient, turn-on or turn-off, is considered, the MOSFET operates in the saturation region. During this period of time, when powered by high DC bus voltages, the device experiences the DIBL effect resulting in an increment of the channel current for a given v_{GS} and in a reduction of the threshold voltage V_{th}. The complete expression of the channel current would be described by (1.6) as stated in [12]. With respect to the i_d-v_{GS} characteristic provided by the manufacturers at low and fixed v_{DS}, the real characteristic at higher bus voltages is shifted to the left and expresses a higher slope. Thus, the DIBL effect neglect implies an overestimation of the losses during current rise and fall. However, the estimation of λ requires an experimental characterization of the device, especially a single pulse test circuit [11], which would be out of the scope of the proposed model. The initial estimation of λ as described in [28] is not possible for most SiC MOSFET part numbers, and therefore the relation between V_{th} and v_{DS} cannot be derived from the datasheet. Therefore, the effect is neglected.

$$i_{ch} = \frac{K_p}{2} \cdot (v_{GS} - V_{th})^2 \cdot (1 + \lambda v_{DS}) \tag{1.6}$$

where i_{ch} is the channel current, K_p is the transconductance coefficient and λ is the short-channel coefficient.

Before proceeding, it should be clarified that the channel current is considered equal to the load current during t_{fu} and t_{ru}: $i_{ch} = i_D$. The actual current flowing in the channel during turn-on, when the voltage drops, is greater than the load current, because an additional current must be applied to discharge $C_{oss} = C_{GD} + C_{DS}$. The opposite happens during turn-off. As explained in [26], the actual E_{on} losses are greater than the ones measured throughout the use of a voltage and a current probe; in contrast, the measured E_{off} losses are lower than the measured ones.

However, if the aim is to evaluate the efficiency, this deviation is no longer significant since E_{oss} is stored but then completely released throughout the switching period: which allows one to simplify the model.

Apart from the aforementioned assumptions, the model aims to maintain the highest possible accuracy taking into account the main aspects of the switching process. Differently from the works in [10]–[15] and [17] it does not require prior measurements. As the research in [16], it employs an iterative method and consequently it avoids the direct resolution of differential equations. However, a step-by-step with feedback updating of the main variables is chosen instead of making strong assumption on the capacitances and on the transfer characteristic. Thus, obtaining, on average, a better accuracy than [24], while maintaining good understandability, avoiding closed-form expressions. The proposed model chooses to compute the main switching times, t_{ri}, t_{fi}, t_{fu} and t_{ru} with a step-by-step algorithm. A merit of the model is also to be efficiency-oriented, since it omits the calculation of E_{oss}.

1.2.7.2 E_{on} calculation

About the E_{on} switching losses, two contributions are distinguished: one due to the current rising and the other to the voltage falling. These processes are considered separately as in the simplified model. Before the current starts increasing, when $v_{GS} < V_{th}$, the channel current is negligible and therefore the power loss contribution of this time period. After the voltage drop v_{GS} goes from V_{mil} to V_{dr} but $v_{DS} = V_{DS,on}$, which is very close to zero, therefore this contribution to power loss is also negligible. Since during t_{ri}, it is true that $v_{DS} > v_{GS} - V_{th}$, the condition of channel modulation is considered true. The same formula explained in [25] and used in [16] can be employed.

$$i_{ch} = k_1 \cdot (v_{GS} - V_{th})^x + k_2 \tag{1.7}$$

where k_1, k_2 and x are three coefficients which can be found from a fitting of the $v_{GS} - i_D$ curve that is found in the datasheet. For the tested part number, these values can be extracted for

25 °C and 150 °C.

$$\begin{cases} k_{1,25°C} = 0.0638 \\ k_{2,25°C} = -0.06898 \\ x_{25°C} = 3.20758 \end{cases} \quad \begin{cases} k_{1,150°C} = 0.1935 \\ k_{2,150°C} = -0.08727 \\ x_{150°C} = 2.86988 \end{cases} \tag{1.8}$$

v_{GS} varies during t_{ri} and v_{GS} defines the trend of i_{ch} which is equal to i_D during this time period. The two main issues in the evaluation of the switching loss contribution of this time period are: the non-linear trend of i_{ch} during t_{ri} and the dependence of t_{ri} by the drain current itself. These difficulties in the power losses evaluation are solved employing a feedback algorithm. After defining a time-step $dt = 0.01$ ns, v_{GS} is initialized and V_{mil} is derived from (1.7) at load current I_0. The dv_{GS}/dt expression is also defined hypothesizing that v_{GS} changes linearly during t_{ri}.

$$\begin{cases} v_{GS} = V_{th} \\ V_{mil} = \sqrt[x]{\frac{I_0 - k_2}{k_1}} + V_{th} \\ \frac{dv_{GS}}{dt} = \frac{V_{mil} - V_{th}}{t_{ri}} \end{cases} \tag{1.9}$$

where I_0 is the load considered current, V_{th}, x, k_1 and k_2 are constant and assume different values if $T_j = 25$ °C or $T_j = 150$ °C and t_{ri} is initialized at the lowest available value based on the datasheet curve. A good amount of points can be extracted from the $(t_{ri} - i_D)$ curve in the datasheet and then a zero-hold interpolation is considered for this curve, i.e. the value of t_{ri} is constant in between two following samples. The number of points, if considerable, increases the precision of the model: in this case, 100 are taken in correspondence of the 100 possible load currents that were considered to build the model (from 0 A to 50 A with a step of 0.5 A). After that a *while* cycle starts and continues until either $v_{GS} < V_{mil}$ or $i_{ch} < I_0$ becomes false. Inside the cycle, if the new value of i_{ch} surpasses the mean value of i_D between one sample and the following one, both t_{ri} and dv_{GS}/dt are updated (1.10). At each iteration of the *while* cycle,

either if the above mentioned inequality is true or not, v_{GS} and i_{ch} are calculated: see (1.11).

$$\begin{cases} t_{ri}(n-1) = t_{ri}(n) \\ \frac{dv_{GS}}{dt}(n) = \frac{V_{mil}-V_{th}}{t_{ri}(n)} \end{cases} \tag{1.10}$$

$$\begin{cases} v_{GS}(n) = v_{GS}(n-1) + \frac{dv_{GS}}{dt}(n) \cdot dt \\ i_{ch}(n) = k_1 \cdot (v_{GS}(n) - V_{th})^x + k_2 \end{cases} \tag{1.11}$$

where n stands for the n^{th} iteration. The trend of i_D or i_{ch} during this time is not linear, therefore a numerical integration method needs to be adopted to evaluate the switching losses: the trapezoidal rule, (1.12), is employed. The time interval is always $dt = 0.01$ ns. The voltage across the MOSFET during t_{ri} does not change and remains equal to V_{DC}.

$$\begin{cases} v_{DS} = V_{DC} \\ \int_{t^*}^{t^*+dt} V_{DC} \cdot i_{ch} dt = V_{DC} \cdot \frac{[i_{ch}(t^*)+i_{ch}(t^*+dt)]\cdot dt}{2} \end{cases} \tag{1.12}$$

$$E_{on,t_{ri}} = V_{DC} \cdot \sum_{k=0}^{m-1} \frac{[i_{ch}(k) + i_{ch}(k+1)] \cdot dt}{2} \tag{1.13}$$

where $m \cdot dt$ corresponds to the effective rise-time. In this way, the non-linear trend of the channel current is considered. The other contribution to the switch-on losses is due to the voltage falling. To estimate the voltage falling time t_{fu} points are extracted from the $(C_{rss}-v_{DS})$ curve that is found in the datasheet. A curve fitting could be used, as in [17], but a zero-hold interpolation of the extracted points is simple and effective. The number of points should be significant and the sampling rate should be higher near the "knee" of the curve, in this case 68 C_{rss} values are taken. Since C_{rss} changes significantly along with v_{DS} a weighted average value

is calculated for t_{fu}. The following indexes are defined (1.14).

$$\begin{cases} l = \max_k \{v_{DS,C_{rss}}(k) | v_{DS,C_{rss}}(k) <= V_{DS,on}\} \\ h = \max_k \{v_{DS,C_{rss}}(k) | v_{DS,C_{rss}}(k) <= V_{DC}\} \end{cases} \tag{1.14}$$

where $v_{DS,C_{rss}}(k)$ is k^{th} sample of the reverse-transfer capacitance curve. After defining the extremes, t_{fu} is initialized considering that $C_{rss} = C_{rss}(h)$ is discharged at a constant current $I_{G,on}$, (1.15) and then dv_{DS}/dt is initialized as well (1.16).

$$I_{G,on} = \frac{V_{dr} - V_{mil}}{R_{G,on}} \tag{1.15}$$

$$\begin{cases} t_{fu} = \frac{(V_{DC} - V_{DS,on}) \cdot C_{rss}(h)}{I_{G,on}} \\ \frac{dv_{DS}}{dt} = -\frac{V_{DC} - V_{DS,on}}{t_{fu}} \end{cases} \tag{1.16}$$

where V_{mil} assumes the value calculated in (1.9). At each iteration of the *while* cycle, v_{DS} is updated and a variable c is increased of one unit to count the integer number of dt during which C_{rss} is considered constant to the sample value $C_{rss}(k)$ (1.17). Whenever $v_{DS} > v_{DS,C_{rss}}(k)$, k is decreased of one unit and c is reset to zero: this operation can occur until $k \geq l$ (1.18). Saving the value of $c(k)$ for each $C_{rss}(k)$ sample, the weighted average value of t_{fu} can be calculated (1.19) at the end of the cycle, when $v_{DS} = v_{DS,on}$.

$$\begin{cases} c(k) = c(k) + 1 \\ v_{DS}(n) = v_{DS}(n-1) + \frac{dv_{DS}}{dt}(k) \cdot dt \end{cases} \tag{1.17}$$

$$\begin{cases} k = k - 1 \\ c(k) = 1 \\ t_{fu}(k) = \frac{(V_{DC} - V_{DS,on}) \cdot C_{rss}(k)}{I_{G,on}} \\ \frac{dv_{DS}}{dt}(k) = -\frac{V_{DC} - V_{DS,on}}{t_{fu}(k)} \end{cases} \tag{1.18}$$

$$t_{fu} = \frac{\sum_{k=l}^{h} t_{fu}(k) \cdot c(k)}{\sum_{k=l}^{h} c(k)} \tag{1.19}$$

Assuming the linear falling of the voltage during this time, (1.20) represents the other contribution to the switch-on losses.

$$E_{on,t_{fu}} = \frac{1}{2} V_{DC} I_0 \cdot t_{fu} \tag{1.20}$$

E_{on} becomes the algebraic sum of the two contributes.

$$E_{on} = E_{on,t_{ri}} + E_{on,t_{fu}} \tag{1.21}$$

1.2.7.3 E_{off} calculation

The E_{off} losses also consists of two contributes: $E_{off,t_{ru}}$, due to the non-instantaneous voltage rising and $E_{off,t_{fi}}$, due to the current falling. The method employed to evaluate t_{ru} is the same as for t_{fu}, but equations in (1.15), (1.16), (1.17), (1.18), (1.19) must be re-arranged. The charging current for C_{rss} becomes (1.22), if a zero voltage is applied by the gate-driver. k is increased until $k \leq h$ and the *while* cycle stop condition is $v_{DS} = V_{DS,on}$.

$$I_{G,off} = \frac{V_{mil}}{R_{G,off}} \tag{1.22}$$

$$\begin{cases} t_{ru} = \frac{(V_{DC} - V_{DS,on}) \cdot C_{rss}(l)}{I_{G,off}} \\ \frac{dv_{DS}}{dt} = \frac{V_{DC} - V_{DS,on}}{t_{ru}} \end{cases} \tag{1.23}$$

$$\begin{cases} c(k) = c(k) + 1 \\ v_{DS}(n) = v_{DS}(n-1) + \frac{dv_{DS}}{dt}(k) \cdot dt \end{cases} \tag{1.24}$$

$$\begin{cases} k = k + 1 \\ c(k) = 1 \\ t_{ru}(k) = \frac{(V_{DC} - V_{DS,on}) \cdot C_{rss}(k)}{I_{G,off}} \\ \frac{dv_{DS}}{dt}(k) = \frac{V_{DC} - V_{DS,on}}{t_{ru}(k)} \end{cases} \tag{1.25}$$

$$t_{ru} = \frac{\sum_{k=l}^{h} t_{ru}(k) \cdot c(k)}{\sum_{k=l}^{h} c(k)} \tag{1.26}$$

It follows that $E_{on,t_{ru}}$ can be evaluated as in (1.27).

$$E_{off,t_{ru}} = \frac{1}{2} V_{DC} I_0 \cdot t_{ru} \tag{1.27}$$

In addition to t_{ri}, also t_{fi} varies along with i_D, therefore a step-by-step method is used as for $E_{on,t_{ri}}$. In this case, V_{mil} has already been calculated during the evaluation of E_{on} losses. In (1.28), the initialization of the variables is shown.

$$\begin{cases} v_{GS} = V_{mil} \\ dv_{GS}/dt = \frac{-V_{mil} + V_{th}}{t_{ri}} \end{cases} \tag{1.28}$$

A *while* cycle is always considered, that continues until $v_{GS} > V_{th}$ becomes false or $i_{ch} > I_0$ becomes false. Inside the cycle, if the new value of i_{ch} is lower than the mean value between one sample of i_D and the following one, v_{GS} and dv_{GS}/dt are updated. Firstly, t_{fi} is updated to the next sampled value and then dv_{GS}/dt is evaluated again. At each iteration of the *while* cycle, if the inequality mentioned above is true or not, the values are updated as for the switch-on losses, (1.11). Subsequently, $E_{off,t_{ri}}$ has the following expression.

$$E_{off,t_{fi}} = V_{DC} \cdot \sum_{n=0}^{m-1} \frac{[i_{ch}(n) + i_{ch}(n+1)] \cdot dt}{2} \tag{1.29}$$

E_{off} losses are then the sum of two contributes: (1.30).

$$E_{off} = E_{off,t_{fi}} + E_{off,t_{fu}} \tag{1.30}$$

The algorithm used for the calculation of the losses E_{on} is resumed in Figure 1.3 and can be implemented in MATLAB. In this figure, n is the index of the current values $I_0 = \{0, 0.5, 1.0, 1.5, ..., 50\}$ A and v is the index of supply voltage values $V_{DC} = \{0, 10, 20, ..., 100, 200, ..., 1000\}$ V. That is very similar to the one used to evaluate E_{off}. Consider that it is implemented for $T_j = 25$ °C and $T_j = 150$ °C. In Figure 1.4, the algorithm is explained graphically and the assumed switching transients are shown for the gate-source voltage and the drain-source voltage and current. Once the E_{on} and E_{off} matrices have been evaluated, they can be uploaded as a look-up table in PLECS to evaluate power losses due to the switching process in several simulating conditions, [29]. Efficiency results over the half-bridge architecture are shown in comparison with the experimental results; see subsection 1.4.

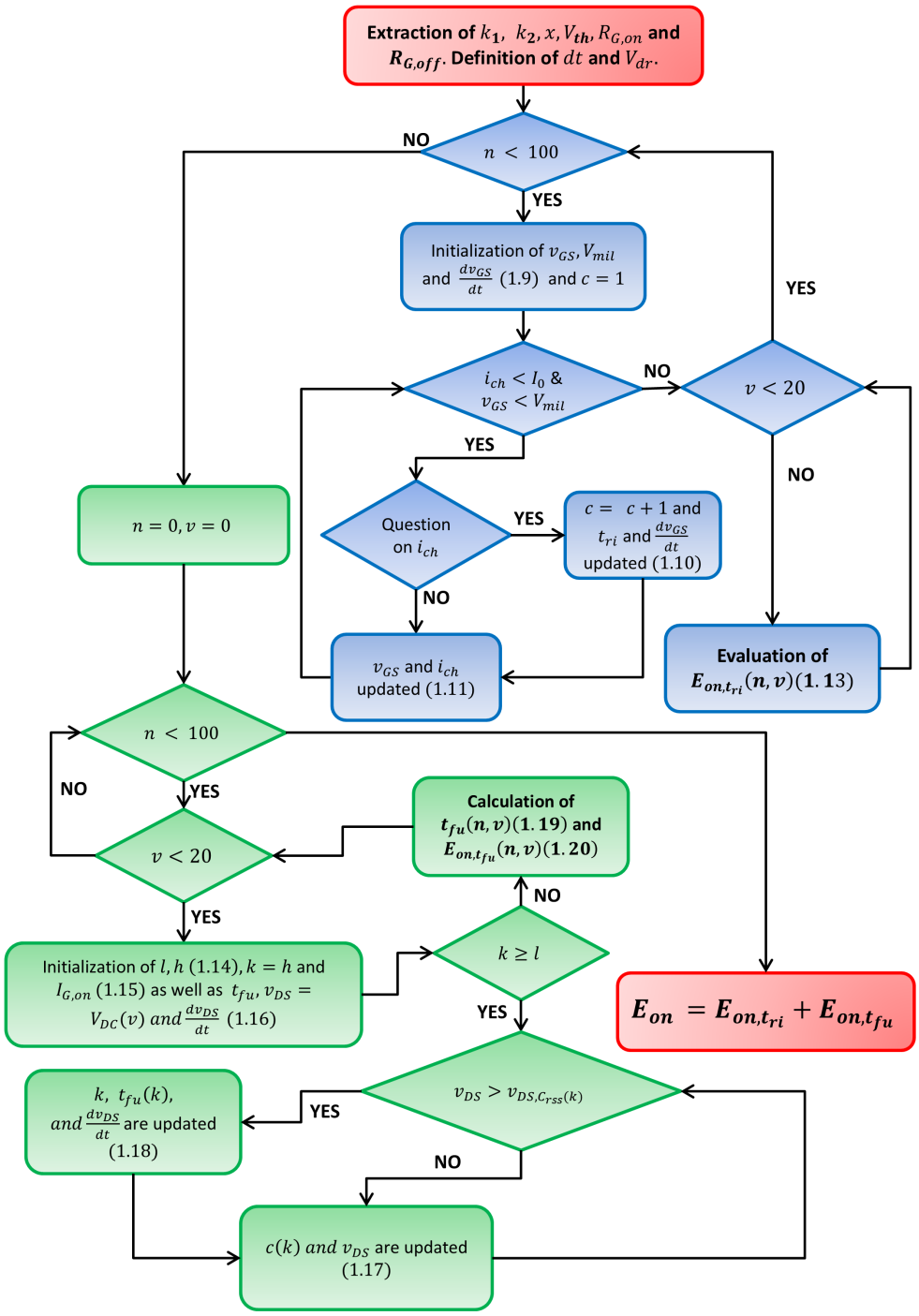


Figure 1.3: Flow chart of the algorithm used to evaluate E_{on}.

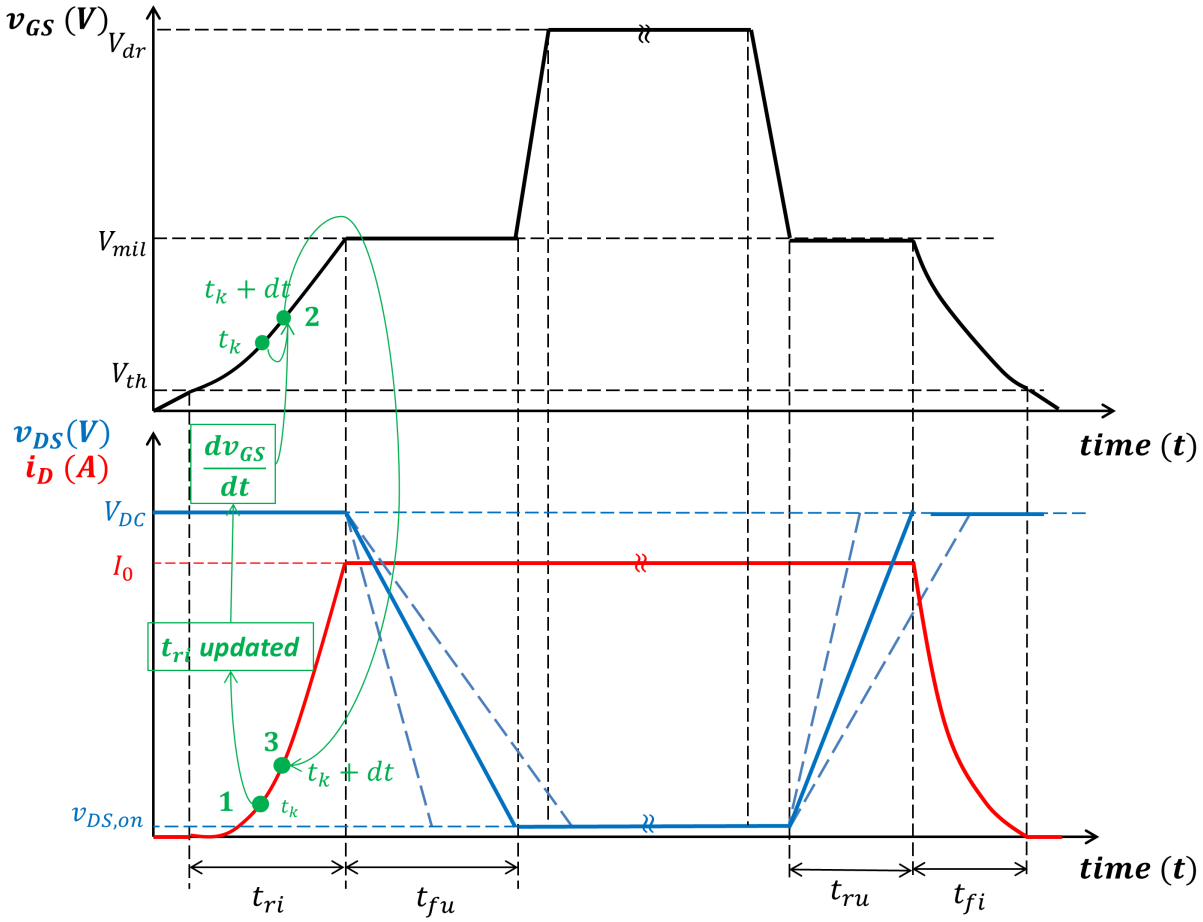
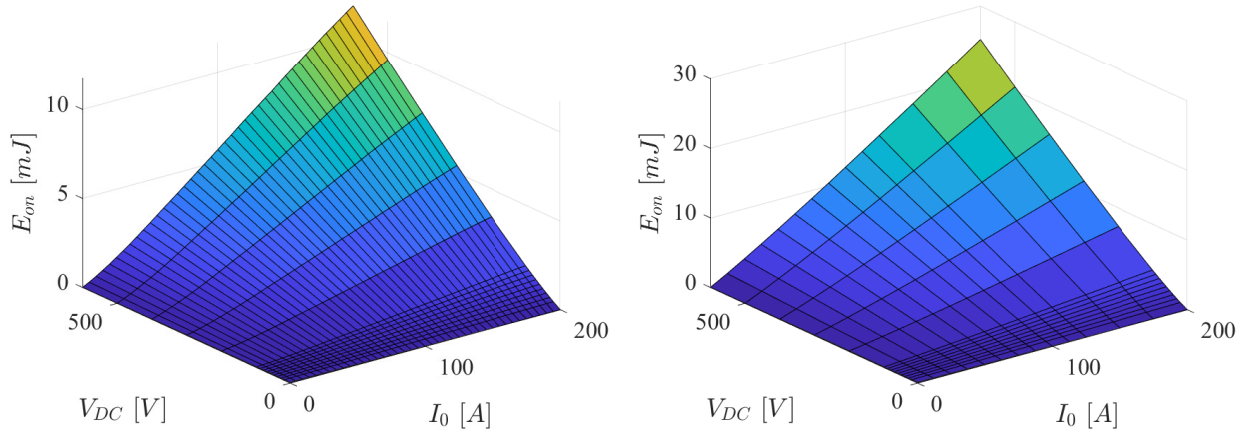


Figure 1.4: Switching transients assumed for the algorithm implementation.

1.2.7.4 Universality and further discussions on the proposed model

The proposed model is meant to be applied to any SiC MOSFET since it is not dependent on the individual part number technology: all the equations in the previous subsection do not include any reference to a specific topology. To further underline that, the algorithm was applied to two 2nd Gen. CoolSiC: IMW65R007M2H, [30] and IMW65R020M2H, [31]. These have the same blocking voltage, technology and package but very different R_{DSon}: 7 mΩand 20 mΩ respectively and switching losses. As shown by Figure 1.5, the algorithm results are coherent with the information provided by the manufacturer. Since it implies an iterative method, any development environment in C or C++ can be employed as a substitution of MATLAB, therefore also the applicability is notable. In this work an all-SiC board, SiC MOSFETs and SiC Schottky diodes in antiparallel, was employed. If MOSFET body-diodes were employed, reverse recovery should be considered: in this case, it is sufficient to add the calculations found in [16] or [17] at the end of the algorithm.



(a) E_{on} IMW65R020M2H **(b)** E_{on} IMW65R007M2H

Figure 1.5: Comparison of the Eon losses at Tj = 25° C between: (a) IMW65R020M2H and (b) IMW65R007M2H

1.2.7.5 Virtual Junction Temperature Estimation

Estimation of junction temperature is the first and most important step in evaluating the thermal stress and lifetime of the SiC MOSFET. If P_{loss} is the sum of the switching and conduction losses of a single device under a certain operating condition, it is sufficient to employ the turn-on and turn-off losses as look-up tables in the micro controller to derive the junction temperature T_j of the device. The process implicitly requires knowledge of the thermal chain between the junction and the environment. The expression of T_j is given in (1.31). The same formula is in open loop, but only because it is described in the easiest way and because this paragraph should be intended as a hint for future development. Indeed, both switching and conduction losses depend on the junction temperature, which is the output and the feedback.

$$T_j(t) = P_{loss}(t) \cdot [Z_{th,j-h}(t) + Z_{th,h-a}(t)] + T_{amb}(t) \tag{1.31}$$

where $Z_{th,j-h}$ and $Z_{th,h-a}$ are the thermal impedance from junction to heat sink and from heat sink to ambient. The first one is generally expressed as $Z_{th,j-h}(t) = Z_{th,j-c}(t) + Z_{th,c-h}(t)$ but only if the device comes in a package. Otherwise, if a bare-die part number is chosen in the application the two terms collapse in one. $Z_{th,j-c}$ can be derived from the part number datasheet curve, for the evaluation of $Z_{th,c-h}$ or $Z_{th,j-h}$, in case of a bare-die component, [32] can be used. Each thermal impedance can be represented as a Foster thermal RC network, thus

the explanation of the temperature dependency of these quantities. P_{loss} changes along with the operating condition and T_j, T_{amb} should be continuously updated, therefore they are also time-dependent. If an operating condition is maintained until a stable temperature is reached, only the thermal resistances are significant and the expression in (1.31) transforms into (1.32).

$$T_j = P_{loss} \cdot [R_{th,j-h} + R_{th,h-a}] + T_{amb} \tag{1.32}$$

The switching losses model calculates E_{on} and E_{off} from the load current and the bus voltage, a commercial current sensor such as the coreless TLI4971, [33], from Infineon employed for the board tested in this work can be used. The bus voltage can instead be measured with a simple voltage divider. Since these physical quantities are important for all electric power drive units or converters connected to the grid, the implementation of the virtual temperature sensor based on the proposed NAM model is straightforward and requires a sustainable effort. This power losses model along with a detailed analysis of the thermal resistance R_{th} and C_{th} parameters allows to make a more realistic lifetime estimation: in fact, in papers like [7], the datasheet turn-on and turn-off energies are used. A work that is not reported in this thesis and that is now under review, employed this switching losses model for the lifetime estimation of a low-voltage high-current inverter. A future work in this direction will also be done to extend the work of chapter 2. Because the virtual junction temperature estimation of a power semiconductor is not the focus of this chapter and the author himself did not delve operatically into this topic, here are some comments on how to obtain the thermal impedances Z_{th}. Each thermal impedance $Z_{th} = Z_{th}(t)$ is time-dependent. For a period of time that is long enough, $Z_{th} -> R_{th}$ (steady-state). Instead, for transient intervals, the thermal capacitance C_{th} also plays an important role and, consequently, for lifetime modeling. Each Z_{th} could be estimated using manufacturer data, if no prior measurement is possible. However, the actual values usually differ from the declared ones. Therefore, a suggestion on how to evaluate each impedance is given below.

- The junction-to-case impedance $Z_{th,j-c}(t)$ can be decomposed into a RC network with three different R_{th} and C_{th}. In this case: STMicroelectronics, Vishay, Infineon, and many other manufacturers already provide accurate $Z_{th,j-c}(t)$, so the suggestion is to employ the curve, which is found in the datasheet.

- The case-to-heatsink impedance $Z_{th,c-h}(t)$ can be calculated applying a constant load

(high-side MOSFET is always turned on). Then with two thermocouples, one placed on the heatsink and one the case, it is possible to calculate the thermal resistance with the following formula, once steady-state is reached.

$$R_{th,c-h} = \frac{T_h - T_c}{P_{diss.}} \tag{1.33}$$

where $P_{diss.} = R_{ds,on} \cdot I_0^2$. $R_{ds,on}$ can be taken from the datasheet: $R_{ds,on} = R_{ds,on}(T_j, I_0)$ or $v_{ds,on}$ can be measured. Monitoring $v_{ds,on}$ corresponds to scanning a thermo-sensitive electrical parameter (TSEP). This is the methodology used in some papers in the literature to estimate the junction temperature on-line and follow the degradation of the MOSFET [34], [35]. The evaluation of $C_{th,c-h}$ is, instead, harder. Once $R_{th,c-h}$ is known, the same measurement should be repeated, but with a higher temperature sampling frequency, and $C_{th,c-h}$ is calculated as in (1.34).

$$C_{th,c-h} = \frac{\tau_{th}}{R_{th,c-h}} \tag{1.34}$$

where τ_{th} is the thermal time constant which can be extracted from the measurement. Consider the order of magnitude for the transients in the case to be ms.

- The heatsink-to-air impedance $Z_{th,h-a}(t)$ can be calculated with the same approach described before, placing the other thermocouple in air, close to the heat source. Because transients are on the order of s or min depending on the size of the heatsink, estimating $C_{th,h-a}$ should be less challenging.

The analytical calculation of these quantities is acceptable if the researcher is working on estimating the useful life of the semiconductors. Otherwise, the experimental approach is suggested.

Finally, the reader should bear in mind that the most accurate method of evaluating the power losses of a converter is probably the colorimetric method [36]. However, building a proper setup and calibrating the calorimeter itself is not a trivial operation [37] and becomes impractical for most companies. The approach followed here, is different as already explained.

1.3 Experimental setup

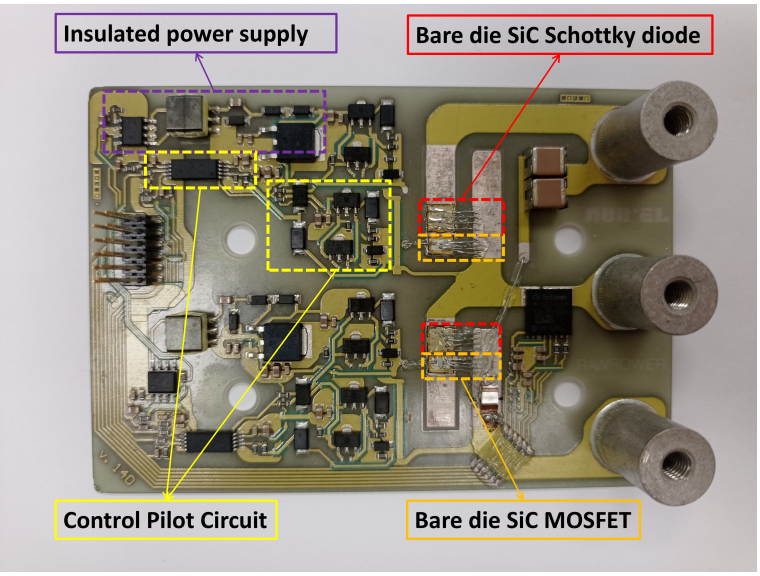


Figure 1.6: All SiC Half-bridge module

The conversion unit has been realized as a PCB, produced over a ceramic support that also contains the insulated power supply for the Control Pilot Circuit. The components are: two SiC MOSFETs s4101, [38] and two SiC Schottky diodes s6305, [39], placed in antiparallel, see Figure 1.6. The PCB has been assembled over an aluminum heat sink. A *STMicroelectronics* controller has been used to pilot the driver and select both the work frequency and duty-cycle. The input filter consists of two film capacitors, one of 56 nF and one of 47 nF, directly placed in parallel to the DC supply voltage source. In addition, three film capacitors (two of 56 nF and one of 1.5 µF) are placed in parallel with three electrolytic capacitors of 470 µF between '+' and '-' of the half-bridge. The DC power supply provides the constant voltage to the half-bridge: experiments are carried out at $V_{DC} = 400, 450$ and 500 V, the LC output filter consists of a ferrite core inductor of 1.2 mH and a group of three capacitors, one ceramic and two electrolytic of 1.5 µF and 470 µF respectively. The resistive load is a parallel of two 47 Ω resistances. Voltages, currents and powers are acquired after the bulk input filter at the input and before and after the LC filter at the output with a *PPA 3500* power analyzer, manufactured by *N4l*, in order to measure the converter efficiency before and after the LC output filter: both measures are needed to compute the filter AC losses. The wiring has been made with short cables to enhance impedance matching and reduce noise during acquisition. The wiring schematic is shown in Figure 1.7. In Figure 1.8, the entire measurement setup is shown, apart from the resistive load, which consists of two 47 Ω resistances placed in parallel.

The results of the experiments take into account the expanded uncertainty, and they are shown in subsection 1.4.

1.4 Comparison with the experiments

In order to validate the analytical model for the switching losses calculation, the measurement uncertainty is evaluated for several operating conditions. The aim of this calculation is to define a proper way to compare simulations and experiments. Specifically, efficiency estimation is considered competent if the simulation result is included between the range defined by the *expanded uncertainty* around the mean measured efficiency. Therefore, a series of 11 measurements is conducted on the half-bridge module. Each of these measurements consists of 10 samples, where the RMS voltage, the RMS current, the power in the three channels and the frequency only in the second channel to which the LC filter is connected are acquired. This procedure is repeated for the following duty-cycles: $0.2, 0.3, 0.4$, 0.5 and 0.7 as well as for 3 switching frequencies: $40, 60$ and 80 kHz. In this way, for each simulation result, there is a respective experimental range. It is believed that a proper estimation of the *real unknown value*, or the center of the range, is represented by the mean value over the 11 runs of the arithmetic mean above each of the 10 samples. Then, it is possible to express the *A-type uncertainty* or the *repeatability deviation* as in (1.35), following the guideline in [40].

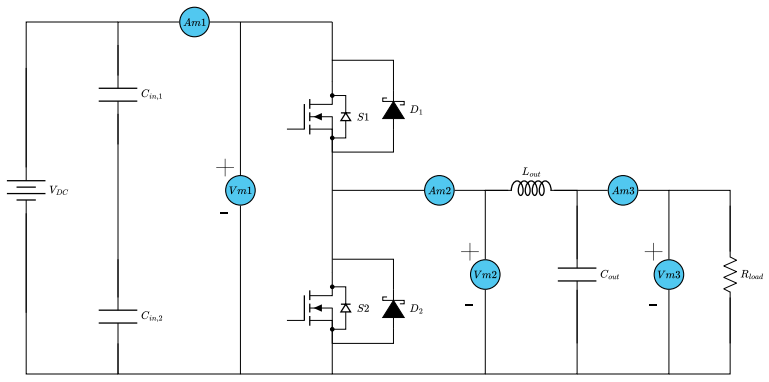


Figure 1.7: Wiring diagram

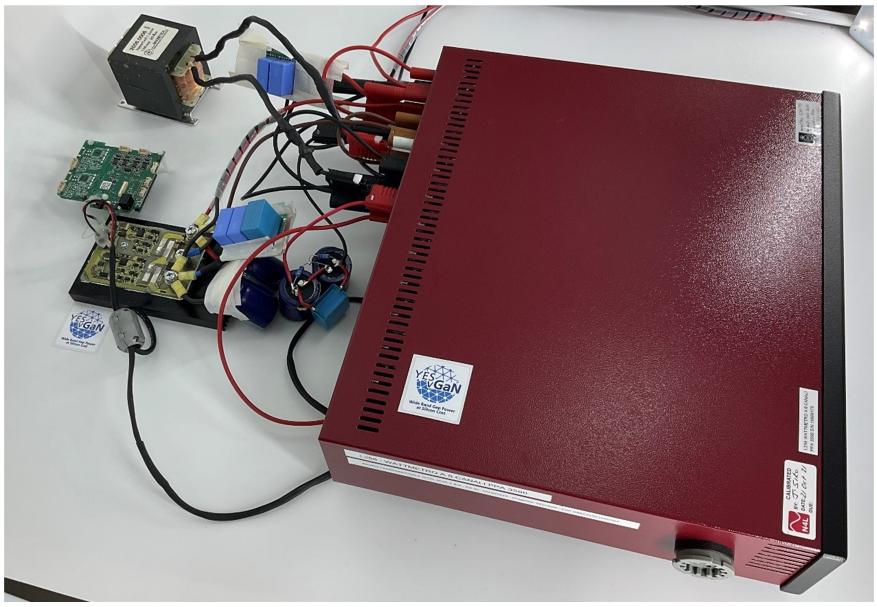


Figure 1.8: Measurement setup.

$$u_{A,j,f} = \sqrt{\frac{\sum_{r=1}^{n}(\overline{\overline{x}}_{\eta,j,f} - \overline{x}_{\eta,r,j,f})^2}{n-1}} \tag{1.35}$$

where n equals 11, the number of runs, $\overline{x}_{\eta,r,j,f}$ is the mean efficiency among the 10 samples of the r^{th} run, j is the duty-cycle index, f is the switching frequency index and $\overline{\overline{x}}_{\eta,j,f}$ is the mean value of the efficiency over the 11 sets of measurements for a specific duty-cycle and switching frequency. The computation of the *B-type uncertainty*, instead, depends on the measurement instrument. Since the PPA 3500 power analyzer is used for the measurements, the authors refer to the user manual [41] to define this bias. For both input and output power, the accuracy on the power measurement is expressed by (1.36).

$$u_{max,W_r} = \frac{\left(0.1 + \frac{0.1}{PF} + \frac{0.01 \cdot f_{sw}}{PF}\right) \cdot W_r + 0.05 \cdot V_p I_p}{100} \tag{1.36}$$

where V_p and I_p are the voltage and ampere range of the instruments and W_r is the measured power, which can be either substituted with W_{in} or W_{out}. u_{max,W_r} represents the maximum deviation in [W] from the mean measured power. PF is the power factor, that can be simply evaluated by dividing the measured power by the product of the input voltage and the input current and f_{sw} is the switching frequency expressed in kHz, $40, 60$ or 80. Once the maximum deviations are found: $u_{max,W_{out}}$ and $u_{max,W_{in}}$, they are then put together to find the B-type

uncertainty for the measured output efficiency; see (1.37). The reason for $\sqrt{3}$ is the assumption of a uniform distribution of the systematic error.

$$u_{B,j,f} = \sqrt{\left(\frac{u_{max,W_{in},j,f}}{V_p I_p \sqrt{3}}\right)^2 + \left(\frac{u_{max,W_{out},j,f}}{V_p I_p \sqrt{3}}\right)^2} \cdot 100 \tag{1.37}$$

The compound uncertainty is considered as the square root of the two components square (1.38). Finally, the expanded uncertainty can be defined with a level of confidence of 95 %, therefore with a coverage factor $k_p = 2$, see (1.39).

Applying these formulae, it is possible to find a range values around the mean efficiency for every duty-cycle and switching frequency, which allows comparing the simulation results with measurements tests.

$$u_{comp,j,f} = \sqrt{u_{A,j,f}^2 + u_{B,j,f}^2} \tag{1.38}$$

$$u_{k,j,f} = k_p u_{comp,j,f} \tag{1.39}$$

The uncertainty range is defined in (1.40) and it varies under different test conditions.

$$[\overline{\overline{x}}_{\eta,j,f} - u_{k,j,f}; \overline{\overline{x}}_{\eta,j,f} + u_{k,j,f}] \tag{1.40}$$

As shown in Table 1.2-1.4, simulation results are consistent with the experimental tests. The efficiencies estimated throughout PLECS show great compliance with the measurements at 40, 60 and 80 kHz. To compare this model with the state-of-the-art, three additional models have been investigated. The first is the old simplified Infineon model [9], the second is a NAM model developed by Christen and Biela [16] and the last is a FAM model, initially developed in [23] and then refined in [24] by Hu and Biela. These, as the one presented in this work, are based on datasheet parameters. As stated at the beginning of this work, other authors introduced further levels of sophistication at the expense of carrying out some preliminary measurements.

Since the proposed model is entirely based on the information provided by the manufacturers, a comparison with those would be beyond its aim of avoiding measurements. To develop the reference models: first, a MATLAB script was built, then the resultant losses were uploaded in the thermal description of the device in PLECS and as a last step, simulations were carried out. To make a comparison between the proposed model and the existing ones, four KPIs were used. Each KPI should be intended per switching frequency f_{sw} (Table 1.2, 1.3 and 1.4).

- The number of simulation results $n°$, which lie in the uncertainty range defined around the measured efficiency.

- The mean absolute error $\overline{e}$, which represents the average displacement with respect to the measured value (1.41).

- The mean absolute percentage error $\overline{e}_{\%}$, which is the unsigned average displacement normalized over the measured value (1.42). This error suggests the average displacement with respect to the test itself.

- The Modified Mean Absolute Percentage Error $MMAPE$, (1.43), is a well-known relative measure of the forecasting accuracy [42].

$$\overline{e} = \sum_{d} \frac{\mid \eta_{s,d,f} - \overline{\overline{x}}_{\eta,d,f} \mid}{N_f} \tag{1.41}$$

$$\overline{e}_{\%} = \frac{1}{N_f} \cdot \sum_{d} \left\| \frac{\eta_{s,d,f} - \overline{\overline{x}}_{\eta,d,f}}{\overline{\overline{x}}_{\eta,d,f}} \right\| \cdot 100\% \tag{1.42}$$

$$MMAPE = \frac{1}{N_f} \cdot \sum_{d} \left\| \frac{\eta_{s,d,f} - \overline{\overline{x}}_{\eta,d,f}}{\eta_{s,d,f} + \overline{\overline{x}}_{\eta,d,f}} \right\| \tag{1.43}$$

where $\eta_{s,d,f}$ is the estimated efficiency at a certain duty d, $\overline{x}_{\eta,d,f}$ is the mean measured efficiency and N_f represents the number of cases for a frequency f. At 40 kHz, the deviation between

the proposed model and the experimental test is significant only for a duty $d = 0.2$, which means at low currents, the remaining 5 values shows great compliance with the experimental tests. The same happens at 60 and 80 kHz: 3 simulation results fall into the uncertainty range in both cases and the displacement is only relevant at low currents. The estimated efficiencies that fall into the uncertainty range are highlighted in bold in Tables 1.2, 1.3 and 1.4. The proposed model appears to be superior to the ones chosen for the comparison by each KPI: the simplified model significantly overestimates the switching losses, instead, Christen's model [16] underestimates them; authors believe that it is mainly due to the equivalent C_{GD} capacitance approximation. Hu and Biela's model in [24] also shows good compliance with the experimental tests, even if the proposed one still wins over in terms of KPIs and displacement with respect to the measured efficiency, excluding the low current condition case. The efforts made by Hu and Biela in developing a low computation time and yet accurate model is indisputable, but as the authors themselves claim in the paper, the mathematic is very challenging and also the algorithm is quite complicated. Furthermore, in favor of the computational time, some initial and strong assumptions are made, such as: the step variation of the capacitances C_{GD}, C_{iss} and C_{DS}, the linear step-wise interpolation of the transfer characteristic and the temperature independency of the switching losses. In fact, not every manufacturer provides the variation of the switching losses with the junction temperature T_j. These simplifications lead to a deviation of the model from the measured values. The deviation is more and more prominent as the switching frequency increases, see Table 1.4, and the reason is trivial: the error on the energy losses increases linearly with the switching frequency. Especially for high power applications, this deviation can be relevant for the thermal, heat-sink, design. In Figure 1.9, simulation results are resumed and shown along with the uncertainty range.

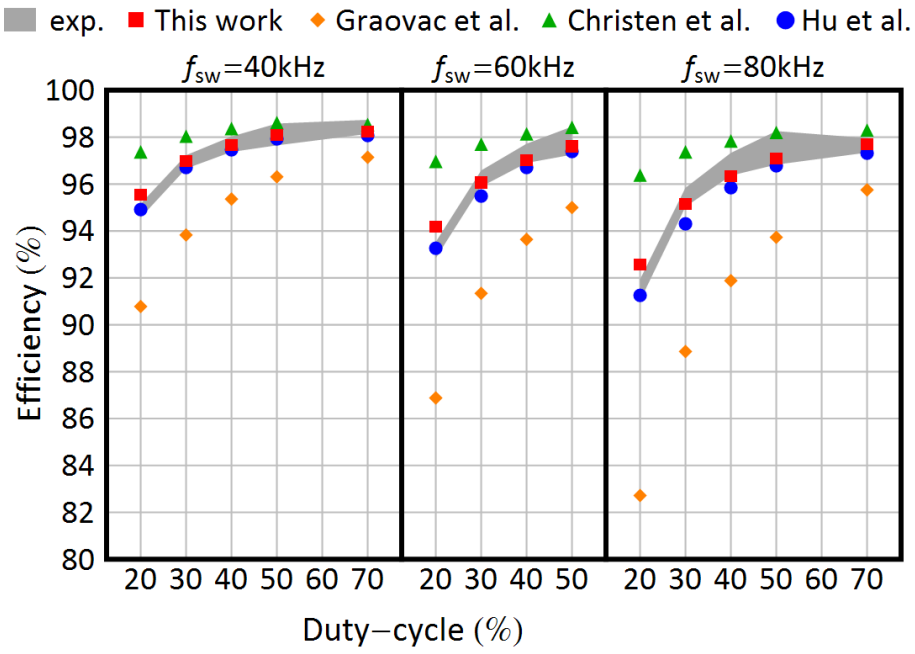


Figure 1.9: Comparison among experimental and simulation results. The filled area represents the experimental results including measurement uncertainty. Simulation results are reported for the model proposed in this work (filled rectangle) and those proposed in [9] (filled diamond), [16] (filled triangle) and [24] (filled circle).

Table 1.2: Efficiency comparisons at 40 kHz.

V_{DC} [V]	Duty [p.u]	Simplified model [9] η_s [%]	Model in [16] η_s[%]	Model in [24] η_s [%]	Proposed model η_s [%]	$[\overline{\overline{x}}_\eta - u_k]$	Measured $\overline{\overline{x}}_\eta$ [%]	$[\overline{\overline{x}}_\eta + u_k]$
400	0.2	90.78	97.37	**94.93**	95.54	94.57	94.87	95.16
400	0.3	93.83	98.04	**96.70**	**96.97**	96.66	96.95	97.23
400	0.4	95.36	98.37	**97.46**	**97.65**	97.37	97.7	98.03
400	0.5	96.31	98.62	**97.94**	**98.09**	97.65	98.12	98.58
400	0.7	97.14	**98.54**	98.07	**98.23**	98.14	98.44	98.74
450	0.7	96.81	98.33	**97.81**	**98.01**	97.80	98.04	98.28
500	0.3	93.35	97.73	96.60	**96.83**	96.80	97.02	97.24
n°		0	1	5	6			
$\overline{e}$		2.51	0.84	0.25	0.17			
$\overline{e}_{\%}$		2.59	0.87	0.26	0.18			
MMAPE		2.63	0.86	0.26	0.18			

Table 1.3: Efficiency comparisons at 60 kHz.

V_{DC} [V]	Duty [p.u]	Simplified model [9] η_s[%]	Model in [16] η_s[%]	Model in [24] η_s[%]	Proposed model η_s[%]	$[\overline{\overline{x}}_\eta - u_k]$	Measured $\overline{\overline{x}}_\eta$[%]	$[\overline{\overline{x}}_\eta + u_k]$
400	0.2	86.88	96.97	93.25	94.51	92.84	93.18	93.53
400	0.3	91.34	97.70	95.5	**96.38**	95.89	96.23	96.58
400	0.4	93.64	98.14	96.71	**97.30**	96.9	97.31	97.72
400	0.5	95.00	**98.42**	97.38	**97.78**	97.25	97.85	98.45
n°		0	1	2	3			
$\overline{e}$		4.43	1.67	0.47	0.43			
$\overline{e}_{\%}$		4.63	1.76	0.48	0.46			
MMAPE		4.75	1.73	0.48	0.45			

Table 1.4: Efficiency comparisons at 80 kHz.

V_{DC} [V]	**Duty** [p.u]	**Simplified model** [9] η_s [%]	**Model in [16]** η_s [%]	**Model in [24]** η_s [%]	**Proposed model** η_s [%]	$[\overline{\overline{x}}_\eta - u_k]$	**Measured** $\overline{\overline{x}}_\eta$ [%]	$[\overline{\overline{x}}_\eta + u_k]$
400	0.2	82.72	96.38	**91.26**	92.57	91.03	91.48	91.94
400	0.3	88.86	97.37	94.32	**95.14**	95.03	95.44	95.84
400	0.4	91.88	97.84	95.86	96.32	96.36	96.85	97.33
400	0.5	93.73	**98.2**	96.79	**97.09**	96.83	97.54	98.26
400	0.7	95.75	98.30	97.33	**97.7**	97.34	97.65	97.96
n°		0	1	1	3			
$\overline{e}$		5.2	1.83	0.68	0.48			
$\overline{e}_{\%}$		5.49	1.95	0.71	0.51			
MMAPE		5.68	1.92	0.71	0.51			

1.5 Final clarifications

It is very common in the literature to validate the switching losses model on a half-bridge with an inductive load; therefore, the same approach was used here. As the reader can see from Tables 1.2-1.4, the duty-cycle and the load current change at the same time. If the model was tested on an inverter for a standard electric drive application, then duty and load current could have been varied independently. The analytical model on a three-phase inverter is a future goal.

As a final clarification, it is worth mentioning that this NAM model is based on datasheet parameters, therefore the switching losses computation and the accuracy of the model strongly depends on the reliability of the datasheet parameters. Excluding incorrect extractions, the accuracy would be lost if the datasheet parameters were differing from the real ones. In the following picture a sensitivity analysis is made on three parameters:

- The internal gate resistance R_G.
- The current rise-time t_{ri} (similar considerations can be made for the current fall-time t_{fi}).
- The gate-drain capacitance C_{rss}.

A variation of $\pm 1\,\Omega$ is applied to the first parameter, instead the other two, which follow, are changed of $\pm 10\,\%$. Apart from t_{ri}, and consequently t_{fi}, which less affect the accuracy of the model, even a small variation of the other parameters generates a visible shift with respect to the reference (efficiency calculated in Table 1.3). The analysis is not complete, because not every parameter was scanned and the study was carried out at a single switching frequency, 60 kHz. Figures 1.10, 1.11 and 1.12 represent the sensitivity analysis of the parameters, in the same order described above.

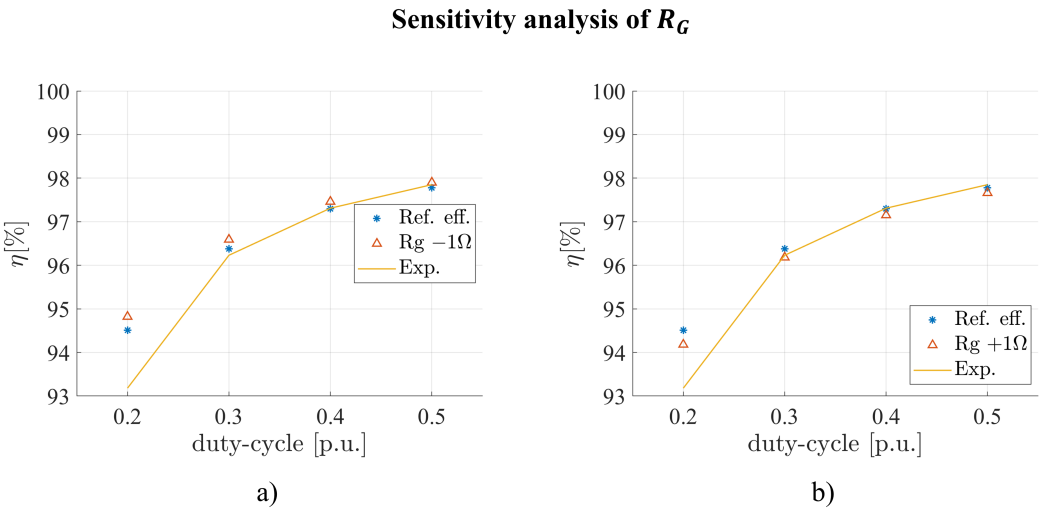


Figure 1.10: Effect of the sensitivity analysis of the gate resistance on the efficiency: a) R_G reduced of 1 Ω and b) R_G increased of 1 Ω. Continuous line represents the experimental results, stars represent the simulated values of Table 1.3 and triangles represent the estimated efficiencies when the parameter is changed.

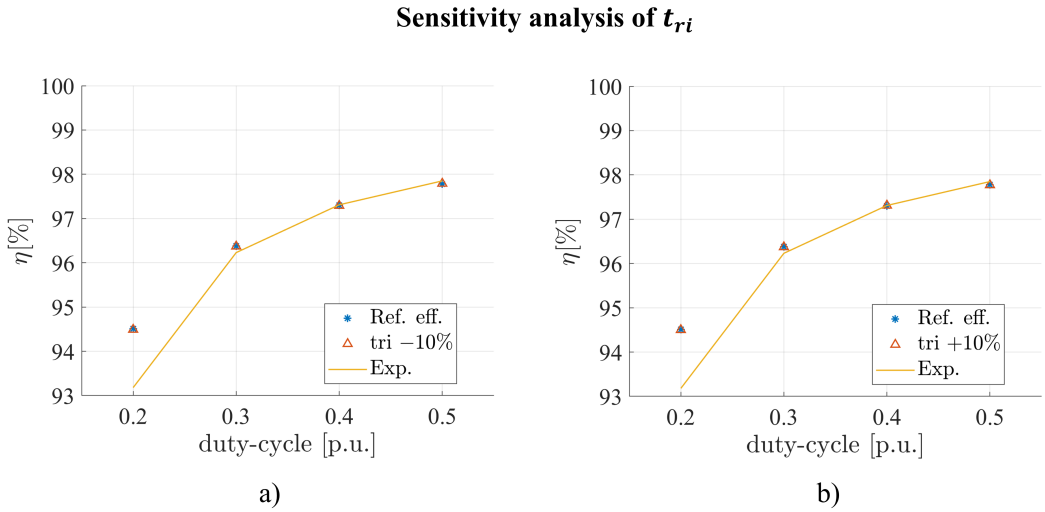


Figure 1.11: Effect of the sensitivity analysis of the current rise-time on the efficiency: a) t_{ri} reduced of 10 % and b) t_{ri} increased of 10 % . Continuous line represents the experimental results, stars represent the simulated values of Table 1.3 and triangles represent the estimated efficiencies when the parameter is changed.

1.6 Conclusions

SiC devices enable higher efficiency and power density due to faster switching and lower conduction losses, as well as operation at elevated temperatures. A comprehensive losses model supports the development of online virtual sensors for indirect efficiency and junction temperature monitoring. As power density increases, thermal stress on MOSFETs grows, which

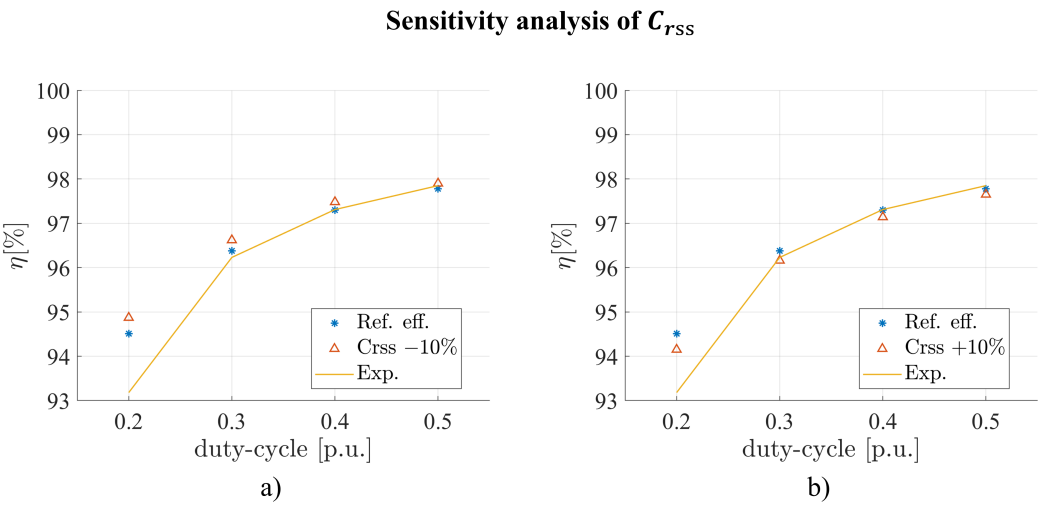


Figure 1.12: Effect of the sensitivity analysis of the gate-drain capacitance on the efficiency: a) C_{rss} reduced of 10 % and b) C_{rss} increased of 10 %. Continuous line represents the experimental results, stars represent the simulated values of Table 1.3 and triangles represent the estimated efficiencies when the parameter is changed.

without proper loss and device status monitoring, reduces system MTTF. An effective analytical model to estimate SiC MOSFET switching losses has been proposed, based exclusively on information derived from datasheets. The model is kept as simple as possible by neglecting some secondary effects on total switching losses, such as the charging and discharging of the output capacitance C_{oss}, which is a useful approximation and does not hinder its applicability in the power electronics industry. Additional assumptions regarding parasitic inductances and the short-channel effect are made to avoid preliminary and time-consuming measurements for parameter extraction. The reverse-recovery approximation applies specifically to the case studied in this work, although this contribution can be easily integrated if needed. Despite these simplifications, the model proved to be consistent with experimental tests and outperformed state-of-the-art models across all selected KPIs. A maximum MMAPE of 0.51 % was recorded at 80 kHz. The accuracy of the model is validated by the experimental results presented in subsection 1.3, which also account for measurement uncertainty. The model demonstrates high versatility, as it can be applied to any SiC MOSFET part number for all-SiC applications and can be easily adapted to lower-performance drives without SiC Schottky diodes. Since the algorithm can run in both C/C++ environments and MATLAB scripts, its implementation for a virtual sensor or online efficiency measurements is also straightforward.

1.7 Future developments

A further development is to implement the model for the calculation of efficiency and temperature in real-time under various load conditions in a typical electric drive application. These tests will also prove the effectiveness of the proposed model in estimating junction temperature and allow a proper lifetime evaluation, which will be carried out in a next work.

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2. Three-phase SiC Photovoltaic Inverter

2.1 Introduction

This chapter can be included, as the first one, as a contribution to the YESvGaN project. As explained in the introduction, both UNIMORE and Raw Power S.r.l. participated in the project. The author participated in the hardware design of a photovoltaic three-phase inverter: especially the design of the DC Bus board was entirely made by the author. The same goes for the simulations. Raw Power S.r.l. gave support in the design and Fraunhofer IIS designed the half-bridge leg, which was revised by other partners Raw Power S.r.l. and the author included. Some tests were performed on a resistive load, but a lot of the activities are still on-going. Depending on funding and time availability, future work will be carried out to make a lifetime assessment of the inverter and to make it inject into the grid. This chapter is therefore organized as followed: in subsection 2.2 main grid codes are listed, which are necessary to inject into the grid are defined. Then, an overview of the existing architectures is presented in subsection 2.3. In subsection 2.4 some simulations are reported. Finally, in subsection 2.5 and the designed board is described. Finally, in subsection 2.6 some conclusions and hints are given mainly for future work.

2.2 Grid Codes

Here a brief list of the grid codes, which are mandatory to connect a PV plant to the grid is presented. The legislation to which this chapter refers consists of both CEI 0-21 [1] and CEI EN 50160 [2].

1. The maximum global admitted THD % for each voltage phase must be under 8 %, even when a non-linear and/or unbalanced load is connected to the grid. There are also requirements for the relative voltage of a single harmonic, about which the author refers directly to the legislation [2].

2. The maximum global admitted THD % for each current phase must be below 5 %. The

same considerations of the voltage harmonics follow for the current harmonics.

3. The maximum DC current injected by a power system should be less than 0.5 % of the rms current injected into the grid for each phase. If this requirement is not satisfied, it is necessary to employ an insulation transformer after the inverter, which is nowadays unlikely because it introduces a decrease in the global efficiency of the power conversion system.

4. For a PV system, the average power factor must be quasi-unitary with the possibility of a little reactive power injection in the grid. The required power factor is greater 0.9 when the output is greater than 50 % [3].

5. Requirements exist also for the frequency; specifically, ranges are defined and need to be respected in the real application.

In the designed PV inverter, compliance with the grid code is granted, as shown in subsection 2.4.

2.3 Overview of known architectures

The pivotal component of grid-tied PV power systems is the PV inverter. Its primary role is to transform the DC electricity produced by PV panels into AC power synchronized with the grid. Depending on how the photovoltaic power plant is setup, photovoltaic inverters can be classified as follows:

- module integrated inverters, usually in the 50–400 W range for very small PV systems (one panel);
- string inverters, typically in the 0.4–2 kW range for small rooftop systems with panels connected in a single string;
- multi string inverters, generally in the 1.5–6 kW range for medium to large rooftop systems with panels arranged in one or two strings
- mini central inverters, typically over 6 kW with a three-phase topology and modular design for larger rooftops or smaller power plants around 100 kW and common unit sizes

of 6, 8, 10, and 15 kW;

- central inverters, normally in the 100–1000 kW range with a three-phase topology and modular design for large power plants spanning up to several megawatts and usual unit sizes of 100, 150, 250, 500, and 1000 kW.

The first grid-connected PV plants, employing thyristor based central inverters, emerged in the 1980s. SMA introduced the first mass-produced transistor-based PV inverter, the PV-WR, in 1990. From the mid-1990s onward, IGBT and MOSFET technologies have been widely adopted in all PV inverter categories except for module-integrated ones, which predominantly use MOSFETs. The high cost of solar energy has made efficiency the main focus of PV inverter technology, leading to a wide variety of PV inverter designs on the market. Compared to motor drive inverters, PV inverters are more intricate in both hardware and functionality. The need to elevate input voltage, implement a grid connection filter, grid disconnection relay, and DC switch contributes significantly to their hardware complexity. Standard functions of PV inverters include maximum power point tracking, anti-islanding, grid synchronization, and data logging.

In contrast to the electrical drive industry, which is two decades older and cost-driven with the full-bridge topology widely accepted globally, novel topologies for PV inverters have recently been introduced to boost efficiency and cut manufacturing costs. Given that PV panels typically last over 20 years, efforts are also being made to extend the lifespan of PV inverters. Nowadays, some manufacturers offer extended services for up to 20 years. The initial approach to improve efficiency involved removing the galvanic isolation traditionally provided by high-frequency transformers in the DC-DC boost converter or by a low-frequency transformer at the output, leading to a standard increase in efficiency of 1-2 %. PV panels generally feature a sandwich structure of glass, silicon semiconductor, and a back-plane framed by a grounded metallic frame, resulting in earth capacitance that creates a pathway for leakage current. This can jeopardize personal safety, monitored through systems that track leakage currents as fault indicators, especially in residential settings. This capacitance can fluctuate significantly based on construction or weather conditions, and typical values of 10 nF/kW for photovoltaic are observed when using the full-bridge with unipolar modulation, a known source of common mode voltage causing leakage current. Unfortunately, the transformer-less design necessitates more intricate solutions, often leading to innovative topologies to maintain control over leakage current and DC current injection to meet safety standards.

A significant design challenge propelling the creation of new topologies is the need to maintain

high efficiency even at partial loads, such as during periods of reduced irradiation. A metric known as 'European efficiency' has been established, which accounts for the varying irradiation levels observed across Europe. Presently, the market is flooded with numerous PV inverter manufacturers like SMA, Sunways, Conergy, Ingeteam, Danfoss Solar, Refu, etc., all of which offer a diverse range of transformerless PV inverters with very high European efficiency ($> 97\%$) and peak efficiency up to 98 %. The evolution of topologies for transformer-less PV inverters has largely been based on two "proven" converter families: H-bridge; and Neutral Point Clamped (NPC). The goal of this chapter is to outline some of the most significant current transformer-less PV inverter configurations derived from these core families. There is considerable diversity since some designs necessitate a boost DC-DC converter, either with or without isolation. Boost converters are well-documented and are out of the scope of this chapter. In subchapter 2.3.1 a brief list of the most common commercially available inverter topologies with their advantages and drawbacks is presented, and in subchapter 2.3.2 the same is done with three-phase topology, to which the designed inverter belongs.

2.3.1 Commercial Photovoltaic Single-phase inverters

The H-bridge or full-bridge (FB) converter family, initially created by W. Mcmurray in 1965, has served as a significant milestone in the evolution of power electronic converter technology. Here, some of the main topologies are defined.

In 2005, SMA secured a patent for an innovative inverter topology known as H5. Illustrated in Figure 2.1 [4], the design is essentially a full-bridge, supplemented with an additional fifth switch in the positive bus of the DC link. This switch plays two crucial roles: it prevents the interchange of reactive power between the grid inductance $L_1(L_2)$ and the DC-BUS capacitors C_{PV} during the zero voltage state, thereby increasing efficiency, and disconnects the photovoltaic module from the grid in the zero voltage state, effectively removing the high-frequency components of V_{PE}. S_2, S_4 and S_5 are switched at high-frequency, instead S_1 and S_3 operate at the grid frequency (50 Hz in Europe).

The main advantage introduced by this topology is the uni-directionality of the voltage across the filter ($0 \rightarrow +V_{PV}$ or $-V_{PV} \rightarrow 0$). The high efficiency of up to 98% is attributed to both the absence of reactive power exchange and the reduced switching frequency in one leg. Moreover, V_{PE} contains only the frequency component of the grid, eliminating the components of the high switching frequency and resulting in very low leakage current and electromagnetic interference

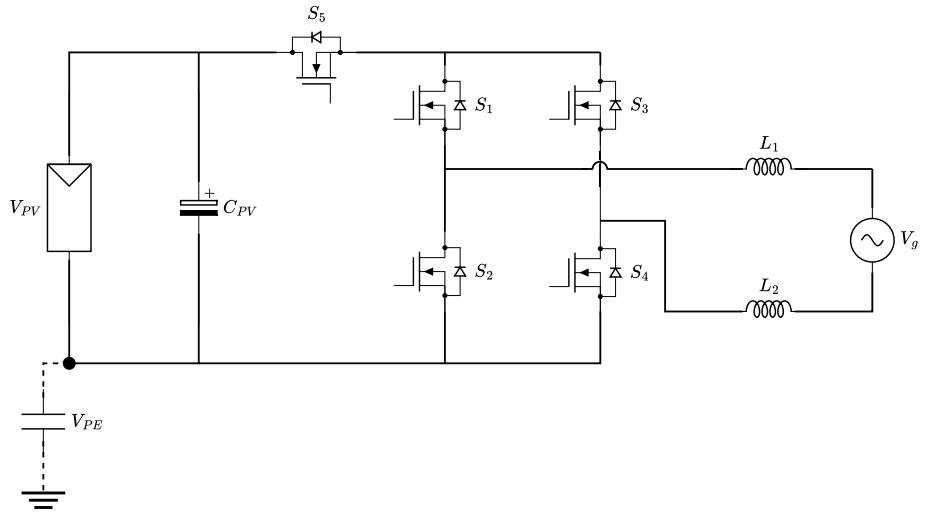

Figure 2.1: H5 Photovoltaic Inverter topology (SMA).

(EMI). The drawback is the need for an additional switch. The topology is therefore very suitable for transformer-less PV applications due to its high efficiency and low leakage current and EMI. It is currently marketed by SMA under the SunnyBoy 4000/5000 TL series, achieving a European efficiency above 97.7 % and a maximum efficiency of 98 % (Photon International, October 2007).

Another topology is the HERIC topology (highly efficient and reliable inverter concept). This innovation incorporated a bypass leg on the AC side using two back-to-back IGBTs, as illustrated in Figure 2.2. AC bypass plays the same crucial role as the fifth switch in the H5 topology.

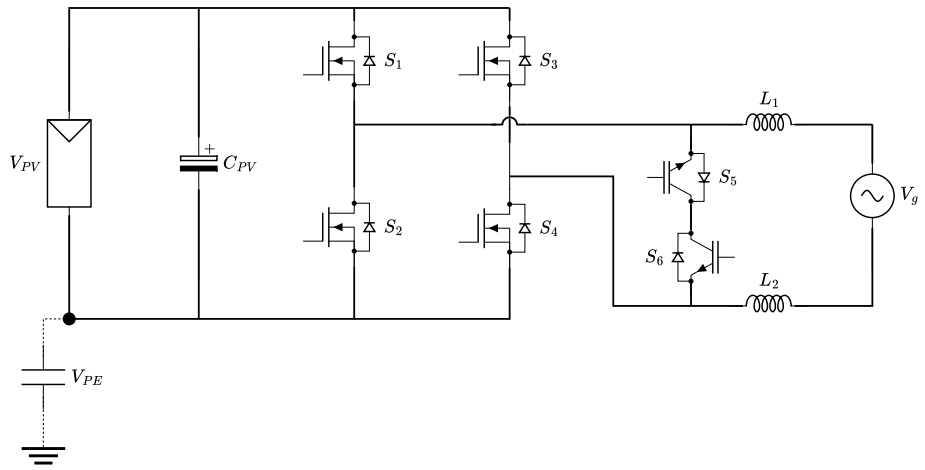

Figure 2.2: HERIC Photovoltaic Inverter topology.

Key features of this converter include:S_1, S_2, S_3 and S_4 switch at high-frequency while the IGBTs, S_4 and S_5, at grid frequency. Two zero output voltage states are possible: S_5 on and S_6 on

(with the bridge switched off). Advantages are similar to the H5 topology. The main drawback is the need of two additional switches. Sunways currently markets this technology in its AT series (2.7–5 kW), with a 95 % and a maximum efficiency of 95.6 % (Photon International, July 2008). The operating principles of HERIC and H5 are quite similar; both disconnect the PV generator from the grid during zero voltage states on the AC and DC sides, respectively. Each employs two high-frequency and one grid-frequency switches, with H5 having three simultaneous switch operations compared to the two of HERIC.

The year after, Refu Solar introduced a patented topology derived from the traditional H-bridge. This new design includes a half-bridge on the AC side bypass and a by-passable DC-DC converter, as illustrated in Figure 2.3 [5]. The AC bypass performs the same essential functions as in HERIC. Unlike HERIC, the AC bypass here employs unidirectional switches made up of standard IGBT modules with a series diode to eliminate the free-wheeling path. Actually, a more recent and efficient version, employed MOSFETs [6]. Another distinguishing feature of this topology is a boost converter that only activates when the input DC voltage is lower than the grid voltage. Here, S_1 and S_2 operate at high frequency when a boost is unnecessary ($V_{PV} >\mid V_g \mid$) instead S_3 and S_4 operate at high frequency, when a boost is required ($V_{PV} <\mid V_g \mid$). S_5 and S_6 switch at the grid frequency, based on voltage polarity. Advantages include a unipolar voltage across the filter ($0 \longrightarrow +V_{PV}$ or $-V_{PV} \rightarrow 0$), resulting in lower core losses.

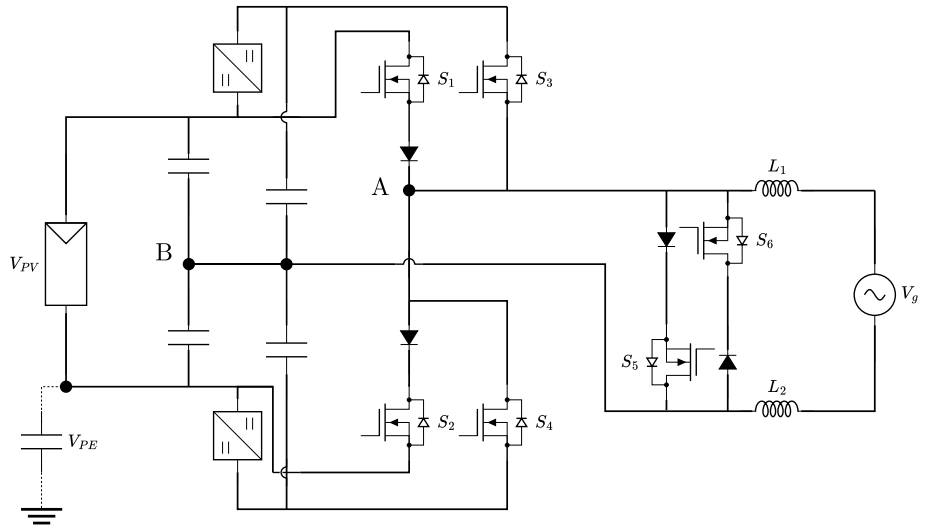

Figure 2.3: The REFU inverter topology.

An increase in efficiency of up to 98 % is achieved due to the lack of reactive power exchange between $L_1(L_2)$ and C_{PV} during zero voltage, activation of the boost function only when nec-

essary, and reduced switching frequency in one leg. The main drawbacks are the fact that it requires double DC voltage; two additional switches are needed, although they operate at low frequency [7].

Some three-level configurations exist, like the traditional NPC and its Conergy variant are also common. They offer the benefits of unipolar voltage on the filter, high efficiency from the clamping of PV panels during zero voltage states, and virtually no leakage due to the grounded midpoint of the DC link [8]. Given their increased complexity compared to FB-derived structures, these designs are commonly utilized in three-phase PV inverters with capacities over 10 kW (mini-central). Additionally, these topologies are highly attractive for high-power applications ranging from hundreds of kW (central inverters), where the advantages of multilevel inverters are even more pronounced.

As said, the Conergy inverter is an alternative to the conventional NPC configuration is a half-bridge setup where the output is tied to the neutral through a bidirectional switch. This switch consists of two series back-to-back IGBTs, as patented by Conergy [9] (see Figure 2.4). A different approach is outlined in reference [10], where the unidirectional clamping switches are arranged in parallel rather than in series, and a full-bridge design is used instead of the half-bridge. The fundamental concept of the Conergy NPC inverter is to achieve zero voltage by "clamping" the output to the grounded midpoint of the DC bus using S_3 or S_4, based on the current direction. S_1 and S_2 and both S_3 and S_4 function at elevated switching frequencies, and there exist two possible zero-voltage conditions: S_3 on, or S_4 on.

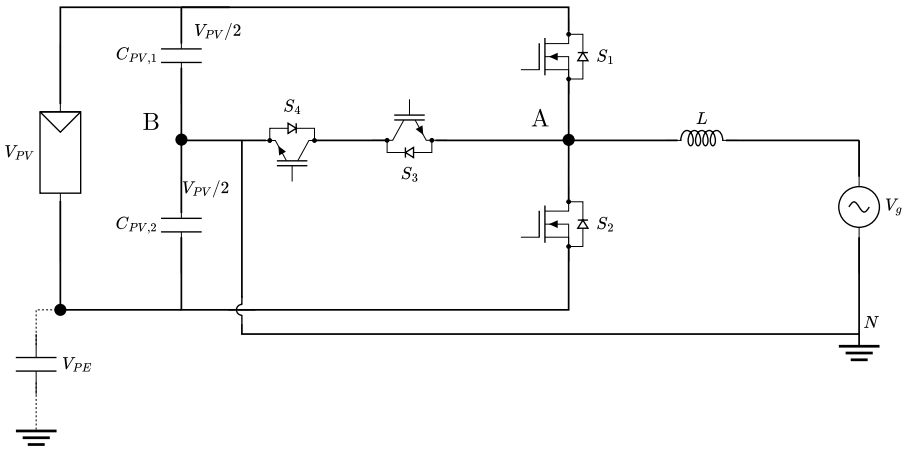

Figure 2.4: SiC MOSFET electric model with parasitic.

The primary benefits are the unipolar voltage across the filter ($0 \rightarrow +V_{PV}$ or $-V_{PV} \rightarrow 0$), which results in reduced core losses and increased efficiency up to 98 %. Moreover, in the

three-level configuration, the voltage drop is reduced with just one switch operating during the active states of the Conergy NPC inverter. V_{PE} remains stable at $-V_{PV}/2$ without switching frequency components, which contributes to a very low leakage current and EMI. Switching losses are also balanced, unlike in the traditional NPC. There are certain disadvantages inherent to this topology. For instance, the voltage rating for S_1 and S_2 must be double that of the outer switches in the NPC. This topology also needs a double voltage input when compared to the FB. Furthermore, any inductance added through the neutral link, like with EMI filters, induces high-frequency common-mode voltage which leads to leakage current.

2.3.2 Three-Phase PV Inverters

Most three-phase PV inverters tend to be three-phase four-wire systems instead of true three-phase three-wire inverters. These inverters act like three distinct single-phase inverters. This method provides the advantage of employing existing single-phase inverters.

Companies such as Conergy, Refusol, and Danfoss Solar are endorsing three-phase inverters in the 10-15 kW range, designed as three-phase configurations. A recent comparative analysis of transformer-less three-phase topologies [11] demonstrated that the three-phase NPC outperforms the full-bridge with a split DC link, particularly in reducing leakage, increasing efficiency, and improving overall performance. The main hurdle with a genuine three-phase three-wire topology is the need for a high DC voltage, around 600 V for a 400 V three-phase grid, restricted to a maximum of 1000 V for safety (maximum installation voltage). This limited voltage range may not support the fluctuations required by MPPT due to temperature changes and allowable grid voltage deviations. In contrast, single-phase inverters typically operate on a 400 V DC voltage, providing a wider variation range and thus greater flexibility.

However, in [12] a light weight 100 kW three phase string inverter is designed for utility applications. The inverter is built with 1200 V SiC MOSFET modules. The basic topology is a T-type circuit that is well-accepted in the PV industry. A new design is proposed to interleave two T-type modules to form a five level line-to-neutral output. Through interleaving, the AC side voltage harmonics and DC side current harmonics can be reduced, which leads to reduced filter size at both side. In this proposed design, AC side line filters are completely removed, and thereby the size and weight of magnetic components are reduced. The 100 kW lab prototype of the PV inverter, which includes the power circuit, magnetics, sensors, relays, cooling system, wireless communication, and auxiliary power supply, weighs less than 20 kg. This solution

is very effective and attractive, and it provides an example of an actual three-phase inverter. The author of this thesis developed a standard two-level three-phase inverter with the idea of simplifying the architecture the architecture, due to the high efficiency of WBG devices. Therefore in the next subsection simulations analyses are made on the topology along with a brief summary of the design. In subsection 2.5 the board design is presented.

2.4 Simulation of the PV inverter

Some hybrid architectures (SiC + Si) were theorized in literature, [13] for example. Although attractive, these solutions have not been perpetuated, since the YESvGaN project aim is the comparison between power converters which employ vertical GaN technology and the ones that employ SiC transistors. Therefore, a digital-twin of a two-level, three phase SiC photovoltaic inverter was built and developed in the Plexim environment.

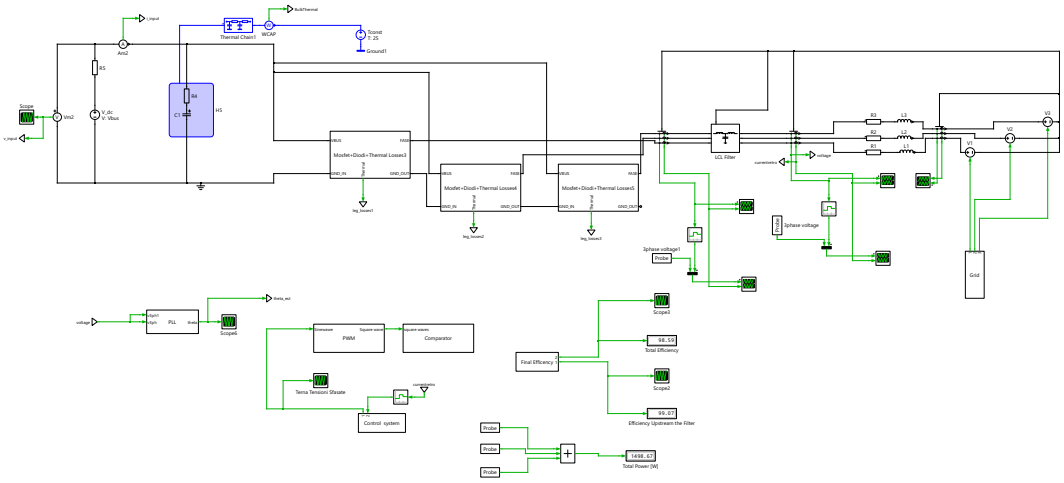

Figure 2.5: Digital-twin of the PV three-phase inverter with SiC technology.

In Figure 2.5, the main schematic of the digital-twin is shown: each subsystem, as called by PLECS, contains a full-bridge: particularly, two parallel SiC MOSFET C3M0075120J [14] are used, since they represent the three modules used to employed in the tests. The thermal model is developed following the guidelines of Chapter 1. An LCL filter is placed and his indeed necessary to meet the grid-codes. The grid is modeled as three voltage-controlled sources: the subsystem Grid just generates three sinusoidal waves shifted by $2/3\,\pi$ from one another and with a peak value $V_{g,peak} = 230\sqrt{2}$ V, which is the standard peak voltage of the low voltage grid in Europe. The three sources are then connected in series to a three-phase resistance and inductance placed in series to the generators: these parameters represent the grid in a

concentrated parameter model. The typical values chosen are as follows:

- $L_g = 0.2$ mH
- $R_g = 1\ \Omega$

Both voltages and currents are measured on the grid side, after the filter because it is not possible to measure them after the voltage sources: these points are not accessible in real grids.

2.4.0.1 Filter design

A great part of the traditional PV inverters which are commercially available, employ an LCL filter instead of an LC filter. The LCL filter must be placed between the converter and the points of interconnection with the grid. The two main roles of a grid filter are to guarantee of a proper operation for a converter when connected to a voltage-source system such as the utility grid, and the smoothness of voltage and current undesired harmonics that arise because of the fast switching of the semiconductors. Harmonics must be reduced because there are very stringent grid codes and the value of the THD % for both voltages and currents injected into the grid by the inverter is limited. For a PV inverter, stressed by high frequencies, it is mandatory to have filters of second or third order, such as LC or LCL. Especially the last one is generally preferred, due to the 60 dB/dec attenuation after the resonance frequency. The design rules of an LCL filter is treated: reference [3] has been followed. The THD % of both currents and voltages has been checked after the sizing, to ensure that it is sufficiently lower than the values specified by the grid codes,considering that they should be maintained when non-linear loads are present. Once the inductance L_{f1} on the converter side and the resonant frequency ω_r have been chosen, there is a degree of freedom in the choice of L_{f2} and C_f.

1. Firstly, the maximum acceptable ripple $\Delta I_{L,max}$ for the grid currents, as measured above the LCL filter should be defined. In (2.1), the subscript r stands for rated, P_r is the rated power, $V_{g,rms}$ is the rms grid voltage, and $I_{g,pp,r}$ is the peak to peak grid current. The coefficient 0.15 is a typical coefficient used to fix the maximum current ripple.

$$\begin{cases} I_{g,rms,r} = \frac{P_r}{3V_{g,rms}} \\ I_{g,peak,r} = \sqrt{2} I_{g,rms,r} \\ I_{g,pp,r} = 2 I_{g,peak,r} \\ \Delta I_{Lf1,max} = 0.15 \cdot I_{g,pp,r} \end{cases} \tag{2.1}$$

2. The L_{f1} is chosen from the maximum current ripple and the relation between them can be derived following the procedure presented in [15]. The relation (2.2) is suggested in [3] where V_{dc} is the supply voltage, f_{sw} is the switching frequency and n is an integer that depends on the number of levels of the PWM. However, the relation employed is shown in (2.3).

$$L_{f1} = \frac{1}{n} \cdot \frac{V_{dc}}{\Delta I_{Lf1,max} f_{sw}} \tag{2.2}$$

$$L_{f1} = \frac{\Delta V_{Lf1,max}}{\Delta I_{Lf1,max}} \cdot \Delta t = \frac{V_{la} - V_{ga}}{\Delta I_{Lf1,max} f_{sw,min}} \cdot \delta_{max} = \frac{V_{dc}}{7 \Delta I_{Lf1,max} f_{sw,min}} \tag{2.3}$$

$f_{sw,min}$ is the minimum switching frequency, δ_{max} is the maximum duty-cycle and $V_{la} - V_{ga}$ is the difference between the maximum voltage before the first inductance at the grid side. The approximation of neglecting the voltage drop across the second inductance L_{f1} has been made and leads to a little over sizing of the first inductance, so it is acceptable. In the designed PV inverter, the connection is made with the LV three-phase power grid and $V_{dc} = 800$ V and a symmetrical PWM is employed. Therefore, considering that the maximum phase voltage is $2V_{dc}/3$ and the peak of the grid voltage is fixed to $230\sqrt{2}$ V, then the maximum duty-cycle will be $\delta_{max} = 0.9$, taking a margin for the voltage drop across the filter.

3. The cut-off frequency for an LC filter is usually chosen as one tenth of the switching frequency. For an LCL filter, a higher value of the resonant frequency can be chosen, since after $\omega_r = 2\pi f_r$ the attenuation is 60 dB/dec instead of 40 dB/dec.

$$\omega_r = \sqrt{\frac{L_{f1} + L_{f2}}{L_{f1} C_f L_{f2}}} \tag{2.4}$$

4. After choosing ω_r, the degree of freedom remains, i.e. L_{f2} or C_f must be chosen. The capacitor C_f is chosen considering the maximum power variation. Empirical value is in the range of 1-5 % of the base capacitance C_b, (3 % is chosen for the design).

$$C_f = 0.03 \cdot C_b = \frac{0.03}{\omega_g Z_b} = \frac{0.03 P_r}{\omega_g V_{LL}^2} \tag{2.5}$$

   In (2.5), V_{LL} is the line-to-line voltage and ω_g is the grid pulsation, Z_b is the basis impedance.

5. Then L_{f2} is derived, inverting (2.4). Since the value of the grid inductance L_g is known, it has been noticed that subtracting it from L_{f2} would lead to more than acceptable THD. Then, L_g has been subtracted from the value of (2.4).

6. A dumping resistor should be chosen because at resonance frequency the LCL filter offers almost zero impedance. To avoid the current control loop instability, a damping solution must be adopted and it is chosen from (2.6).

$$R_D = \frac{1}{3\omega_r C_f} \tag{2.6}$$

Of course, the LCL filter parameters have been adjusted with respect to the theoretical ones, to guaranty a proper behavior of the PV inverter. In the simulations, each filter is individually placed on a heatsink.

Referring to the procedure mentioned above, the resulting parameters are listed below.

- $L_{f1} = 0.929$ mH.
- $L_{f2} = 0.345$ mH.
- $C_f = 6.02$ µF.

- $f_r = 3500$ Hz.
- $R_D = 2.518\ \Omega$.

Resulting $THD\%$ are the following.

- $THD_v = 0.0507$ %, for each voltage phase.
- $THD_v = 0.0507$ %, for each voltage phase.
- $THD_i = 0.669$ %, for each current phase.

And finally about the injected DC current for each phase:

- $I_{dc} = 0.00583$ % of I_{rms} for phase one.
- $I_{dc} = 0.00196$ % of I_{rms} for phase two.
- $I_{dc} = 0.00387$ % of I_{rms} for phase three.

All these were measured in at 10 kW of delivered output power into the grid and 20 kHz of switching frequency.

2.4.0.2 PLL structure

As well explained in [3], the PLL consists of three main blocks.

- *Phase detector* (PD): it receives both the measured voltage, usually normalized, and an angle generated internally by an oscillator inside of the PLL itself, which defines the PLL as a feedback system. The PD outputs an error proportional to the difference between the measured voltage and the voltage signal generated inside. If the PLL can connect perfectly, this error is zero in the regime condition.
- *Loop Filter* (FL): the loop filter is a low pass filter that cuts-off the high frequency components of the input signal. This filter is necessary because the input voltages, especially if the power is injected into the grid by power converters, contains several harmonics, but the PLL needs to synchronize to the grid frequency, so only the fundamental component of the voltage should be kept. The loop filter is usually a Proportional Integral PI controller.
- *Voltage-controlled oscillator* (VCO): the last block receives as input a voltage signal from the LP and firstly multiplies it for a gain k_{vco}, then the resulting pulsation is added to the fundamental grid pulsation $\omega_g = 2\pi\,50$, which allows pushing the dynamics of the PI regulator because it will work in a narrower range. The resulting pulsation $\omega^{'}$ is integrated and finally the estimated phase angle $\theta^{'}$ is obtained. The angle $\theta^{'}$ is used for

Park's transformation.

The feed forward pulsation ω_c in this case of a grid connected converter corresponds to the grid pulsation under normal conditions of operation $\omega_c = \omega_g$. In a PV inverter, a three-phase PLL must be implemented in the synchronous reference frame. The type of PLL employed here is the SRF-PLL, Synchronous Reference Frame PLL, see Fig. 2.6. The PD in this case evaluates the q component and normalize it, v_q becomes the error itself because the aim is injecting currents in phase with the voltages. the relation between teh dq components and line components is described by both Park and Clarke transformation.

$$v_{dq} = \begin{bmatrix} v_d \\ v_q \end{bmatrix} = \begin{bmatrix} \cos(\theta') & \sin(\theta') \\ -\sin(\theta') & \cos(\theta') \end{bmatrix} \cdot \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \cdot \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \tag{2.7}$$

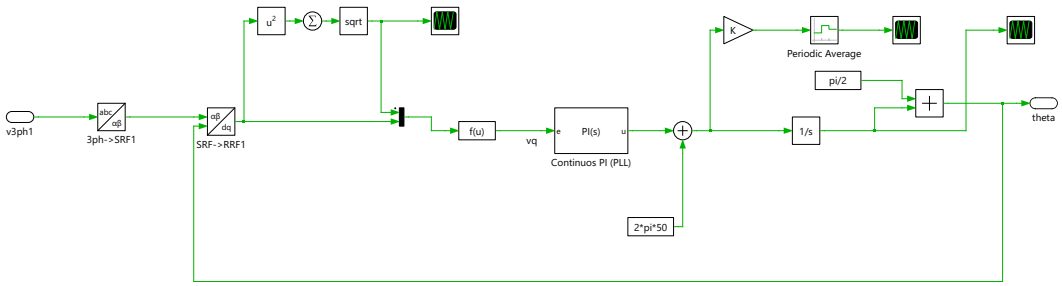

Figure 2.6: SRF-PLL structure.

The gains of the PI inside the PLL, were selected in order to obtain the following bandwidth and phase margin:

- $\omega_{BW,PLL} = 2\pi \cdot 30$ rad/s
- $\phi_{PLL} \approx 65\,^\circ$

The bandwidth is typical for grid connected converters between 20-50 Hz, and the phase margin was selected for proper stability. Both proportion and integral gains were slightly adjusted from the analytical values, which are given in (2.8).

$$\begin{cases} k_{P,PLL} = \frac{2\zeta\omega_n}{V_{d,peak}} \\ k_{I,PLL} = \frac{\omega_n^2}{V_{d,peak}} \end{cases} \tag{2.8}$$

where $V_{d,peak} = 230\sqrt{2}$ and $\zeta = 0.707$ for the proper phase margin and ω_n is selected based on $\omega_{BW,PLL}$.

2.4.0.3 Control system

The control system mainly consists of a regulation on two synchronous reference frame axes d and q. Two PI regulators are implemented. The references are a step of 20 A with a step-time of 5 ms for the d-axis of and a constant of $I_q^* = 0$ A during the whole simulation. The step is not set at beginning of the simulation, to give a proper time to the PLL to tie. The references are compared to I_d and I_q derived from Clarke and Park transformations of the measured currents on the grid side. Both PIs, as well as for the PIs in the PLL subsystem, are provided by PLECS library. In this case, for both regulators, a Conditional Integration anti-windup method is employed: the upper and lower limits are ±50 V on the d-axis and ±20 V for the q-axis. On the d-axis, a feedforward compensation is implemented, where the constant is equal to $V_{g,peak}$. In this way, the PI dynamic can be improved. For both regulators, gains were tuned by adjusting the analytical values. The bandwidth should be chosen in the range $10 \cdot \omega_{BW,PLL} \leq \omega_{BW,I} \leq 10 \cdot 2\pi\, f_{sw}$. The phase margin ϕ_I is normally selected around 60 °.

- $\omega_{BW,I} = 2\pi\, 1000$ rad/s
- $\phi_I = 60\,^\circ$

$$\begin{cases} k_{P,I} = (L_{f1} + L_{f2}) \cdot \omega_{BW,I} \\ k_{I,I} = R_g \cdot \omega_{BW,I} \end{cases} \tag{2.9}$$

PI dynamic allows following the step reference in less than 3 ms with a small overshoot, in Fig. 2.7 the schematic is shown.

The modulation used is a symmetrical PWM. The simulations reported in this chapter refer to the condition of unity power factor ($I_q^* = 0$). However, other operating points were tested, even if not reported considering the possibility of injecting a non null reactive power Q into the grid to compensate for voltage dips, for example.

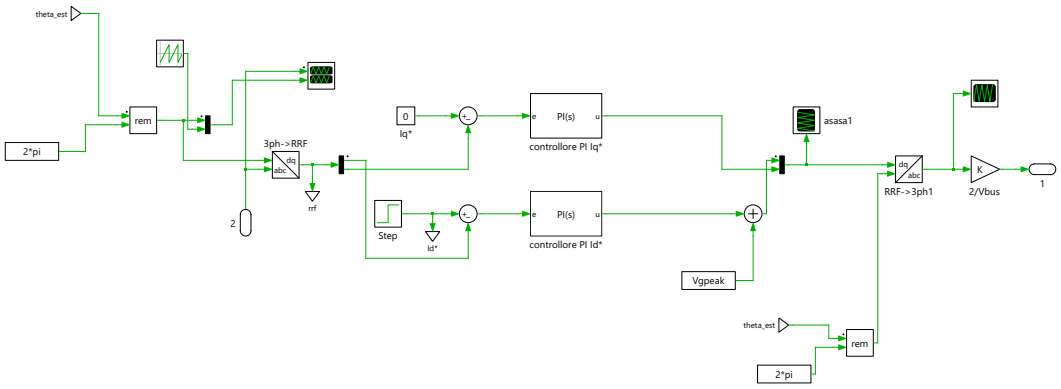

Figure 2.7: Control schematic of the PV inverter.

2.4.0.4 Efficiency computation

The calculation of efficiency for different current values, at frequencies: 20 kHz and 40 kHz, resumed in Tables 2.1 and 2.2, highlights the possibility of using simple architectures for PV inverters with WBG components. Efficiency is computed as in (2.10).

$$\eta = 1 - \frac{P_{loss}}{P_{in}} \tag{2.10}$$

Here, P_{loss} is evaluated as the sum of all the components of the losses: each leg individually, the bulk thermal losses, and the output filter losses. Some simulation captures of currents before and after the filter at both 10 and 40 kHz and for 20 and 30 A_{pk} setpoint are shown. In the

Table 2.1: PV inverter simulation results at 20 kHz.

I_d [A_{pk}]	P_{out} [W]	P_{loss} [W]	**Eff. before filter** η [%]	**Eff. after filter** η [%]
5	2444	56	98.60	97.74
10	4996	94	98.70	98.14
20	10346	194	98.67	98.16
30	16061.4	324.2	98.59	98.02

next subsection, the PV inverter is designed and explained, and a few remarks are made about future work.

Table 2.2: PV inverter simulation results at 40 kHz.

I_d [A_{pk}]	P_{out} [W]	P_{loss} [W]	**Eff. before filter** η [%]	**Eff. after filter** η [%]
5	2424	76	97.59	96.97
10	4953	137	97.72	97.30
20	10254	286	97.73	97.28
30	15866.4	471	97.76	97.12

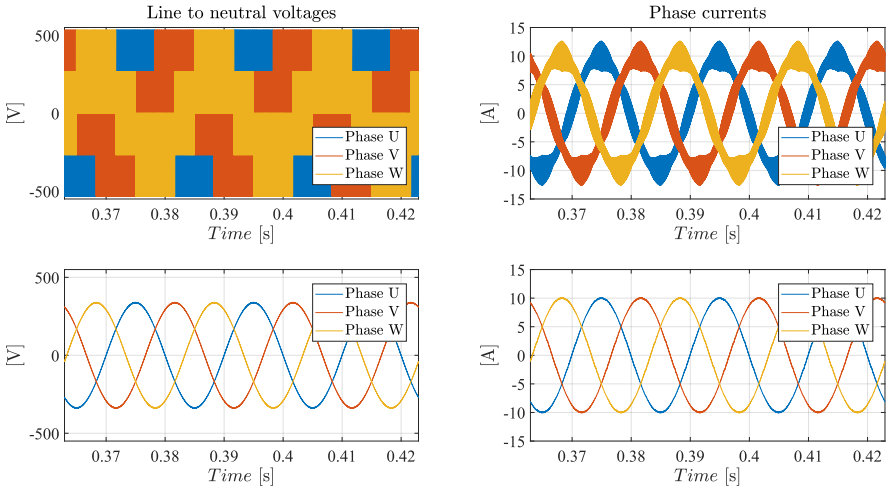

Figure 2.8: Results of simulations for $f_{sw} = 20$ kHz and $I_d = 10$ A. On top the captures before the filter and on the bottom the ones after.

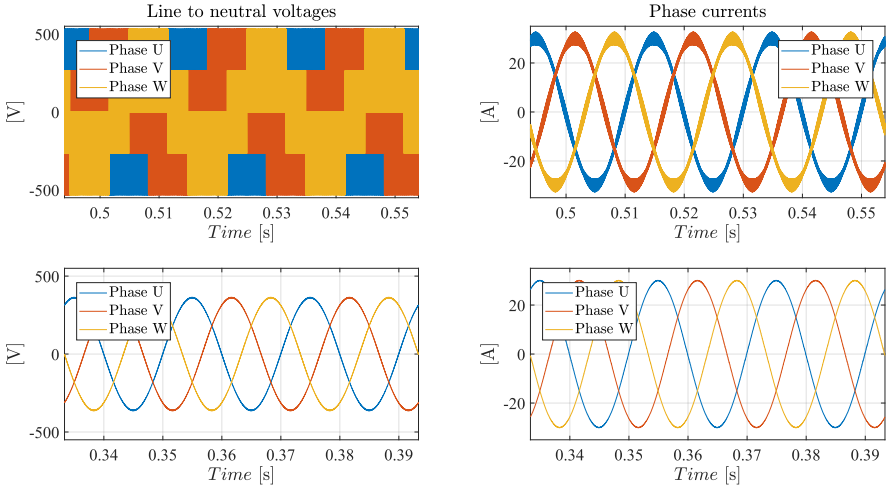

Figure 2.9: Results of simulations for $f_{sw} = 20$ kHz and $I_d = 30$ A. On top the captures before the filter and on the bottom the ones after.

2.5 Photovoltaic Inverter design

In this subchapter, schematics and PCB screenshot of the DC-Bus board, taken from Altium Designer, are presented. DC Bus includes: Bus capacitors and input current sensing, phase

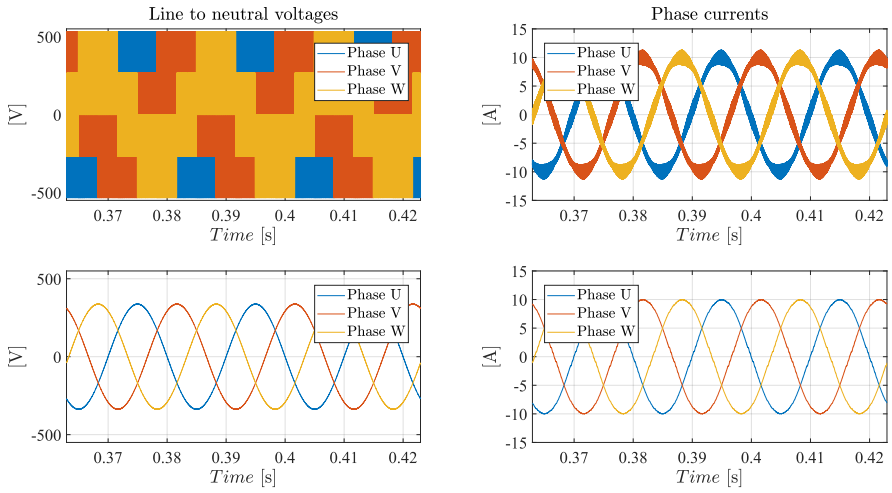

Figure 2.10: Results of simulations for $f_{sw} = 40$ kHz and $I_d = 10$ A. On top the captures before the filter and on the bottom the ones after.

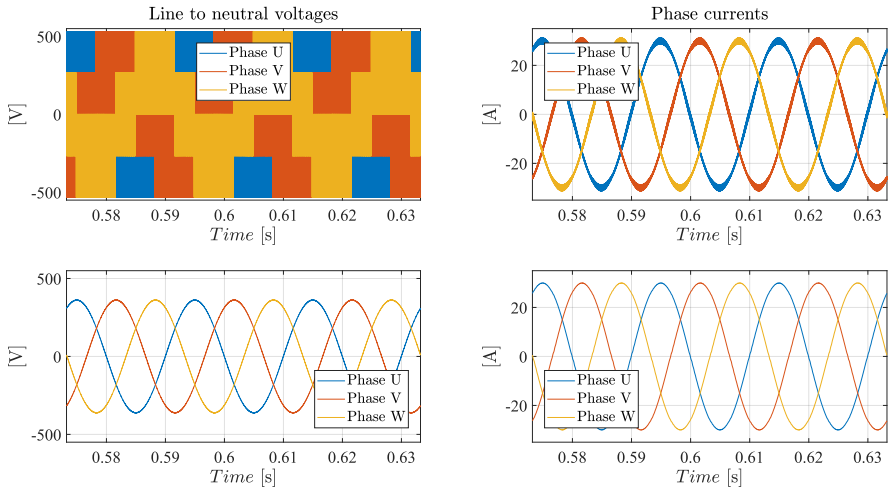

Figure 2.11: Results of simulations for $f_{sw} = 40$ kHz and $I_d = 30$ A. On top the captures before the filter and on the bottom the ones after.

current and phase voltage sensing as well as the conditional circuitry for phase voltage. Power and logic supply are completely separated. Unlike the current detection in Figure 2.13, which provides a single-ended output, the TV transformers used for voltage detection are differential, Figure 2.14, which explains the circuit of Figure 2.15. Logic is managed by an integrated SOM Board, with a STM32G473 microcontroller on. The SOM board is shown in Figure 2.16. The DC-Bus board has been designed to host three half-bridges of Fraunhofer GmbH: board schematics are confidential and cannot be shown. To explain briefly, the module integrates a full half-bridge power module, constituted by a pair of parallel of SiC MOSFETs C3M0075120J by Wolfspeed. Gate drive circuitry is integrated in the module: the employed gate drive is

IVCR1401, one for the high-side and one for the low-side. Isolated supplies are made through two flyback converters,LT8301IS5 (transformer part number is PM9595NLT). A picture of the module alone is shown in Figure 2.17.

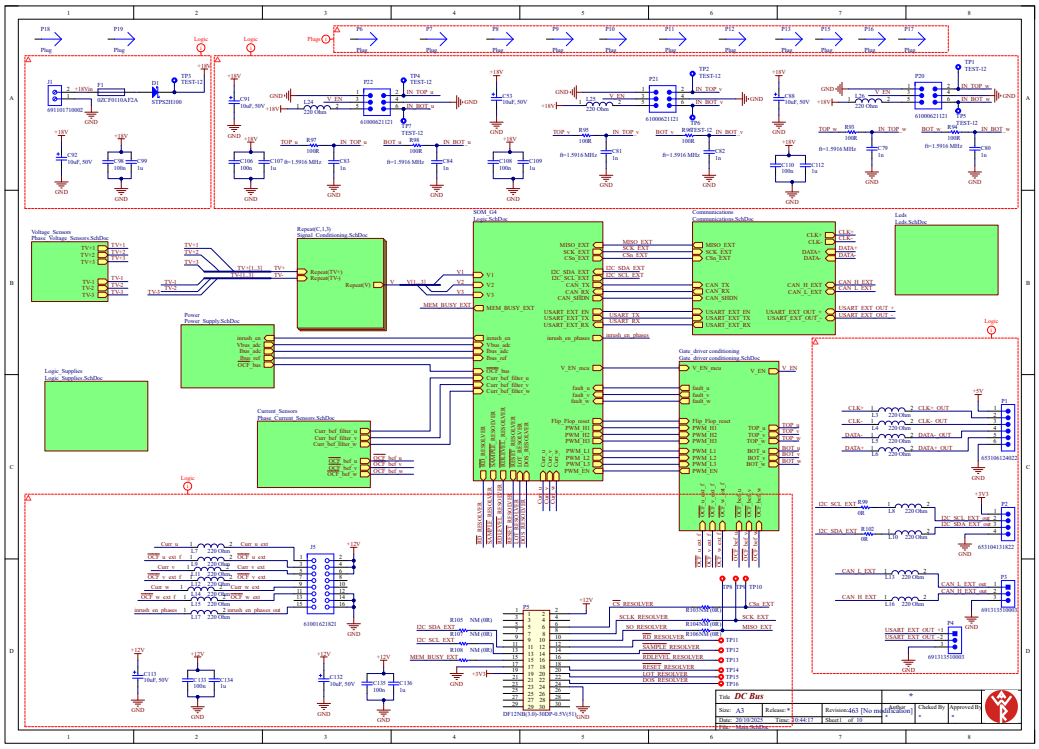

Figure 2.12: Main schematic DC Bus board.

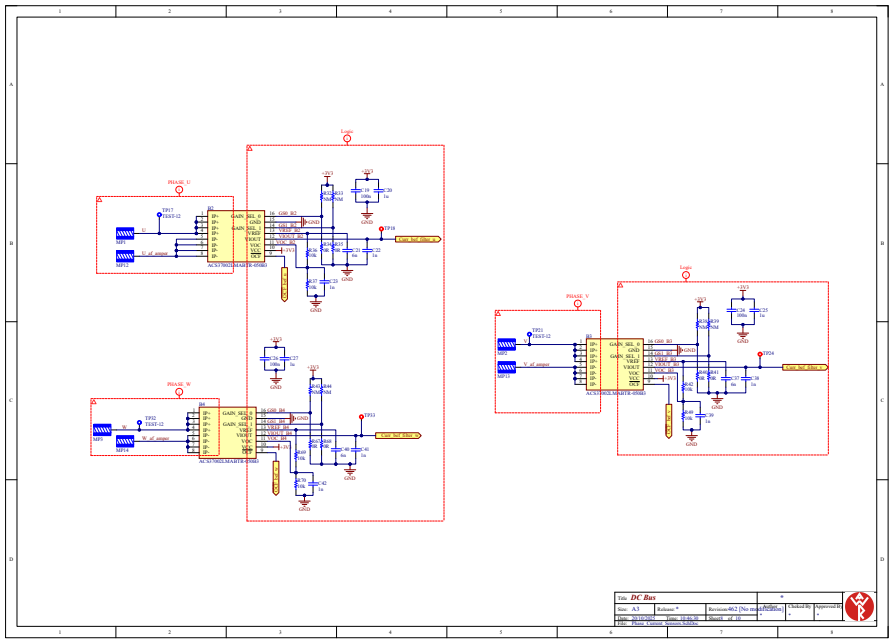

Figure 2.13: Phase current sensing: ACS37002LMABTR-050B3 sensor.

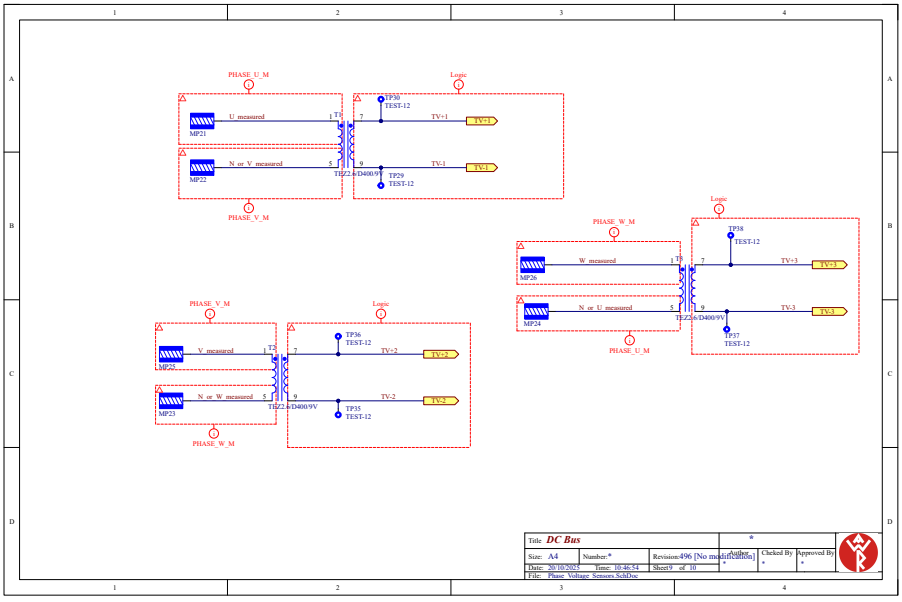

Figure 2.14: Phase voltage sensing: TEZ2.6/D400/9V TV transformer.

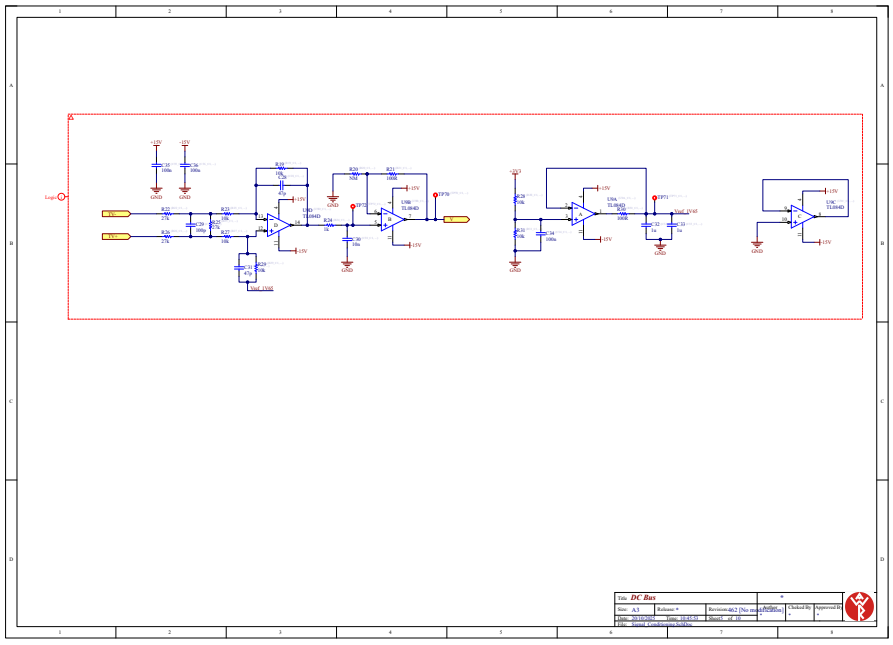

Figure 2.15: Voltage conditioning circuit.

In Figure 2.18 and 2.19 a screenshot of the PCB is reported. The three modules are meant to be be placed where the purple rectangles are.

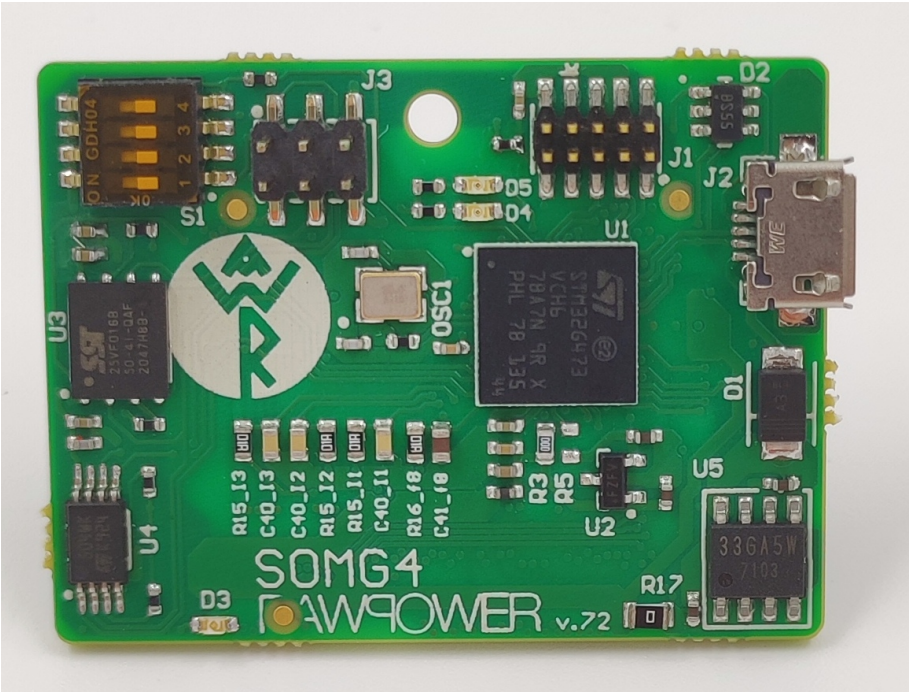

Figure 2.16: SOM logic board that is placed on the DC Bus.

Figure 2.17: Fraunhofer half-bridge module.

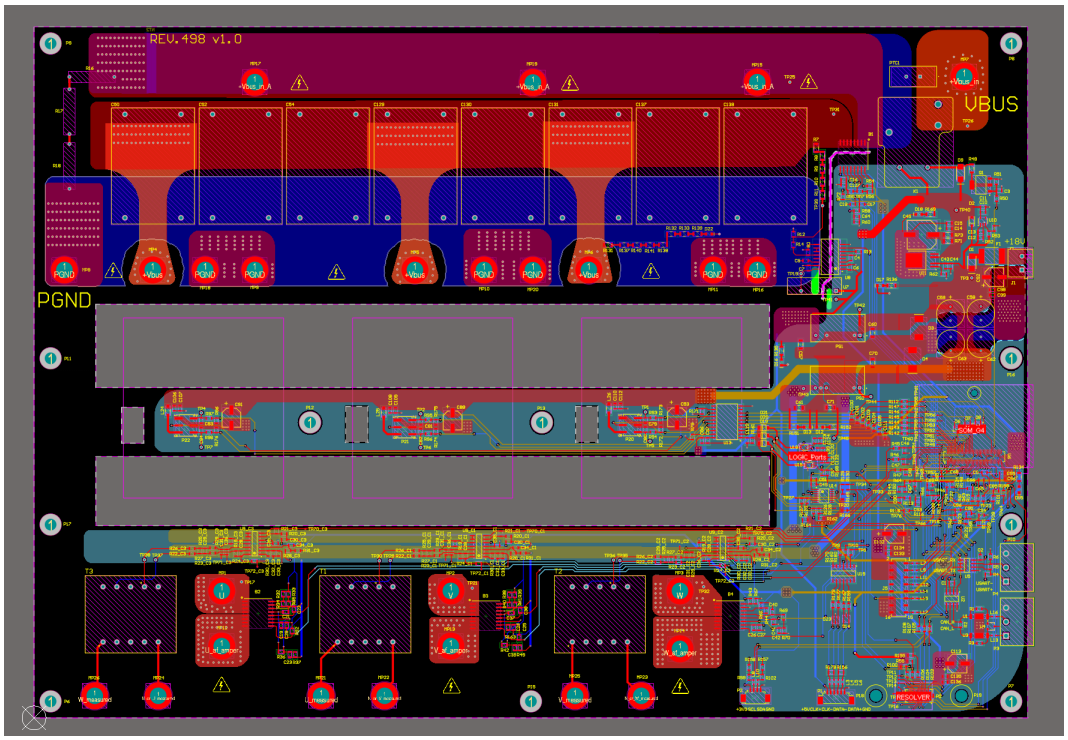

Figure 2.18: PCB screenshot of the whole DC Bus.

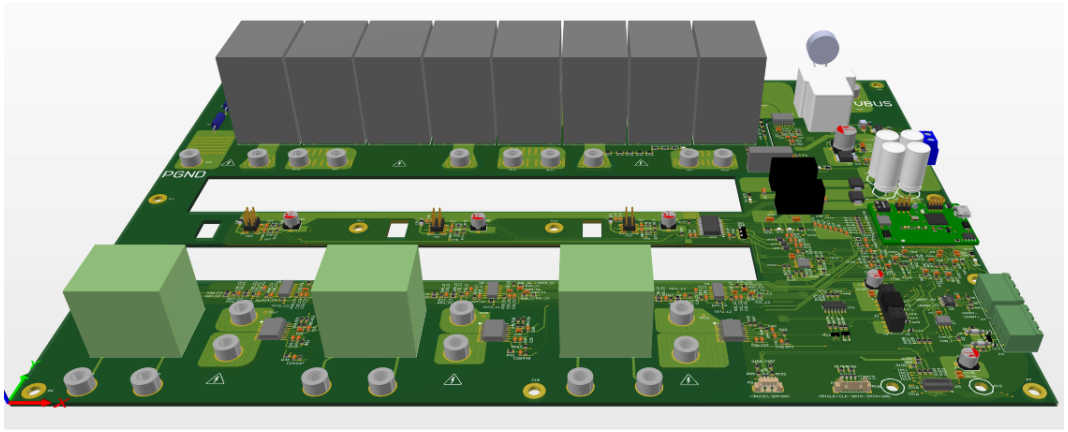

Figure 2.19: PCB screenshot of the whole DC Bus.

2.6 Conclusions and future work

This work is currently under development, and especially two forward steps are willing to be taken. First, test will be made on the power converter, first on a resistive load with a DC voltage supply as shown in Figure 2.20. Then a test on the grid injection with an LCL filter will be made. Several load test conditions will be useful to further validate the SiC switching losses of chapter 1. Up to now, just some successful debug tests have been made. Another step forward will be the lifetime assessment of the converter based on a typical load profile over the whole year in Emilia-Romagna region. Lifetime model will be always be based on the switching power losses model presented in chapter 1. From the simulations the efficiency results are very promising, it is hoped and awaited will show results accordingly.

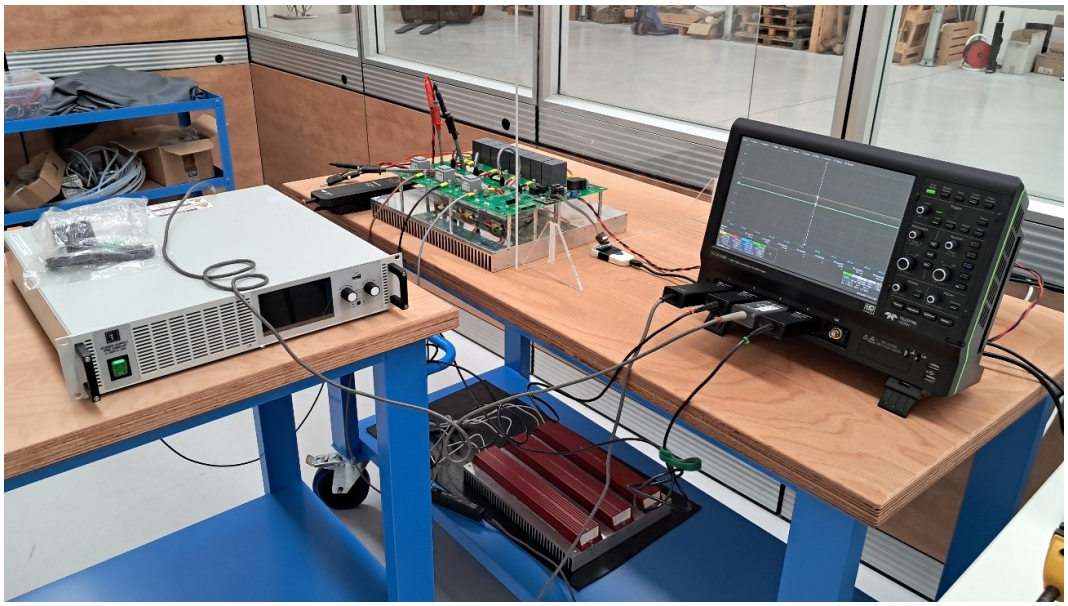

Figure 2.20: Three-phase photovoltaic inverter test setup.

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3. Current Source Inverter Drive of an Ironless Motor for Flywheel Batteries

3.1 Introduction

3.1.1 Motivation

The most common electric drive is a traditional two-level voltage source inverter (VSI). The widespread use of WBG components gave light to new converter and inverter architectures and restored already known ones, which became interesting again. Since SiC, and even more GaN, show higher efficiencies and allow reducing both volume and weight of passive filters. Among these architectures, the CSI inverter became popular again. The world of electrical drives is still dominated by voltage source inverters (VSIs) which are more simple and require a lower number of switches. Its high efficiency, simplicity, and widespread availability of voltage sources make it the de facto standard solution. Current source inverters (CSI), on the other hand, have never been popular because of their difficult implementation. An additional diode is required in a series to the transistor, in order to ensure its reverse-blocking capability, thus doubling the conduction losses. Moreover, a CSI requires a DC input inductor that may be bulky and heavy due to the limitation of the maximum frequency of the power switches. Eventually, CSI requires a current source and a pre-stage preserving the continuity of the current on the DC inductor, degrading the overall performance of the system. Even though some efforts have been made recently on the elimination of the pre-stage, this achievement is still very recent and should also be studied in comparison with a traditional VSI in terms of efficiency, although it is very promising [1],[2]. The new switching devices feature: higher switching frequencies; reverse-blocking capability and lower conduction losses. Hence, the dimensions of the input inductor can be reduced and an additional diode will be avoided in the future with the emerge of GaN bi-directional switches. Specific advantages of CSI make them an attractive solution for some niche applications. CSI directly modulates the current, which means a simpler current control and the DC inductor limits overcurrent in case of phase leg shoot-through [3]. In addition, CSI's low output-voltage total harmonic distortion reduces stress on the insulation systems of both

the electric machine and the converter. Due to its inherent voltage boost capability, CSI is ideal for high-speed drives limited by low DC link voltages, delaying the flux weakening operation [4]. At high-speed and higher frequency, the size of the DC inductor can be further decreased. In conclusion, the power density is increased [5] because of the absence of electrolytic capacitors and of the above mentioned features.

On the other hand, the main drawback of a CSI is represented by higher conduction losses: four devices are always on and a pre-stage is needed. New topologies have been investigated: an additional leg that conducts during the overlapping periods, reducing the conduction losses [6]. Eventually, it may be possible to avoid the pre-stage in high-speed drives [7].

The performances of a CSI-fed drive for flywheel battery based on a ironless machine are assessed. A prototype ironless machine, named MechSTOR, was specifically designed and realized for a flywheel energy storage system (FESS) [8]. In an ironless machine, the linked fluxes between phases must cross high reluctance paths of air and PM, thus reducing inductance values and filtering capability.

For a VSI-fed ironless machine, the current and torque ripple can be reduced with high switching frequency and large filtering inductors, thus increasing switching losses. On the other hand, for a CSI-fed ironless machine, the current waveform are excellent, reducing harmonic distortion of the supply current even at lower switching frequency.

Performance of CSI and VSI for MechSTOR supply are compared from the standpoint of the phase currents THD and torque ripple. MechSTOR, VSI-fed and CSI-fed drives are modeled in PLECS in the same conditions, i.e. by keeping the same switching frequency and simulation parameters. subsection 3.2 provides a brief presentation of the flywheel energy storage system and of the MechSTOR prototype. In subsection 3.3, the simulation models of both VSI-fed and CSI-fed drives are presented; subsection 3.4 reports compared performances. Eventually, conclusions are drawn in subsection 3.5.

3.2 Flywheel Energy Storage Systems and MechSTOR

In Flywheel Energy Storage Systems (FESS), the electric energy is stored as the kinetic energy of a rotating flywheel and an electric motor/generator is used for the electro-mechanical conversion. FESS feature a number of advantages with respect to chemical batteries: a immediate charging time; higher lifetime; lower environmental impact and lower costs. FESSs are ideal for applications that require frequent charge/discharge operations, and fast response time [9].

However, their self-discharge duration time is a critical parameter [10]. It is defined as the amount of time in which the system is able to keep the stored energy if disconnected from the source and the load and it must be extended to increase their competitiveness. Self-discharge duration time is strictly dependent on losses. Mechanical losses can be reduced using high performance bearings; and the entire system has to be sealed in a vacuum chamber. The most critical electromagnetic losses are iron losses that can result in self-braking effect even when the power supply is disconnected. The MechSTOR prototype is a ironless machine: the stator windings were encapsulated in epoxy resin to minimize iron-core losses. This solution was already proposed for FESSs with different configurations [11], [12].

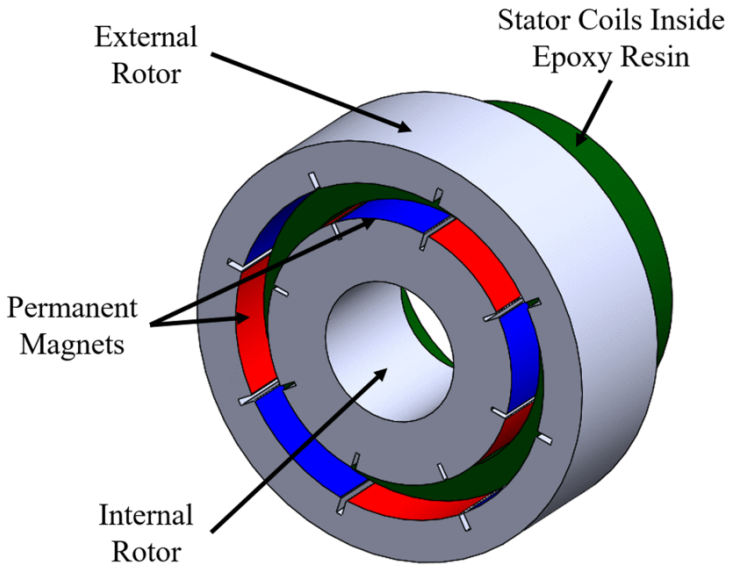


Figure 3.1: MechSTOR's dual rotor topology [8].

Table 3.1: Motor Parameters.

Name	Value
Stator Resistance R_s	1.375 Ω
Stator Inductance L_s	1.25 mH
Poles Number P	8
PM Flux Linkage λ_{PM}	0.16 Vs
Rated Torque T	3.67 Nm
Rated Current I_s	1.375 A_{rms}
Minimum operating speed ω_{ref}	1500 rpm
Reference speed ω_{ref}	6000 rpm
Maximum operating speed ω_{ref}	9000 rpm

A drawback of ironless machines is the increased reluctance of the core, which is partly compensated by a dual-rotor configuration, that minimizes the magneto-motive force (MMF) drops along magnetic flux paths, Figure 3.1. The dual-rotor topology: outer rotor, stator and inner rotor allows splitting the air gap in two: for a fixed outer diameter it allows a higher torque-per-ampere, which is useful due to the mechanical constraints. However, the mutual coupling between phases is lower because the linked fluxes must cross high-reluctance paths of air and magnets. The mutual coupling between the phases is further reduced because a concentrated winding was adopted. This lower value for the mutual coupling causes a lower overall value for the phase inductances and a lower filtering capability of the supply currents. The current and the torque ripple shall be reduced by large size filtering inductors and by high switching frequency. The former increases the size and weight of the power converter; the latter increases switching losses. Motor/generator parameters are listed in 3.1. Here the motor characteristics were described briefly, author reminds to [8] for any mechanical or electrical specification, that is not mentioned above.

3.3 Modeling of VSI-fed and CSI-fed Drives

The complete motordrive, with control system, VSI/CSI and MechSTOR machine, was modelled in PLECS. SiC MOSFETs s4101 [13] and SiC Schottky diodes s6305 [14] were chosen for both VSI and CSI. PLECS allows to automatically compute total conduction and switching losses of the inverter thanks to the thermal model of devices, obtained from their datasheets. Specifically, PLECS allows to upload a 3D look-up table for the switch-on losses, E_{on}, as a function of the blocking voltage over the transistor v_{DS}, the drain-current i_D and the junction temperature T_j, then the software linearly interpolates the losses between two given values. An equivalent look-up table can also be created for the switch-off losses E_{off}. These look-uo tables are critical, as well as the values for E_{on} and E_{off}.

A MATLAB algorithm extrapolates the data for each (i_D, v_{DS}) couple, taking into account several aspects: the non-linear dependency between the channel current i_{ch} and the gate-source voltage v_{GS} and the gate-drain C_{GD}; the variation of capacitance C_{rss} with v_{DS}. The first relation is defined by (3.1), considering that during the current rise in turn-on and during the current fall in turn-off the transistor is in a channel modulation condition. The channel current i_{ch} is otained by the following iteration:

$$i_{ch} = k_1 \cdot (v_{GS} - V_{th})^x + k_2 \tag{3.1}$$

where the coefficients k_1, k_2, and x are extrapolated by devices datasheets and V_{th} is the threshold voltage. A mean weighted value C_{rss} was computed for for both voltage drop and rise, during turn-off and turn-on, respectively, thanks to a step-by-step approach. Turn-on and turn-off losses were calculated with the relationships (3.2).

$$\begin{cases} E_{on} = E_{on,t_{ri}} + \frac{1}{2} V_{DC} I_0 \cdot t_{fu} \\ E_{off} = E_{off,t_{fi}} + \frac{1}{2} V_{DC} I_0 \cdot t_{ru} \end{cases} \tag{3.2}$$

where $E_{on,t_{ri}}$, $E_{off,t_{fi}}$ are the losses caused by current rise and drop, respectively; and t_{fu} and t_{ri} are drop-time and rise-time, respectively. In a switching period, the power switching losses P_{sw} can be obtained by (3.3).

$$P_{sw} = (E_{on} + E_{off}) \cdot f_{sw} \tag{3.3}$$

PLECS can compute conduction losses too, adding the conduction characteristic curve to the thermal model. For SiC Schottky diodes, conduction losses are the only losses. Moreover, the reverse-recovery is not an issue for these devices. The thermal parameters: resistance R_{th} and capacitance C_{th} are modeled in PLECS by a thermal chain. Since thermal and electrical worlds are separated in PLECS, the efficiency has been computed as shown in (4.5):

$$\eta = 1 - \frac{P_{loss}}{P_{in}} \tag{3.4}$$

where P_{in} is the input power provided by the source and P_{loss} are the total losses, considering all the devices. This method was evenly applied to both converters. The losses on the input

filtering capacitor for the VSI, and the input filtering inductor for the CSI have not been taken into account. For any converter employing SiC technology, the most challenging task is always represented by the modeling and simulation of switching losses, and the model reported here is the same as described in detail in Chapter 1 and published in [15]. Simulations were carried out for both converters under the same conditions, with the parameters listed in Table 3.1 and the performances were estimated steady state. Simulations were repeated for different values of the switching frequency: 40 kHz, 60 kHz, 80 kHz and 100 kHz.

3.3.1 Voltage Source Inverter

For VSI, the traditional architecture with filtering input capacitor was chosen and no output filter was used (Figure 3.2). The machine was operated in Maximum Torque Per Ampere (MTPA) mode with $\pi/2$ nominal angle and Space Vector Modulation (SVM).

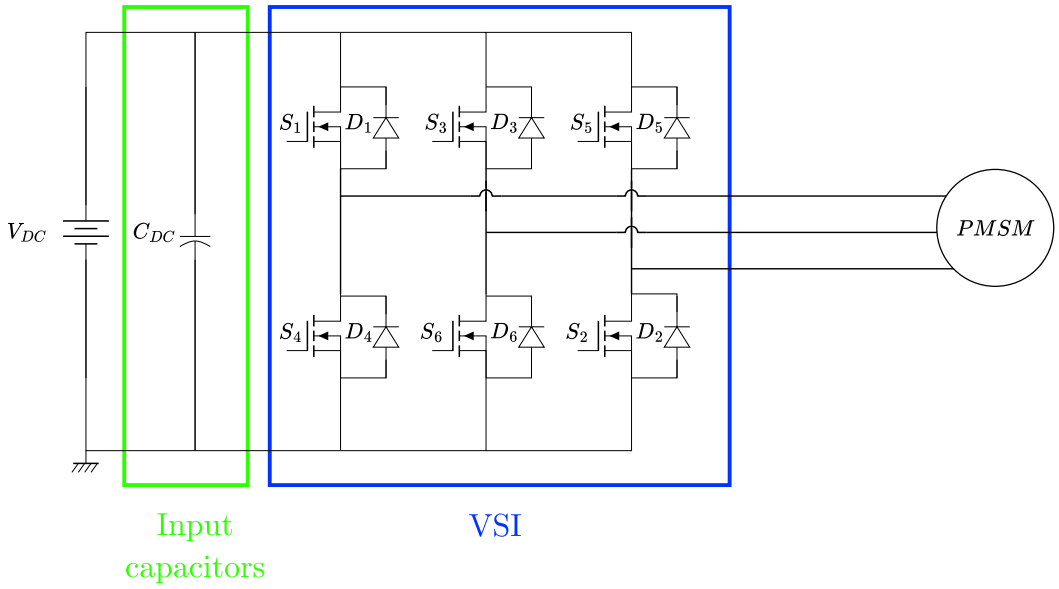


Figure 3.2: VSI architecture.

3.3.2 Current Source Inverter

For CSI, a six switches architecture was chosen, with the pre-stage, the input inductors and the output filtering capacitors, as shown in Figure 3.3. When the output voltage is smaller than the input voltage, the CSI behaves as a boost converter, hence, it is not possible to obtain a good control of the input DC current without a pre-stage. A bidirectional PWM boost was chosen as a pre-stage, in order to keep constant the input current source. The CSI was

modulated with SVM too. A main difference with VSI happens during the zero state, when a shoot-through of one leg occurs that creates a re-circulation path for the current because of the presence of the inductor. During this zero state, CSI provides its boost effect on the output voltage. For this reason, an overlap between active and zero states is required to prevent an over voltage on the power devices (opposite to the dead-time required for VSI). In addition to that, Field-Oriented Control for CSI-fed drives is different from VSI-fed drives because there are no reference voltages and reference currents are directly modulated from the DC link current. A peculiar alternated SVM technique was employed for the CSI, but a detailed description of this modulation technique will be explained in detail in Chapter 4.

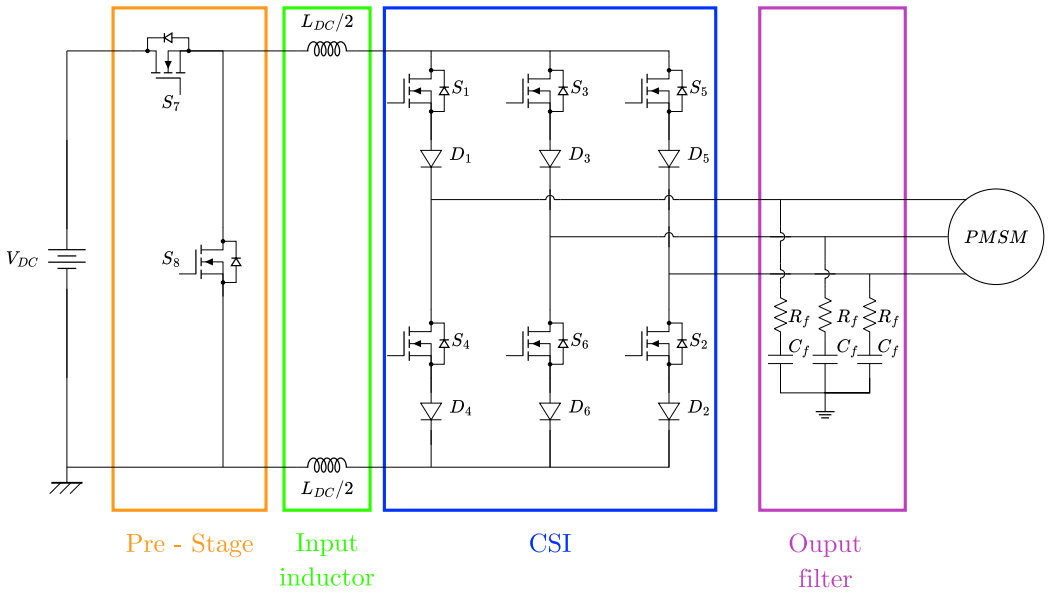


Figure 3.3: CSI architecture.

3.4 CSI/VSI Simulation results

The phase currents and output torque waveforms for the VSI-fed drive at 40 kHz switching frequency during two electrical periods are shown in Figure 3.4, a) and b) respectively. In this case, a current THD of about 11 % and a peak-to-peak torque ripple of about 1.4 Nm were obtained. This level of THD is not acceptable for industrial applications, and a significant torque ripple appears because of the low filtering capability of the ironless machine. Figure 3.5, a) and b) respectively show the same signals obtained with the CSI. The quality of the waveforms is superior with a current THD of about 1.1 % and the peak-to-peak torque ripple is reduced at 0.16Nm with a switching frequency of 40 kHz. It should be clarified that the ripple

over the average torque is due to the PWM harmonics injected by the drive and the low phase inductance of the motor.

As for inverter losses, the average value over one switching period and the efficiency in steady state were computed. Even if CSI has more devices because of the presence of the pre-stage, its losses are slightly lower with a value of about 80 W compared to the 108 W of the VSI at 40 kHz switching frequency. In fact, CSI losses are mainly composed of the pre-stage losses that are about twice the losses of the actual inverter stage (56 W and 25 W, respectively). In Chapter 1 the problem of modeling any loss in the magnetic was exposed, especially if a custom inductor is needed. Therefore, in the efficiency computation, losses on the input inductor were not taken into account for the CSI-drive. To avoid an unbalanced comparison, the input capacitor losses were also omitted, although the author is aware that they are less prominent with respect to the losses on the input inductor. The estimated values for current THD %, peak-to-peak torque ripple, and inverter efficiency are summarized in Figure 3.6 and Figure 3.7 for increasing values of the switching frequency. As visible, current waveforms and torque ripple, obtained with a CSI-drive, are highly superior even at lower frequencies; the efficiency is slightly superior too. Hence, CSI outperforms VSI in this specific application.

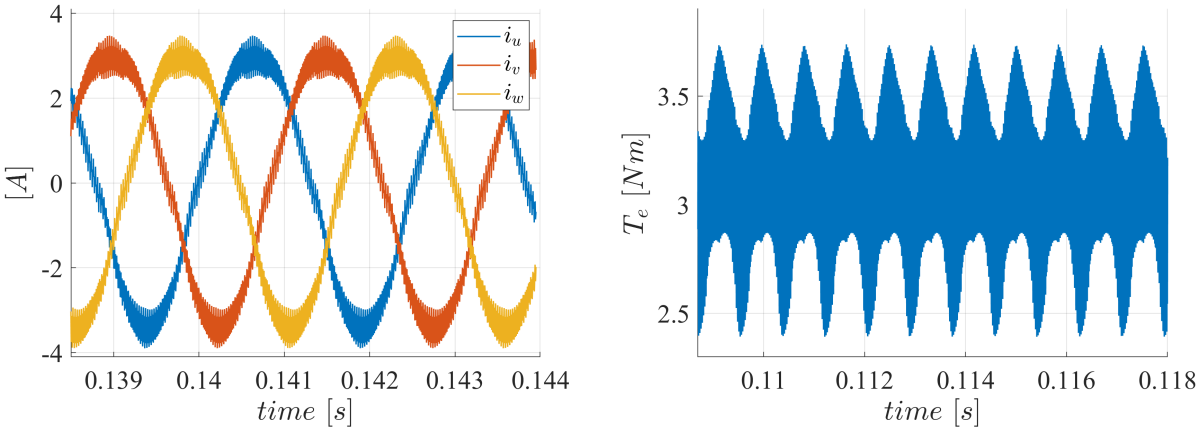
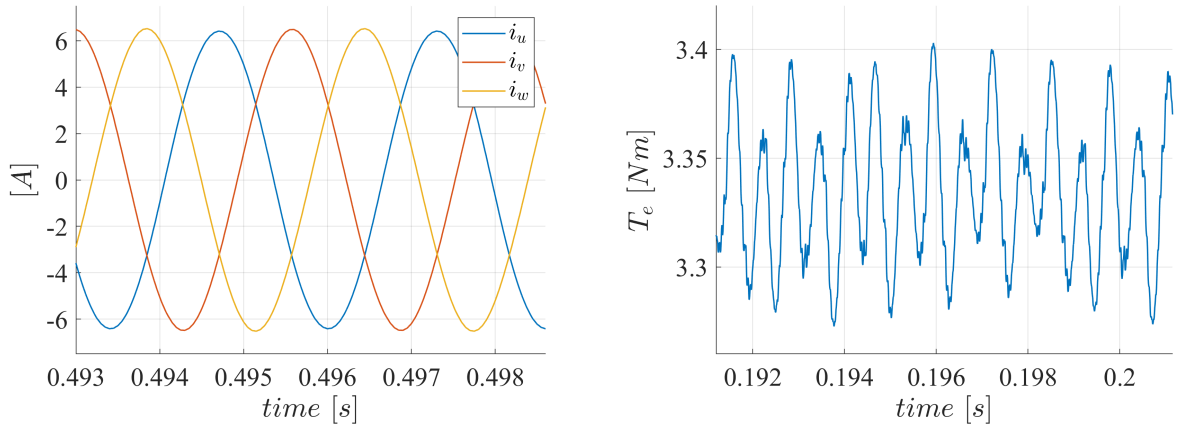


Figure 3.4: VSI-fed simulation results: a) motor phase currents and b) output electrical torque.

3.5 CSI/VSI Comparison conclusions

The first comparison was based on the performances of a CSI-fed drive and a conventional VSI-fed drive for a FESS application. The flywheel battery is based on an ironless motor/generator that has quite low inductance values, which means a low filtering capability for the supply



(a) (b)

Figure 3.5: CSI-fed simulation results: a) motor phase currents and b) output electrical torque.

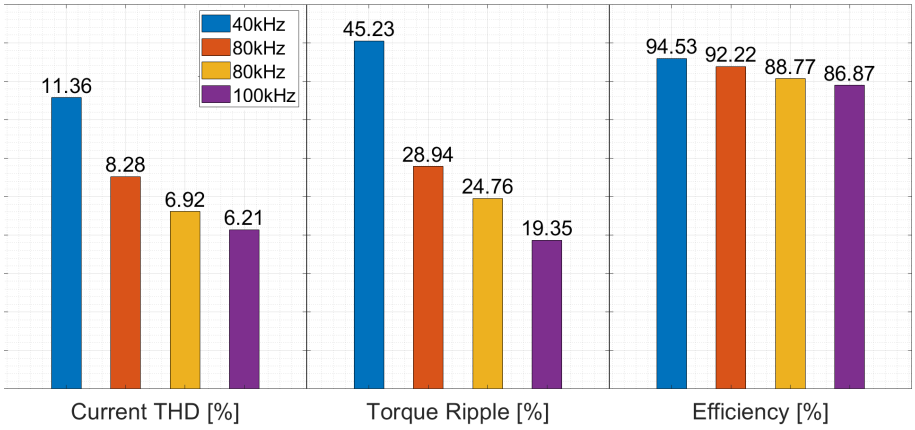


Figure 3.6: Current THD, torque ripple and efficiency obtained for VSI at different switching frequencies.

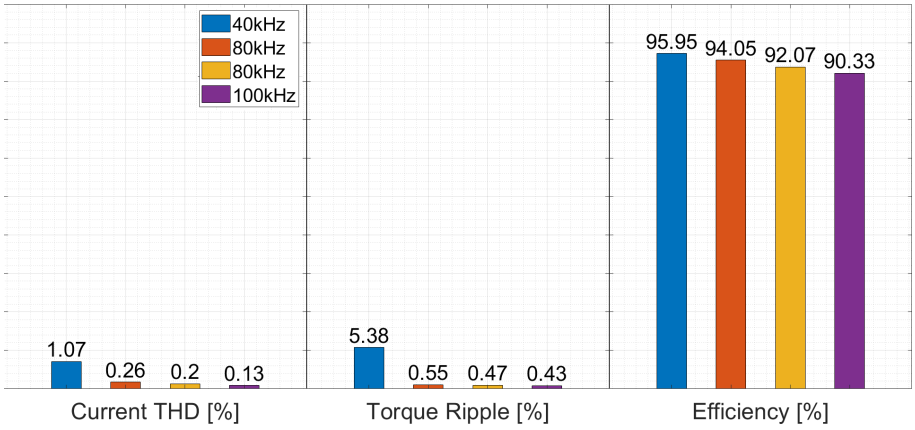


Figure 3.7: Current THD, torque ripple and efficiency obtained for CSI at different switching frequencies.

currents. Hence, the quality of supply current waveforms is of the utmost importance to prevent high current ripple. Both VSI-fed and CSI-fed drives were modeled and simulated with the same parameters to compare their current and torque ripples and total inverter losses. The simulation results show that the performances of CSI are better both in terms of harmonic distortion and losses. Here, the comparison is based on inverter losses only. The performances of CSI-fed drives would be even when we consider motor losses also. In fact, the torque ripple decreases the performance of the electric motor and hence, its conversion efficiency. In addition to that, losses in the permanent magnets highly depend on the current ripple and a low THD of the current is required to prevent the risk of magnet demagnetization and overheating. These benchmarks are even more important for the FESS applications, where all the losses must be minimized in order to increase the self-discharge duration time. These features will also result in a reduction of vibrations, a feature that is best suited to magnetic bearings that will be used in the final application.

Eventually, in this application it could be possible to remove the pre-stage, the main loss source for the CSI, increasing its performance even more. In fact, the pre-stage is needed only when the back-EMF is lower than the DC bus voltage. In FESS, the electric motor has to work for almost all the time at high speed and the minimum speed value is regulated to avoid energy-consuming start-ups. Hence, the pre-stage would be needed only during the initial start-up, and, once high speed is reached, CSI could be directly connected to the DC bus voltage. CSI would operate in boost mode most of the time, allowing a lower DC link voltage source.

In conclusion, CSI proves to be a highly convenient solution for the MechSTOR prototype and FESS application. Motor losses which were excluded here can be significant, especially when this type of prototype is powered by a VSI. Current ripples on the motor phases leads to both unstable torque and PWM losses on windings and magnets. It is awaited that these losses will be significantly lower when the motor/generator is powered by a CSI. The lack of a precise and profound study on the AC losses of an ironless machine brought to an extension of the work in this sense. In the following sections this research activity is described in details, but experimentally and analytically.

3.6 Extension of the work on MechSTOR machine

As discussed in the previous subsection, ironless machines exhibit lower reactance than conventional ones, resulting in higher current ripple at PWM frequencies (10–20 kHz), which induces

significant eddy currents due to skin and proximity effects [16]. AC losses, influenced by winding configuration and these effects, cannot be accurately assessed via DC resistance alone. In [17], an analytical method was proposed to estimate AC losses by relating R_{AC} to R_{DC} through a simple DC measurement.

In [18] a fast finite element (FE)-based method was proposed to compute AC losses in the stator windings. Although the method is applicable to any type of electrical machines windings, the analysis is limited to conventional slot geometries with an iron-core stator, while magnetic losses are beyond the scope of this study. Hairpin windings were also investigated: these are very suitable for high-speed applications [19], [20].

The conductor count and slot arrangement significantly affect AC resistance. Studies have examined strand configuration and transposition to model their impact on losses [21], [22]. Various layouts were evaluated in [23] to reduce AC losses in high-speed machines. Most analyses rely on 2D-FEA, which balances accuracy and efficiency better than complex analytical models [24]. Although 3D-FEA is also used, authors of [25] introduced a hybrid approach that combines analytical and 3D simulations for more comprehensive modeling.

AC losses in ironless machines are still underexplored. A simplified 3D-FEA was used in [26], though without experimental validation. In [27], an axial flux ironless machine with a PCB stator was analyzed using an optimization algorithm, but losses in windings and magnets were not differentiated. The extension of the study employs a 2D-FEA to evaluate AC losses in both components of a dual-rotor ironless machine, with a focus on inverter-fed configurations. Results gave strength to the idea of employing a CSI to power these machines. The research was conducted on the MechSTOR prototype, mentioned in the previous sections.

This second part of the chapter is organized as it follows: subsection 3.7 reviews the main drawbacks of the ironless topology related to the AC motor losses, subsection 3.8 introduces the modeling of stator and magnet losses using both approximate and exact methods, with the former offering good accuracy and reduced computation time. Experimental tests on a rotor-locked prototype (subsection 3.9) enabled separation of copper and magnet losses. Results are compared with 2D-FEA simulations in subsection 3.10. Subsection 3.11 further discusses the benefits of CSI supply, while subsection 3.12 concludes and suggests future research directions.

3.7 Ironless machine drawbacks

The MechSTOR prototype, designed in [8], is tested and the motor/generator topology is the same described in Figure 3.1. It consists of an ironless machine where the stator windings are encapsulated in epoxy resin to minimize iron core losses. A drawback of this machine topology is the increased reluctance of the core, which is partly compensated by the dual-rotor configuration, which minimizes the magnetomotive force (MMF) drops along magnetic flux paths. However, the mutual coupling between phases remains low because the linked fluxes must cross high-reluctance paths of air and magnets. Furthermore, the mutual coupling is reduced as a result of the adoption of a concentrated winding configuration. These design choices inevitably result in lower overall phase inductance values and a reduced filtering capability of the supply currents. Magnets are monolithic, not segmented, slices made of NdFeB-35SH, and they are placed on the outer surface of the internal rotor and on the inner surface of the external rotor. When the machine is fed by a three-phase VSI, the current ripple on the motor phases becomes relevant along with the AC losses on both the magnets and the stator windings. This issue highlights the need for an AC loss estimation method tailored to this electrical machine topology, which is unconventional and has not yet been thoroughly analyzed in the literature. Therefore, in the following sections, the proposed method will be presented, and accurate experimental investigations will be conducted under various conditions.

3.8 AC losses simulation

3.8.1 Overview of the literature

To assess motor losses caused by both fundamental and carrier harmonics, it is necessary to evaluate the contributions imputable to both windings and permanent magnets. Winding losses consist of two primary components: skin effect losses and proximity effect losses. Skin effect losses arise from currents induced by the conductor itself as a result of the time-varying magnetic field. In contrast, the proximity effect results from the influence of the magnetic field generated by two or more adjacent conductors. Accurately solving or expressing these effects analytically is challenging. In [16], the author formulates the problem for an inductor with a ferromagnetic core, an approach that can be extended to windings within stator slots. However, an electrical machine is a much more complicated system. Moreover, an ironless

topology does not have slots and the issue of estimating the magnet losses persists. In [17], the ratio R_{AC}/R_{DC} or P_{AC}/P_{DC} was derived and compared with the results of the 2D-FEA simulation, but the authors themselves claim the qualitative approach of the analysis and the significant difference between the two. Furthermore, magnet losses have not been investigated in the paper. The authors of [18] developed a fast finite element-based method to estimate the strand eddy current losses in a randomly wound machine. Although very interesting and applicable to several electric motors, it focuses only on winding losses and comparison with experimental tests only aims to demonstrate the trend of R_{AC}/R_{DC}. The real comparison is made with other FEA methods. Other works, such as [19]–[23] focused on a single slot of a high-speed machine with hairpin windings. Works in [21] and [22] also took strand configuration and transposition into account, but these analyses are limited to a specific case and to an atomic part of the whole electrical machine. All the aforementioned works, along with this research, employed 2D-FEA software to compute the AC losses and, as suggested by [24], do not consider some effects, such as the end-windings which cannot be modeled. However, the 2D or a 3D hybrid and simplified approach is faster, see [25]. Since the issue of eddy current losses for an ironless motor has already been addressed in [26] and [27], a 2D-FEA approach is used to evaluate the AC windings and magnet losses of the MechSTOR prototype.

Before delving into the method, it should be noted that an ironless machine does not have an iron stator. Regarding the iron core of the rotor, losses should be investigated case by case, but for the MechSTOR prototype tested in this work, they appeared to be completely negligible in the simulations. Due to the clear and sound compliance between experimental tests and simulations under different load conditions, shown in subsection 3.10, it is believed that they could be omitted and therefore they are not addressed here.

3.8.2 Proposed method

The AC losses of the ironless stator dual rotor prototype MechSTOR are analyzed through FEMM, an open-source 2D-FEA software. An approximate and computationally convenient method is described here, which is based on the continuum approximation method, proposed by David Meeker [28]. This can be employed to compute both skin and proximity effects in a generic conductor, therefore, it is effective for the windings. The magnets instead do not require any approximation since they are monolithic components. In the next subsection, Meeker's approximated solution to the problem is defined. Although the formulation is completely original by Meeker, a detailed insight and explanation of the equations is given in the next subsection

3.8.2.1. These calculations cannot be found in literature as for which is the candidate's knowledge. The following subsection, explains in details what the software implicitly does. Skip to subsection 3.8.2.2 for the algorithm employed in the study.

3.8.2.1 Meeker's approximated solution to the problem

A general one-dimensional (1D) problem applied to a foil conductor should be considered. The reference foil is the one in Figure 3.8 and the problem is formulated using the 1D Poisson equation for the vector potential (3.5).

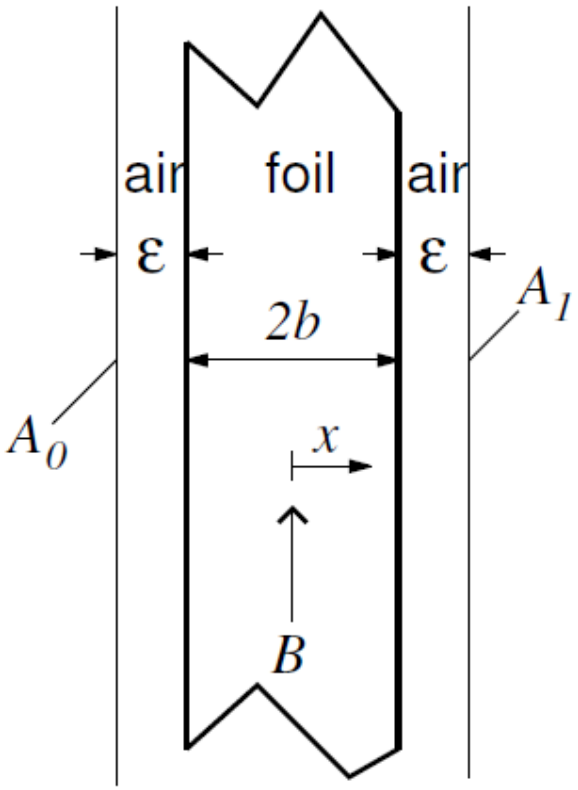


Figure 3.8: Reference foil parameter: ε represents the air (insulating) gap between two foils, $2b$ is the coil width on the x and only dimension, $\vec{B}$ is the direction of the magnetic flux density and both A_0 and A_1 are the extreme values of the vector potential at $-b-\varepsilon$ and $b+\varepsilon$ respectively.

$$\frac{d^2\mathbf{A}}{dx^2} = j\omega\mu\sigma\mathbf{A} + \mu\sigma\nabla v \tag{3.5}$$

The problem is then decomposed into three independent subproblems (3.6), (3.7) and (3.8).

$$\frac{d^2\mathbf{A}}{dx^2} = j\omega\mu\sigma\mathbf{A} \tag{3.6}$$

where $A(\pm b) = \pm\frac{A_1 - A_0}{2}$.

$$\frac{d^2\mathbf{A}}{dx^2} = \mu\sigma(j\omega\mathbf{A} + \nabla v_r) \tag{3.7}$$

where $A(\pm b) = 0$.

$$\frac{d^2\mathbf{A}}{dx^2} = \mu\sigma(j\omega\mathbf{A} + \nabla v_i), \tag{3.8}$$

where $A(\pm b) = \frac{A_1 + A_0}{2}$.

The subdivision in the three subproblems is not trivial. To understand the physical meaning one should refer to the equation of the electrical field (3.9), which gives the general expression.

$$\mathbf{E} = -\frac{\partial\mathbf{A}}{\partial t} - \nabla v \tag{3.9}$$

Considering (3.9) and imposing $\nabla v = 0$ like in the first subproblem corresponds to look for the impedance opposed by the conductor to an external imposed voltage gradient or any external source of $\mathbf{E}$. The 2^{nd}-order differential equation becomes a homogeneous Helmholtz equation. Physically, it would account to the eddy current contribute because of the time varying magnetic field and the fact that $A(-b) = -A(b)$ is the correct boundary condition to apply since it follows that there is no net flux linkage. more than the physical meaning, one should think that the homogeneous problem should be solved anyway and in this sense it is used to find a value for the complex permeability μ_{fD}, that will be used also in the other two subproblems. Finding a complex permeability and than a complex 2^{nd}-order differential equation is the way the approximate solution is found. The second subproblem considers both a reactive component, $\partial\mathbf{A}/\partial t$ and a resistive component ∇v_r imposed externally. The pedicle means that only resistive external electrical field exists, therefore the external field causess only resistive losses through a conservative external $\mathbf{E}$ field. The non-external component varies because of the

local magnetic field, since the boundary conditions impose that the flux cannot exit the foil. Physically, this is the condition of a conductor within a varying current flows, causing resistive DC losses (∇v_r) and skin-effect losses ($\partial \mathbf{A}/\partial t$). The last subproblem instead considers just the inductive/induced component of the electrical field. The source term is inductive (induced by environment or nearby conductors) and the reactive power stored locally by a varying $\mathbf{A}$ is also considered. The flux linkage generated by nearby conductors (proximity effect) is just accounted in this last subproblem. The total voltage gradient is the sum of the resistive and inductive components.

$$\nabla v = \nabla v_r + \nabla v_i \tag{3.10}$$

Each of the three subproblems should be solved separately, and then the solutions should be combined.

The no net flux linkage problem consists of solving the equation in (3.6).

$$A(x) = c_1 \exp\{\sqrt{j\omega\mu_0\sigma_f}x\} + c_2 \exp\{-\sqrt{j\omega\mu_0\sigma_f}x\} \tag{3.11}$$

To find c_1 and c_2, the border solution should be imposed.

$$\begin{cases} c_1 \exp\{\sqrt{j\omega\mu_0\sigma_f}b\} + c_2 \exp\{-\sqrt{j\omega\mu_0\sigma_f}b\} = \frac{A_1 - A_0}{2} \\ c_1 \exp\{-\sqrt{j\omega\mu_0\sigma_f}b\} + c_2 \exp\{\sqrt{j\omega\mu_0\sigma_f}b\} = -\frac{A_1 - A_0}{2} \end{cases} \Rightarrow$$
$$\Rightarrow c_1 = -c_2 = \frac{A_1 - A_0}{2} \cdot \frac{1}{\left[\exp\{\sqrt{j\omega\mu_0\sigma_f}b\} + \exp\{-\sqrt{j\omega\mu_0\sigma_f}b\}\right]} \tag{3.12}$$

$$A(x) = \frac{A_1 - A_0}{2} \cdot \frac{\sinh\left(\sqrt{j\omega\mu_0\sigma_f b^2}\frac{x}{b}\right)}{\sinh\left(\sqrt{j\omega\mu_0\sigma_f b^2}\right)} \tag{3.13}$$

The solution in (3.13) allows finding a single value for the permeability. If the foil is imagined

from the outside, the field intensity which can drive an average flux B_{avg} in the foil is the one in $-b$ or b (it can be demonstrated that here they are equivalent. Since $\mathbf{B}$ has only a y component, A_y is null.

$$\mathbf{H} = \frac{(\nabla \times \mathbf{A})}{\mu_0} = \frac{1}{\mu_0} \cdot \begin{vmatrix} \hat{i} & \hat{j} & \hat{k} \\ \frac{\partial}{\partial x} & \frac{\partial}{\partial y} & \frac{\partial}{\partial z} \\ A_x & A_y & A_z \end{vmatrix} = \frac{\partial A_z}{\partial x}\hat{j} = -\frac{1}{\mu_0} \cdot \frac{dA}{dx} \tag{3.14}$$

It directly follows that in b, H assumes the expression in (3.15).

$$H(b) = \left(\frac{A_0 - A_1}{2\mu_0 b}\right) \cdot \frac{\sqrt{j\omega\mu_0\sigma_f b^2}}{\tanh\left(j\omega\mu_0\sigma_f b^2\right)} \tag{3.15}$$

At the same time, the average field B_{avg} is found by the integral over the dominium of the flux density itself. The definition of the equivalent average permeability will be the ratio of B_{avg} and $H(b)$.

$$B_{avg} = -\frac{1}{2b}\int_{-b}^{+b} \frac{dA}{dx} \cdot dx = -\frac{1}{2b} \cdot [A(b) - A(-b)] = \frac{A_0 - A_1}{2b} \tag{3.16}$$

$$\mu_{fD} = \frac{B_{avg}}{H(b)} = \mu_0 \cdot \frac{\tanh\left(\sqrt{j\omega\mu_0\sigma_f b^2}\right)}{\sqrt{j\omega\mu_0\sigma_f b^2}} \tag{3.17}$$

The last interesting relation, which can be derived from the first subproblem is represented by (3.17).

Regarding the second subproblem, since $A(\pm b) = 0$ by definition: one can obtain the trivial solution $A(x) = 0$, for each $x \in \{-b, b\}$, or there is an inflection point in the domain, so $\partial^2 A/\partial x^2 = 0$ for a $x = p$. A_p represents the particular integral of the second-order differential

equation.

$$-j\sigma_f\mu_0\omega A = \sigma_f\mu_0\nabla v_r \Rightarrow A_p = -\frac{\nabla v_r}{j\omega} \tag{3.18}$$

$$A(x) = c_1 \exp\left\{\sqrt{j\omega\mu_0\sigma_f b^2}\frac{x}{b}\right\} + c_2 \exp\left\{-\sqrt{j\omega\mu_0\sigma_f b^2}\frac{x}{b}\right\} - \frac{\nabla v_r}{j\omega} \tag{3.19}$$

The next step consists of finding c_1 and c_2 for the extreme of the domain. Thus, other cases can be found.

$$\begin{aligned} &\begin{cases} c_1 \exp\{\lambda\} + c_2 \exp\{-\lambda\} - \frac{\nabla v_r}{j\omega} = 0 \\ c_1 \exp\{-\lambda\} + c_2 \exp\{\lambda\} - \frac{\nabla v_r}{j\omega} = 0 \end{cases} \Rightarrow \\ &\Rightarrow (c_1 - c_2)\cdot(\exp\{\lambda\} - \exp\{-\lambda\}) = 0 \Rightarrow \\ &\Rightarrow c_1 = c_2 = -j\frac{\nabla v_r}{\omega}\cdot\frac{1}{\exp\{\lambda\} + \exp\{-\lambda\}} \end{aligned} \tag{3.20}$$

where $\lambda = \sqrt{j\omega\mu_0\sigma_f b^2}$. Then the solution for the vector potential naturally follows.

$$A(x) = j\frac{\nabla v_r}{\omega}\cdot\left[1 - \frac{\cosh\left(\lambda\frac{x}{b}\right)}{\cosh(\lambda)}\right] \tag{3.21}$$

From (3.21), the current density J and its mean value J_{foil} can be found in the foil domain. The procedure always requires the integration over the domain.

$$J = \sigma_f E = -\sigma_f\left(j\omega A + \nabla v_r\right) = \sigma_f\nabla v_r\cdot\frac{\cosh\left(\lambda\frac{x}{b}\right)}{\cosh(\lambda)} \tag{3.22}$$

$$J_{foil} = -\sigma_f\nabla v_r\left[\frac{\tanh(\lambda)}{\lambda}\right] \tag{3.23}$$

The most important relation, which also constitutes one of the building blocks of (3.10) is represented by (3.24). ∇v_r is the voltage gradient component that accounts for resistive losses. The flux linkage due to nearby conductors is instead accounted by ∇v_i, which derives from the solution of the third problem.

$$\nabla v_r = -\frac{\mu_0}{\sigma \mu_{fD}} \cdot J_{foil} \tag{3.24}$$

The flux linkage due to other conductors induces a magnetic field and also eddy currents on the foil conductor under study. In the borders, the vector **A** needs to remain constant because the net density current is zero and because from an outer perspective the same field is applied to both sides. The starting equation is that of (3.8). It should be recalled that $A(\pm b) = \frac{A_0+A_1}{2}$ by definition of the problem. The border formulations of the subproblem derive from the other two subproblems, considering that $A(-b) = A_0$ and $A(b) = A_1$ for the overall problem definition. The most trivial solution is a costant vector potential $A(x) = \frac{A_0+A_1}{2}$ per each $x \in \{-b, b\}$. The solution becomes interesting just to compute a value for ∇v_i that counteracts the density current, making the applied net density current in the subproblem null.

$$J = -\sigma_f E = -\sigma_f \cdot (j\omega A + \nabla v_i) = 0 \Rightarrow \nabla v_i = -j\omega A = -\frac{j\omega(A_0 + A_1)}{2} \tag{3.25}$$

The overall problem can be written again representing μ, A and J as generic complex numbers: μ_{fD}, $\mathcal{A}$ and J_{coil}. The differential equation, becomes the one in (3.26).

$$-\frac{1}{\mu_{fD}} \nabla^2 \mathcal{A} = J_{coil}, \quad with \begin{cases} \mathcal{A}(-b) = A(-b) = A_0 \\ \mathcal{A}(b) = A(b) = A_1 \end{cases} \tag{3.26}$$

The differential equation is solved integrating twice over the domain and substituting the boundary conditions to find the constant c_1 and c_2. Of course, everything is conducted to a 1D problem.

$$\mathcal{A} = \iint_{-b}^{b} (-\mu_{fD} J_{coil}) \cdot dx^2 = \frac{1}{2} \mu_{fD} J_{coil} b^2 \cdot \left[1 - \left(\frac{x}{b}\right)^2\right] + \frac{A_1 - A_0}{2} \cdot \frac{x}{b} + \frac{A_0 + A_1}{2} \tag{3.27}$$

Applying the known theorem to find the average of the complex vector potential, one can find $\mathcal{A}_{avg}$ (3.28).

$$\mathcal{A}_{avg} = \frac{1}{3}\mu_{fD} J_{foil} b^2 + \frac{A_0 + A_1}{2} \tag{3.28}$$

Once the average continuum vector potential representation is found, ∇v_i can be re-written in this way, (3.29), which is the voltage drop due to the ambient field in terms of the continuous representation of the vector potential.

$$\nabla v_i = -j\omega(A_{avg} - \frac{1}{3}\mu_{fD} J_{foil} b^2) \tag{3.29}$$

The two solutions of (3.24) and (3.29) can be summed to find the total voltage gradient (3.30).

$$\nabla v = \frac{J_{foil}}{\sigma_{fD}} + j\omega\mathcal{A}_{avg}, \quad with\, \sigma_{fD} = \left[\frac{\mu_0}{\sigma_f \mu_{fD}} - \frac{1}{3} j\omega\mu_{fD} b^2\right]^{-1} \tag{3.30}$$

For n conductors of the same winding the voltage drop becomes (3.31), when extended in 3D.

$$v = \frac{n \cdot \iiint_V \left(\frac{J_{foil}}{\sigma_{fD}} + j\omega\mathcal{A}_{avg}\right) \cdot dV}{\iint_S dS} \tag{3.31}$$

When a real magnetic is considered, such as an inductor, a transformer or an electric motor: the winding is constituted by several strands, with eventually the option of Litz wires, separated by an insulator (air, papel, resin, etc. . .). Thus, the equivalent continuum representation should account for the insulator as well. The problem can be divided in the same three sub problems, mentioned above. The derivation of the two voltage gradients ∇v_r and ∇v_i is gonna change in accordance to the e effective permeability μ_{eff} and the effective conductivity σ_{eff}. They both consider the weighted average of the conductor and insulation material properties. The effective values are indeed the average value that FEMM software considers in the continuum representation. On the interface region the vector potential should remain the same:

discontinuity is not admitted.

$$\begin{cases} -\frac{1}{\mu_{fD}}\frac{d^2A}{dx^2} = J_{foil}, \quad for\,|x| \leq b \\ -\frac{1}{\mu_0}\frac{d^2A}{dx^2} = 0, \quad for\,b \leq x \leq b+\varepsilon \end{cases} \tag{3.32}$$

$$\begin{cases} A_1 = -\frac{1}{2}\mu_{fD}J_{coil}\cdot x^2 + c_{1,1}x + c_{2,1}\Big|_{A_1(-b)=A_2(b)}^{A_1(b)=A_2(b)} & for\,|x| \leq b \\ A_2 = c_{1,2}x + c_{2,2}\Big|_{A_2(b)=A_1(b)}^{A_2(b+\varepsilon)=0} & for\,b \leq x \leq b+\varepsilon \end{cases} \tag{3.33}$$

$$H_1(b) = H_2(b) = -\frac{1}{\mu_{fD}}\frac{dA_1}{dx} = -\frac{1}{\mu_0}\frac{dA_2}{dx} \Rightarrow J_{coil}b - \frac{c_{1,1}}{\mu_{fD}} = -\frac{c_{1,2}}{\mu_0} \tag{3.34}$$

The system of four equations is described by the following.

$$\begin{cases} c_{1,2}\cdot(b+\varepsilon) + c_{2,2} = 0 \\ c_{1,2}b + c_{2,2} = -\frac{1}{2}\mu_{fD}J_{coil}b^2 + c_{1,1}b + c_{2,1} \\ J_{coil}b - \frac{c_{1,1}}{\mu_{fD}} = -\frac{c_{1,2}}{\mu_0} \\ -\frac{1}{2}\mu_{fD}J_{coil}b^2 + c_{1,1}b + c_{2,1} = -\frac{1}{2}\mu_{fD}J_{coil}b^2 - c_{1,1}b + c_{2,1} \end{cases} \Rightarrow$$

$$\Rightarrow \begin{cases} c_{2,2} = \mu_0 J_{coil}b\cdot(b+\varepsilon) \\ c_{2,1} = \mu_0 J_{coil}b\varepsilon + \frac{1}{2}\mu_{fD}J_{coil}b^2 \\ c_{1,2} = -\mu_0 J_{coil}b \\ c_{1,1} = 0 \end{cases} \tag{3.35}$$

Substituting in (3.33), one can find:

$$\begin{cases} A_1 = J_{coil} \cdot \left[\frac{1}{2}\mu_{fD} \cdot (b^2 - x^2) + \mu_0 b\varepsilon\right] \quad for,\ |x| \leq b \\ A_2 = \mu_0 J_{coil} b \cdot + (b - x + \varepsilon)\,, \quad for\, b \leq x \leq b + \varepsilon \end{cases} \tag{3.36}$$

The continuum representation of the complex vector potential field over the foil will be the average on $[-b, b]$.

$$\mathcal{A}_{foil} = \frac{1}{2b}\left\{\int_{-b}^{b} J_{coil} \cdot \left[\frac{1}{2}\mu_{fD} \cdot \left(b^2 - x^2\right) + \mu_0 b\varepsilon\right] dx\right\} = \frac{1}{3}\mu_{fD} J_{coil} b^3 + \mu_0 b\varepsilon \tag{3.37}$$

From (3.37), the expression of ∇v_r derives for gapped conductors.

$$-\nabla v_r = \frac{J_{foil}}{\sigma_{fD}} + j\omega\mathcal{A}_{foil} \Rightarrow -\nabla v_r = \left(\frac{\mu_0}{\sigma_f \mu_{fD}} + j\omega\mu_0 b\varepsilon\right) \cdot J_{foil} \tag{3.38}$$

Considering $J_{avg} = [b/(b + \varepsilon)] \cdot J_{foil}$ the average actual current density in the homogeneous region. That because J_{avg} is just a part of J_{foil}.

$$\nabla v_r = -\left[\frac{\mu_0}{\sigma_f \mu_{fD}} \cdot \frac{b + \varepsilon}{b} + j\omega\mu_0\varepsilon \cdot (b + \varepsilon)\right] \cdot J_{avg} \tag{3.39}$$

The third subproblem can also be formulated with an effective permeability.

$$-\frac{1}{\mu_{eff}}\nabla^2\mathcal{A} = J_{avg}, \quad with\ \mu_{eff} = \left(\frac{b}{b + \varepsilon}\right)\mu_{fD} + \left(\frac{\varepsilon}{b + \varepsilon}\right)\mu_0 \tag{3.40}$$

It naturally follows the expression of $\mathcal{A}$ for the third subproblem integrating twice over the

domain $[-b-\varepsilon; b+\varepsilon]$.

$$\mathcal{A} = \frac{1}{2}\mu_{eff} J_{avg} (b+\varepsilon)^2 \cdot \left(1 - \left(\frac{x}{b+\varepsilon}\right)^2\right) + \frac{A_1 - A_o}{2} \cdot \frac{x}{b+\varepsilon} + \frac{A_o + A_1}{2} \tag{3.41}$$

Averaging over the whole domain of the gapped conductor, one can obtain the expression of $\mathcal{A}_{avg}$.

$$\mathcal{A}_{avg} = \frac{1}{3}\mu_{eff} J_{avg} (b+\varepsilon)^2 + \frac{A_o + A_1}{2} \tag{3.42}$$

The third sub-problem leads to the computation of the inductive contribution ∇v_i.

$$\nabla v_i = -j\omega \mathcal{A}_{avg} + \frac{1}{3} j\omega \mu_{eff} J_{avg} (b+\varepsilon)^2 \tag{3.43}$$

Consequently, the voltage gradient also changes and is expressed in (3.46) as the sum of the resistive and inductive components, given in (3.39) and (3.43), respectively.

$$-\nabla v = \left[\frac{\mu_0}{\sigma_f \mu_{fD}} \cdot \frac{b+\varepsilon}{b} + j\omega\mu_0\varepsilon \cdot (b+\varepsilon)\right] J_{avg} + j\omega \mathcal{A}_{avg} - \frac{1}{3} j\omega \mu_{eff} J_{avg} (b+\varepsilon)^2 \tag{3.44}$$

$$-\nabla v = J_{avg} \cdot \left[\frac{\mu_0}{\sigma_f \mu_{fD}} \cdot \left(\frac{b+\varepsilon}{b}\right) + j\omega\mu_0\varepsilon \cdot (b+\varepsilon) - \frac{1}{3} j\omega \mu_{eff} (b+\varepsilon)^2\right] + j\omega \mathcal{A}_{avg} \tag{3.45}$$

$$\nabla v = -\frac{J_{avg}}{\sigma_{eff}} + j\omega A_{avg} \tag{3.46}$$

where the relation between the foil current density and the average current density over the region of the gapped conductor is expressed by: $J_{avg} = b/(b+\varepsilon) \cdot J_{foil}$ and μ_{eff} is the effective permeability of the dominium, i.e. a weighted sum of the coil and the insulator (air)

permeability, (3.47). Finally, σ_{eff} is expressed in (3.48).

$$\mu_{eff} = \left(\frac{b}{b+\varepsilon}\right) \cdot \mu_{fD} + \left(\frac{\varepsilon}{b+\varepsilon}\right) \cdot \mu_0 \tag{3.47}$$

$$\sigma_{eff} = \frac{1}{\left[\left(\frac{b}{b+\varepsilon}\right)\mu_{fD} + \left(\frac{\varepsilon}{b+\varepsilon}\right)\mu_0 - \frac{1}{3}j\omega\mu_{eff}(b+\varepsilon)^2\right]} \tag{3.48}$$

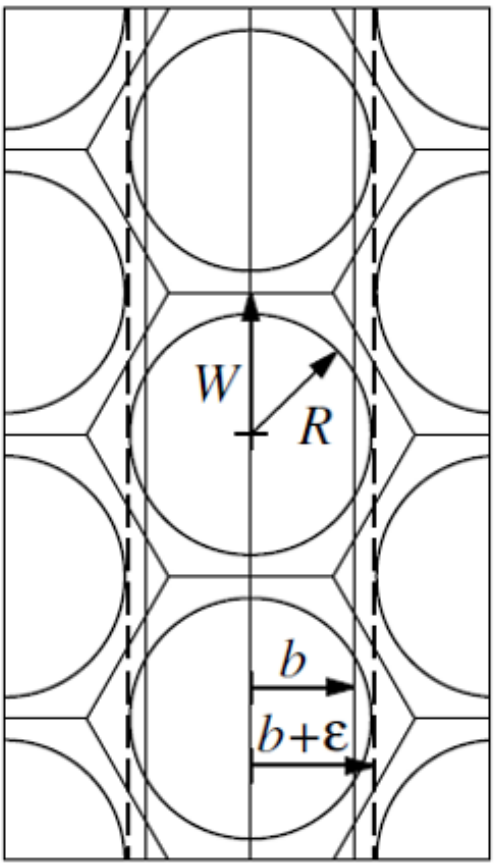


Figure 3.9: Hexagonally packed conductors: W is the hexagon apothem and R is the radius of the round coil.

The equivalent foil problem with an insulator can be extended for the continuum representation in 2D, considering the pitch $b+\varepsilon$ as the diagonal of the hexagon, see Figure 3.9. The equivalent foil of pitch $b+\varepsilon$ and width b allows to obtain the same results over a frequency range. These are the chosen conditions:

1. **DC losses** in the winding must match the DC losses in the equivalent foil.

2. **Low freq. Proximity losses** are identical for the winding and the equivalent foil.

3. $b + \varepsilon$ corresponds to the pitch of the columns in the hexagonal winding.

Considering that the fill factor defines the percentage hexagon area that is filled with winding (conductive material), the following equations can be written for the first and third conditions.

$$\left(W \cdot \frac{W\sqrt{3}}{2}\right) = fill \cdot \pi R^2 \Rightarrow W = R\sqrt{\frac{\pi}{2\sqrt{3}fill}} \tag{3.49}$$

$$b + \varepsilon = \frac{\sqrt{3}}{2}W = R\sqrt{\frac{\pi\sqrt{3}}{8fill}} \tag{3.50}$$

The second condition instead is applied considering a uniform field B at the center of the foil winding. Power losses at low frequencies due to the proximity are then expressed in this way (perpendicularity of the magnetic through the section). Integrating over $2b$ and $2W$.

$$\begin{cases} \frac{l}{2\sigma} \cdot \pi \int_0^R \int_0^R |J|^2 \, dr^2 = \frac{l\pi}{2\sigma} \cdot \int_0^R \int_0^R \sigma^2 \left(-\frac{dA}{dt}\right)^2 dr^2 = -\frac{l\pi\sigma\omega^2}{2} \cdot \int_0^R \int_0^R B^2 r^2 dr^2 \\ \frac{l}{2\sigma_{coil}} \cdot \pi \int_{-W}^W \int_{-b}^b |J|^2 \, dwdx = \frac{l\pi\sigma_{coil}\omega^2}{2} \cdot \int_{-W}^W \int_{-b}^b |A|^2 \, dwdx = \; -\frac{l\pi\sigma_{coil}B^2\omega^2}{2} \cdot \int_{-W}^W \int_{-b}^b x^2 dwdx \end{cases} \tag{3.51}$$

The losses at low frequencies in the foil and in the hexagonally packed coil are given by (3.52).

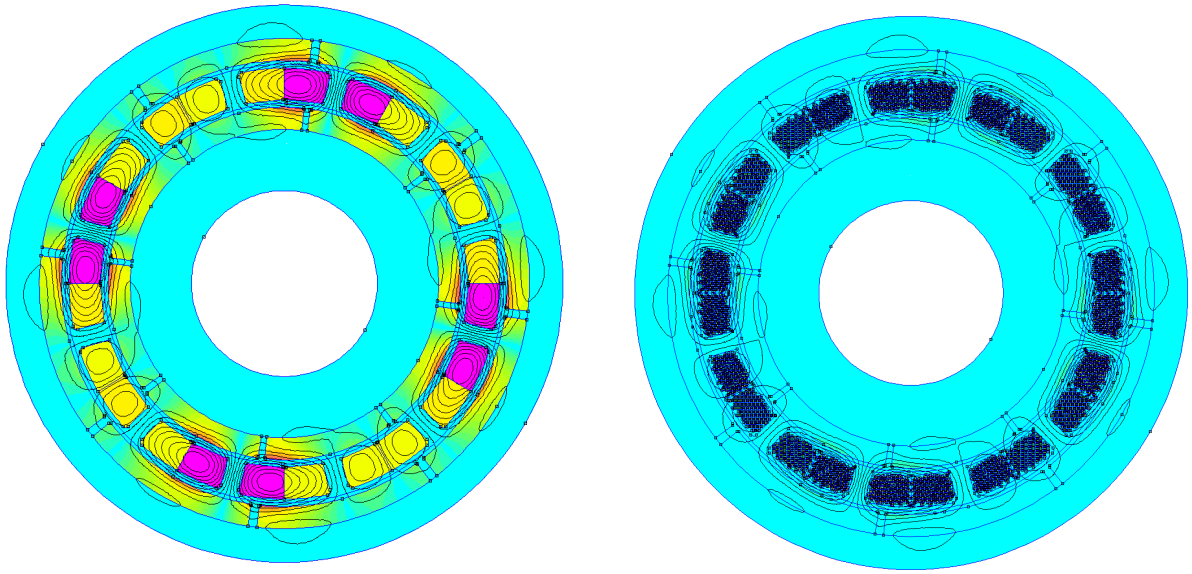
$$\begin{cases} P_{loss,hex} = -\frac{l\pi R^4 \sigma B^2 \omega^2}{8} \\ P_{loss,foil} = -\frac{2l\pi b^3 W \sigma_{coil} B^2 \omega^2}{3} \end{cases} \tag{3.52}$$

If these are forced to be equals and assuming symmetry in all spatial directions, this leads to

(3.53).

$$\begin{cases} b = \frac{\sqrt{3}}{2} R \\ \sigma_{foil} = \frac{\sigma \pi R}{2\sqrt{3} W} = \sqrt{\frac{fill \cdot \pi}{2\sqrt{3}}} \end{cases} \tag{3.53}$$

where σ_{foil} is the conductivity of the equivalent foil, σ is the conductivity of the round wire, $fill$ is the fill factor of the hexagonally packed winding and W is the hexagon apothem and R is the radius of the round coil.



(a) **(b)**

Figure 3.10: FEMM simulations at f_{sw}: a) *Approximate method*; b) *Single conductors method*, with a focus on the current density distribution on the single conductors.

The continuum approximation is very useful to reduce the simulation time, giving a good estimation of the real AC losses even if it does not allow to visually spot the current density distribution. In FEMM software it is sufficient to the define the area where the windings are placed, assign copper material to that area and specify the diameter of the the single conductor. From this point on, this procedure will be referred as *Approximate method*. The *Single Conductors method*, instead, considers the drawing of each single conductor constituting the coil. The difference between the two approaches is shown in Figure 3.10. The single conductors method allows to screen the current density distribution and it is generally more accurate. However, the computational effort is significantly higher. In this case study, the two methods are compared in the final plots in subsection 3.10.

3.8.2.2 Proposed method for AC losses evaluation

The AC losses estimation process follows the steps listed below.

1. A first simulation is carried out under no load condition and the permeability values are then saved for the next simulations, employing the *Frozen Permeability*.

2. The coercive field H_c of the magnets is set to zero. They are therefore considered as conductors, since their effect on the magnetic field has already been taken into account in the previous step.

3. A simulation at the fundamental frequency $f_{fund.}$ is carried out, applying three circuits, each for one phase of the motor, according to the wiring of the experimental setup. In this case study, especially:

$$\begin{cases} I_a = I_{rms} \cdot \sqrt{2} \\ I_b = -\frac{I_{rms}}{2} \cdot \sqrt{2} \\ I_c = -\frac{I_{rms}}{2} \cdot \sqrt{2} \end{cases} \tag{3.54}$$

   where I_{rms} the fundamental RMS value of the load current injected into the motor phases. It should be noted that $I_a = -2I_b = -2I_c$, because of the considered setup.

4. A further simulation is carried out at the switching frequency f_{sw} of the VSI. Three current ripples are applied to the three phases of the motor. In this case study, especially:

$$\begin{cases} I_a = I_{pk,pk}/2 \\ I_b = -I_{pk,pk}/4 \\ I_c = -I_{pk,pk}/4 \end{cases} \tag{3.55}$$

   where $I_{pk,pk}$ is the peak-to-peak ripple at the PWM frequency, which is approximated as the first harmonic. First harmonic approximation is a very effective approximation, because it allows reducing significantly the number of simulations. A finer method would

suggest to make the Fast Fourier Transform (FFT) of the signal in PLECS and consider higher harmonics, multiples of f_{sw}. In this case-study, applying the FFT, it was verified the negligible contribute of higher harmonics. To further prove it, an FFT of the real waveform is shown in Figure 3.11. $I_{pk,pk}$ is obtained replicating the measurement setup in PLECS and extrapolating the current ripple from the simulation. It was verified that the current ripple derived in the simulation overlapped the one measured by the oscilloscope in the experimental tests.

5. The total power losses depend on four terms that are: $P_{M,fund.}$, $P_{Cu,fund.}$, $P_{M,fsw}$ and $P_{Cu,fsw}$. $P_{Cu,fund}$ and $P_{Cu,fsw}$ are the copper losses and they should be corrected, considering the end windings. Therefore $P_{Cu} = P_{Cu,fund.} + P_{Cu,fsw}$ is multiplied by the factor (3.56).

$$k_R = R_{DC}/R_{DC,femm} \tag{3.56}$$

where R_{DC} is the measured DC resistance of the windings in the setup configuration and $R_{DC,femm}$ is the respective resistance measured by FEMM applying a DC current. If stator coils were wounded on iron teeth, this correction could only be applied when the current density distribution remains uniform over the cross section of the conductors, since in the end windings the current would redistribute. In this case, each coil is wounded in air, therefore the current density distribution is supposed to not vary. The overall losses estimated by FEMM are defined in (3.57).

$$P_{sim} = k_R \cdot P_{Cu} + P_{M,fund.} + P_{M,fsw} \tag{3.57}$$

6. AC contribution to the total losses is finally computed by cutting out the contribution of DC resistance.

$$P_{sim,AC\,only} = P_{sim} - R_{DC} \cdot I_{rms}^2 \tag{3.58}$$

where $P_{sim,AC\,only}$ represents solely the AC contribution to the power losses in windings and magnets and R_{DC} is the measured DC resistance of the stator windings in the configuration described in subsection 3.9.

7. The process from point 2 to point 6 is iterated by a MATLAB script (Octave would represent an alternative open-source solution).

The effect of superposition for non-linear ferromagnetic materials is an approximation, but it was found effective, when permanent magnet losses were compared with the simulated ones, in section 3.10. To give an hint of the time needed: the approximated method requires 2 minutes to estimate the losses for each load condition (steps 2 to 6). The single conductors method instead, requires 50 minutes. Times were estimated by the MATLAB script on a 12th Gen Intel(R) Core(TM) i7-12700K 3.60 GHz with 32 GBs of RAM. In the following section, the

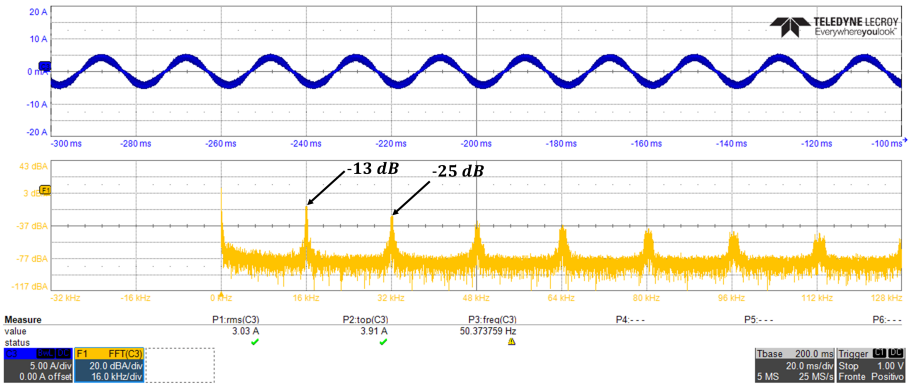


Figure 3.11: FFT spectrum of the experimental phase current waveform I_a (3 A_{rms}). Please note the scale: the first peak at $f_{sw} = 16$ kHz is ~12 dB higher then the next one at $2f_{sw}$.

simulated losses estimated with both methods will be compared with the experimental results.

3.9 Experimental Setup

The motor losses generated by the carrier harmonics of the PWM inverter are mainly two: eddy current losses in the magnets and losses in the winding conductors due to both the skin and proximity effects. As anticipated in the previous sections, MechSTOR is an ironless machine, therefore, no harmonic losses are generated in its core.

Motor losses are measured in a locked motor test as in [29]. The locked rotor condition is achieved by shortening two phases of the MechSTOR stator winding. The two short-circuited

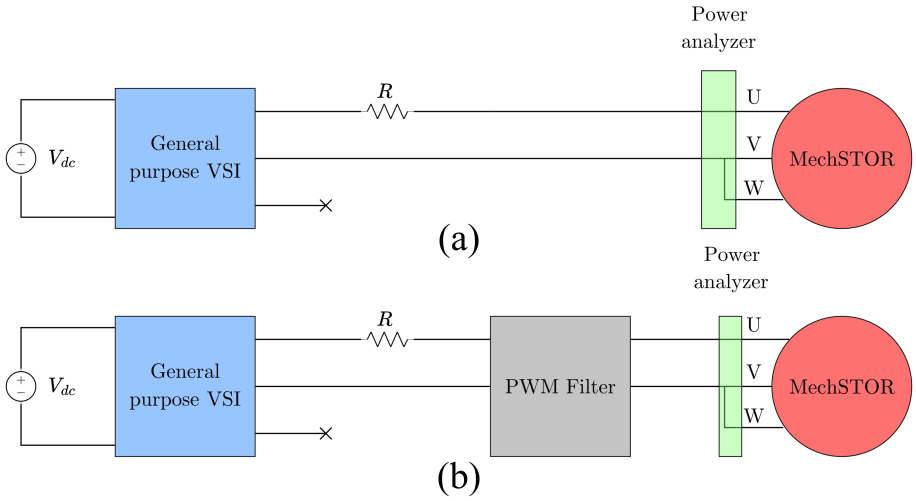


Figure 3.12: Scheme of the experimental setup in case of: (a) direct VSI-fed (no PWM filter), and (b) fundamental harmonic injection in the MechSTOR machine (PWM filter is used).

phases are directly connected to one of the three outputs of a VSI and the third phase is connected to another output of the same VSI. The drive supplies power with a fundamental component $f_{fund.}$. More precisely, tests have been carried out at the following fundamental frequencies: 50, 100, 200, 400 and 600 Hz (50 Hz tests are shown only in the tables). The inverter switching frequency was set at 16 kHz in all set of measurements. Unlike [29], it is not necessary to inject a supply voltage with a fundamental component placed at 4 or 5 Hz, nearly DC, because MechSTOR is an ironless prototype: therefore, iron losses are negligible even at higher frequencies. Maintaining the rotor in a locked condition permits one to directly measure the electric machine losses, and therefore, it is the fastest and most suitable methodology to assess the effectiveness of an AC losses model, that is the aim of this work. Although the direction of fundamental excitation highly impacts the losses of the permanent magnets and the rotor locked condition does not account for it, the aim of this chapter is the model validation and if possible the simplification of the measurements. As explained above, the rotor-locked test to estimate the power losses is a known method.

With the rotor locked, the machine does not generate a back electromotive force (EMF). Consequently, high phase current values are achieved at output voltages lower than those present under rated load conditions. Under these circumstances, the harmonic losses within the machine and the phase current ripple remain relatively low, failing to accurately replicate real-rated load conditions. This happens because the current ripple is highly dependent on the rate of change in current (di/dt) experienced by the motor windings, which in turn is influenced by the voltage applied by the inverter. In this scenario, the accuracy of the model, in comparison

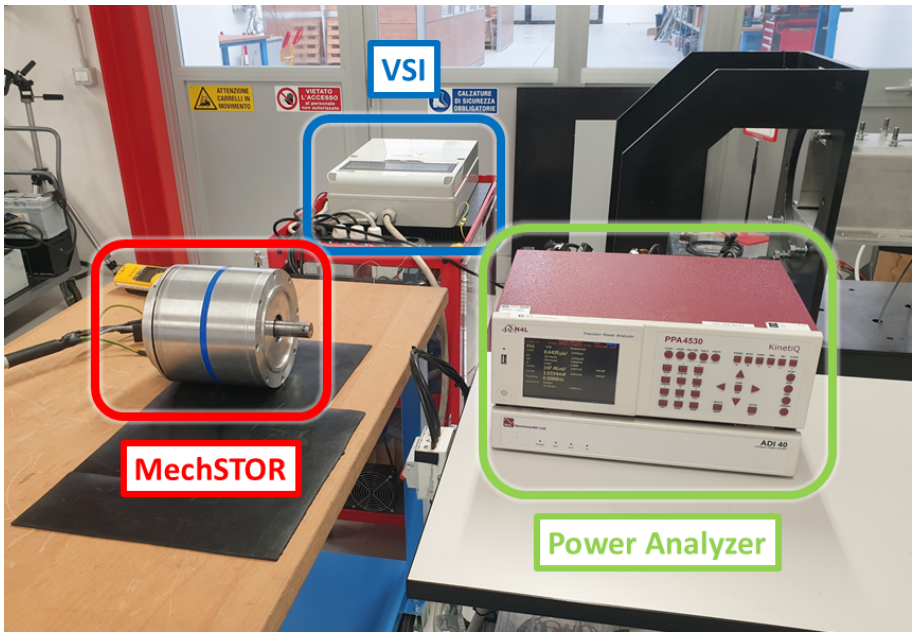


Figure 3.13: Experimental setup with MechSTOR machine, general purpose VSI and power analyzer. PWM filter and power resistor are not visible.

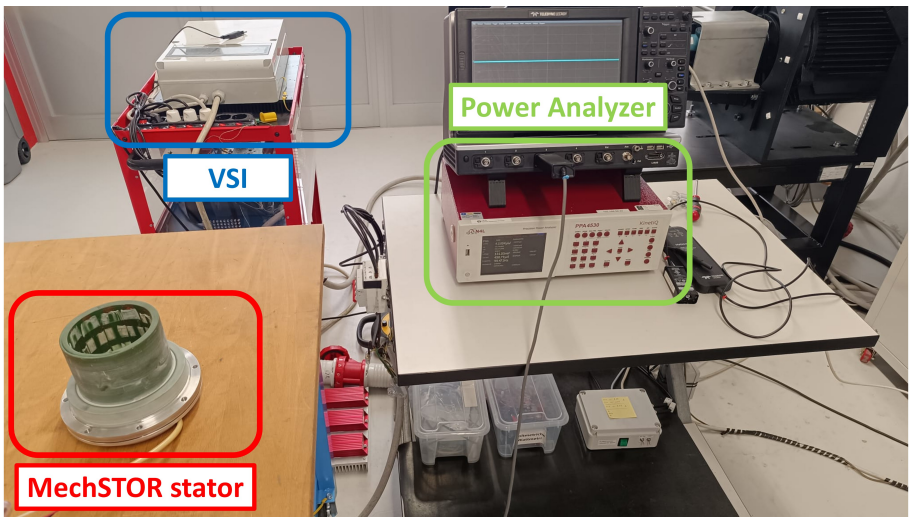


Figure 3.14: Experimental setup with MechSTOR stator only, general purpose VSI and power analyzer. PWM filter and power resistor are not visible.

with the experimental tests, could not be discerned. To compensate for the absence of the back electromotive force (EMF), a 22 Ω resistor is connected to one of the VSI outputs. This operation allows to increase the supply voltage and, consequently, enhances the current ripple. As a result, the motor losses observed in these tests are more representative of those under rated load conditions. AC losses are caused not only by the PWM injections but also by the injection of the first harmonic. The only way to further separate these contributions is achieved through the interposition of a PWM filter between the power resistor and the motor under test.

When the electric machine is directly fed by the VSI, both the drive and MechSTOR are connected through a Newton 4th PPA4530 precision power analyzer to measure motor losses, as illustrated in Figure 3.12 (a). Instead, a PWM LC filter is added before the power analyzer as shown in Figure 3.12 (b). In this way, it is possible to feed MechSTOR with perfectly sinusoidal current, thus injecting the first harmonic only. Furthermore, the absence of iron in the stator allows one to pull the rotor from the prototype and consequently exclude the magnets from the losses evaluation. Pictures of the experimental setup are shown in Figure 3.13 and in Figure 3.14.

A complete set of measurements has been conducted to also split the magnets and the winding losses. MechSTOR has been supplied with a fundamental current ranging from 3 to 8 A_{rms}, corresponding to an overload condition. Motor losses are determined as the mean value of 10 measurements, each acquired with a sampling time of 1 second per each current level. The difference between the VSI supply and the VSI with PWM filter supply, which imitates the CSI behavior, is visible from the oscilloscope, see Figure 3.15 and 3.16, which respectively represents the two cases. In the following paragraph results will be compared for the various operative conditions.

3.10 Results and Comparison

In this subsection, results of measurements are discussed and compared with the simulation outputs. The experimental results are shown in Tables 3.2-3.5. Specifically, Tables 3.2 and 3.3 contain the processed data obtained with a direct VSI feed of the machine prototype, Figure 3.12 a). Respectively, they refer to the experimental tests on the whole machine, Figure 3.13 and only on the stator windings, Figure 3.14. On the other hand, Tables 3.4 and 3.5 disclose the measurements with the interposition of the LC filter, for the entire MechSTOR and for stator windings only, respectively. The last two columns of each table refer to the results obtained in the simulations. Looking at Tables 3.2 and 3.3, one can notice the good compliance between the simulation results and the measurements. The simulation results have already been corrected with the formula in (3.58), to account for the end-windings. A minimal difference can be observed from the results obtained with the *approximate method* and those obtained with the *single conductors method*. For this machine, windings of the same phase are placed in series, i.e. there are no parallel connections. Thus, skin-effect losses prevail over proximity losses. A 2D-FEA *approximate method* allows for fast simulations but would struggle to account for

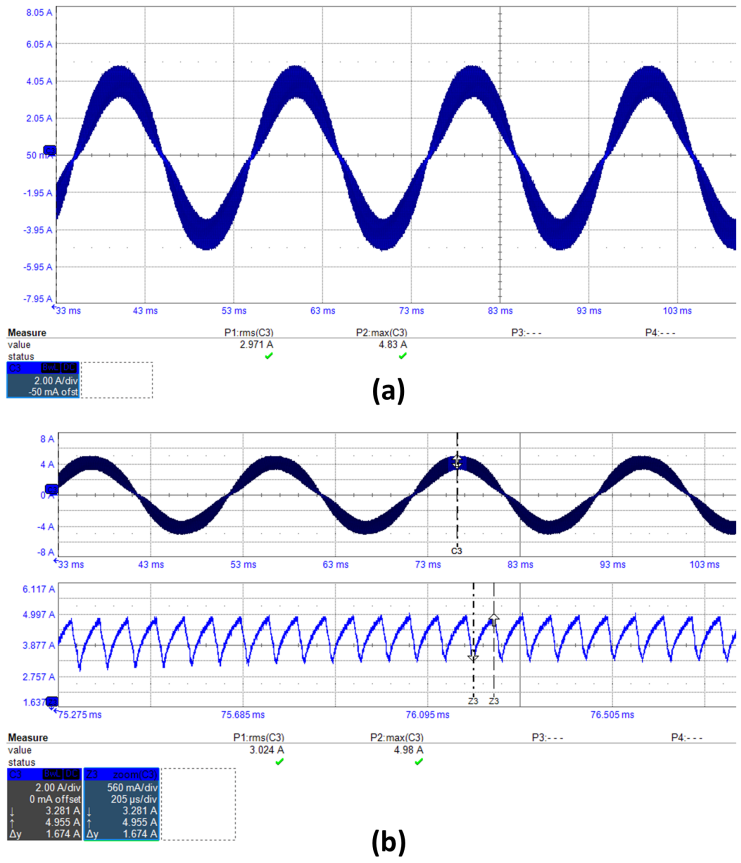


Figure 3.15: Oscilloscope capture of the current phase, 3 A_{rms} for VSI-fed: a) oscilloscope capture and b) current ripple zoom (1.674 A).

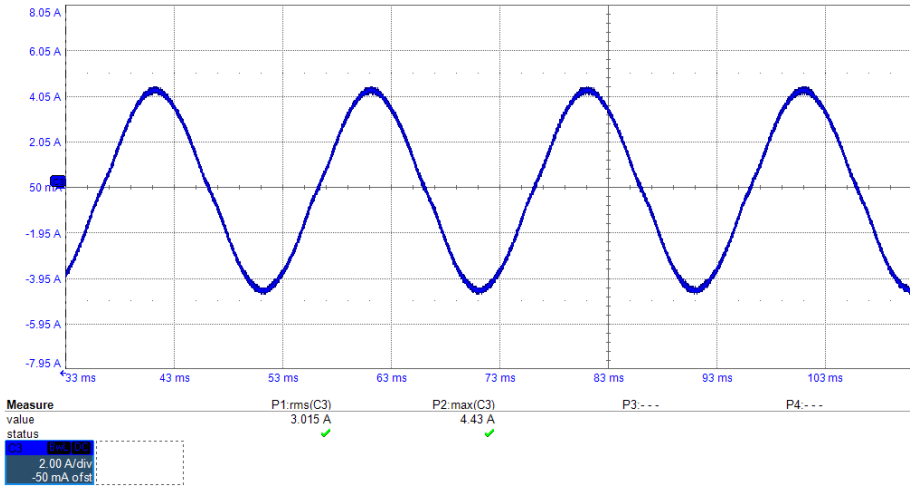


Figure 3.16: Oscilloscope capture of the current phase, 3 A_{rms} for VSI-fed with PWM filter interposed, here the ripple is negligible.

parallel paths. MechSTOR winding connections enhance considerable time savings. A good compliance is found with the experimental tests in both cases. The mean absolute errors,

calculated as in (3.59), for the *approximate method* at the different fundamental frequencies are: 8.01, 6.90, 3.55 and 8.58%. For the *single conductors method*, these errors are: 4.92, 5.59, 2.63 and 11.94 %, resulting in a slightly better AC losses estimation on average, although with minimum differences. Similar discrepancies between the two methods can be observed when magnets are removed, Table 3.3.

$$\overline{e}_{\%} = \sum_{I_{rms} \in \{3 \ldots 8\}} \frac{|P_{exp.,AC\,only} - P_{sim,AC\,only}|}{P_{exp.,AC\,only}} \tag{3.59}$$

These assertions are clarified by Figure 3.17 a) and 3.17 b), where the ratio between the AC power losses and the corresponding DC power losses, $P_{DC} = R_{DC} \cdot I_{rms}^2$ is shown as function of load conditions. The choice of representing the data at 100 and 600 Hz is justified by the operating range of MechSTOR (1500 and 9000 rpm). A growing P_{AC}/P_{DC} or R_{AC}/R_{DC} can be seen in Figure 3.18 a) and 3.18 b) for the extreme load conditions and also here, FEMM results are compliant with the experimental tests. Figure 3.17 and 3.18 are all refer to Table 3.2.

Another interesting evidence appears comparing Table 3.2 and Table 3.3. Since the current ripple is similar for the same load condition, no growing trend can be derived from Table 3.3, which is, instead, present when the whole machine is put under test. The only possible explanation are the growing losses in the magnets the fundamental frequency: in fact, in Table 3.4 the losses change significantly passing from 100 to 600 Hz. A losses breakdown is shown in Figure 3.19 for 3 and 8 A_{rms} and the growing relevance of the magnet losses is clearly visible.

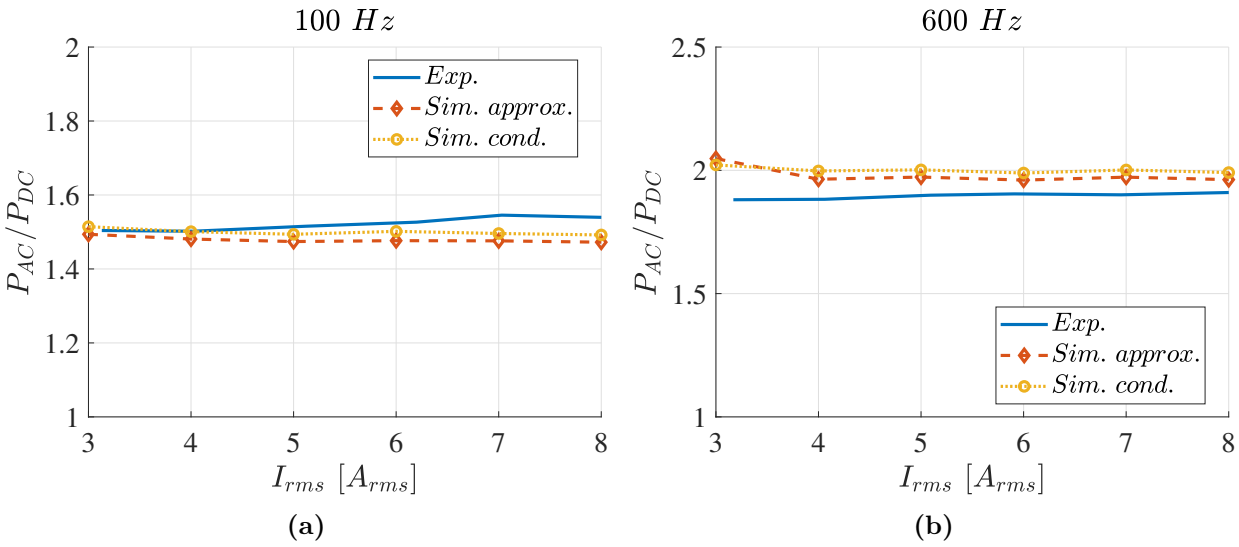


Figure 3.17: Comparison of the motor AC losses at 100 Hz (a) and 600 Hz (b). Experimental tests (solid line), FEMM simulations with the continuum approximation (dashed line with diamonds) and with single drawn conductors (dotted line with circles).

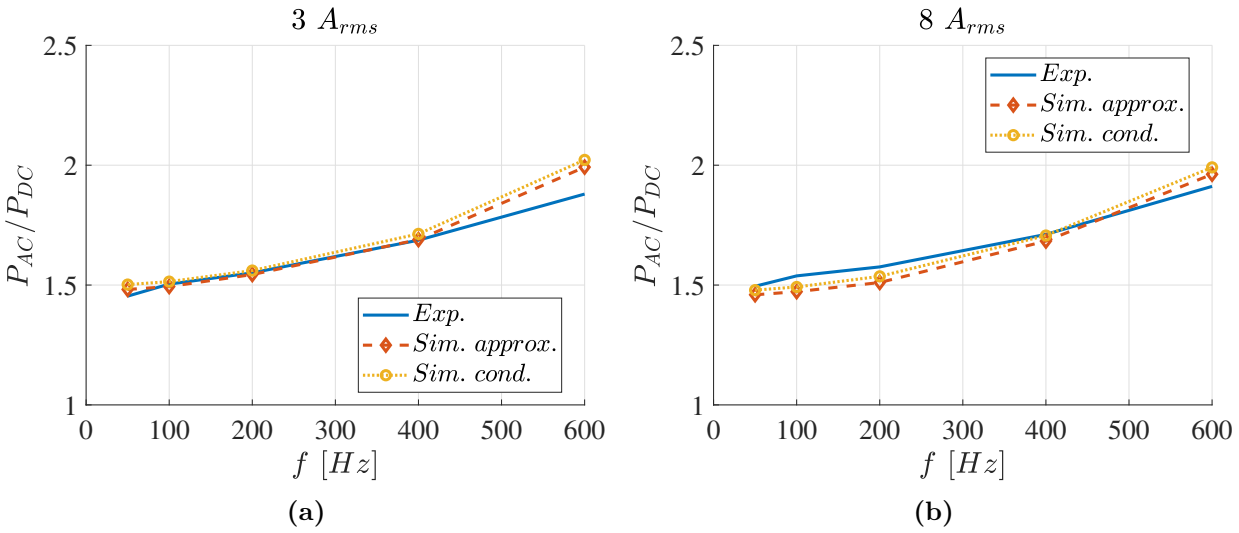


Figure 3.18: Comparison of the motor AC losses at 3 A_{rms} (a) and 8 A_{rms} (b). Experimental tests (solid line), FEMM simulations with the continuum approximation (dashed line with diamonds) and with single drawn conductors (dotted line with circles).

On the other hand, when the filter is interposed, losses are significantly lower; see Table 3.4 and 3.5 with respect to 3.2 and 3.3. Here, the only contribution is the power loss caused by the first harmonic, which significant on the windings only at 100 Hz and on both windings and magnets at 600 Hz. In Figure 3.20, the magnet losses are shown at 100 and 600 Hz compared to the simulation results. Experimental losses at the fundamental frequency and at the PWM frequency are found through the algebraic difference between tests with and without the rotor and with or without the PWM filter. From this picture a good compliance is found

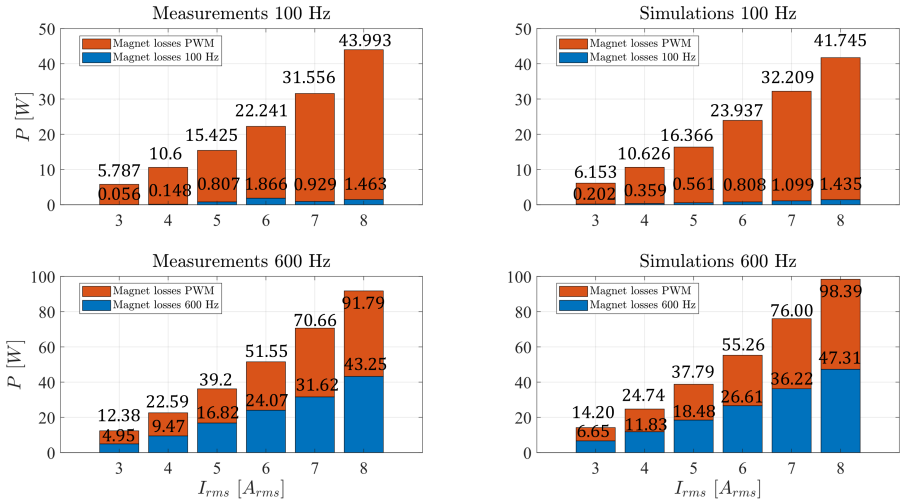


Figure 3.19: Comparison and split of the magnets losses between fundamental and PWM component for different load (I_{rms}) conditions, for $f_{fund.} = 100$ and 600 Hz. On the left side the experimental results and on the right side the simulation results (approximate method).

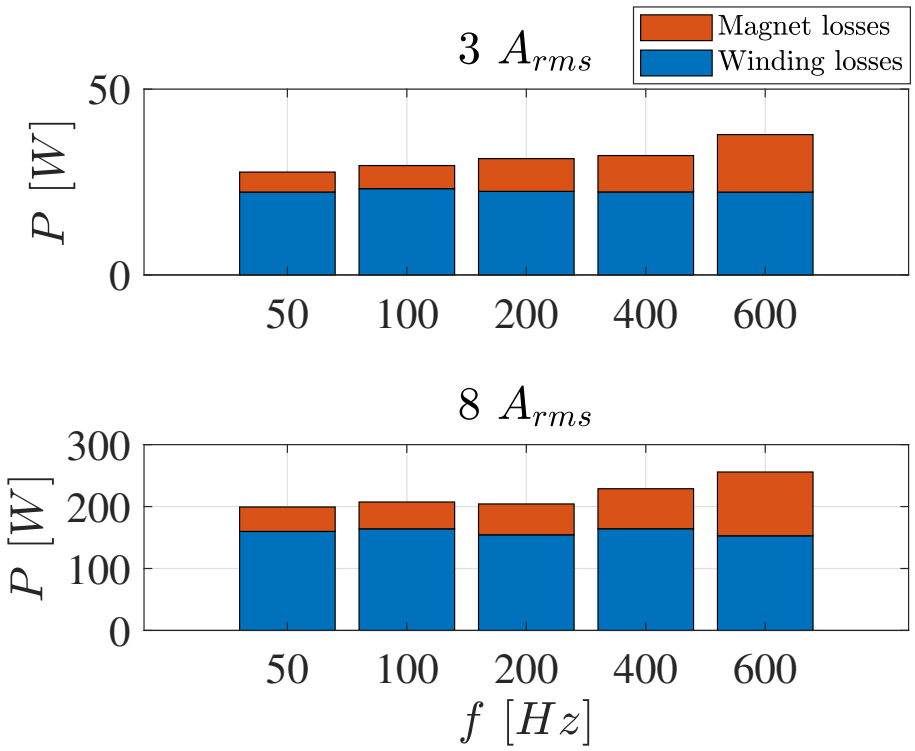


Figure 3.20: Breakdown of magnet and winding losses for different fundamental frequencies.

with the proposed model. The compliance with the results appears to be poor, but losses are little and the discrepancy increases along with the load. The reason behind the deviation is the temperature rise of the windings: FEMM only accept a constant value of the material conductance per each simulation. The difference between the AC losses when magnets are removed, gives an idea of the error committed by the model in the estimation. Even though

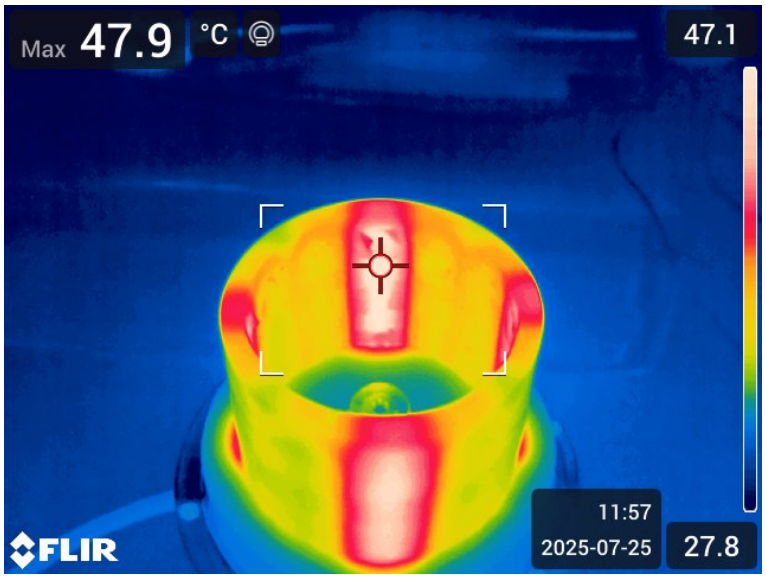


Figure 3.21: Windings temperature after the overload test at 8 A_{rms} without PWM filter.

the tests were rapid (30 to 40 s), at the highest overload, it is sufficient to heat the windings up to 50 °C, see the capture of the infrared camera at the end of the highest load test, Fig, 3.21. Considering a copper resistivity of $\rho = 1.75 \cdot 10^{-6}$ Ωm and a thermal constant of the material equal to $\alpha = 4.1 \cdot 10^{-3}$ K, the discrepancy would be justified. The variation of the the winding temperature is not accounted in FEMM and it explains why the software does not see significant additional losses when the PWM filter is interposed, especially at low fundamental electrical frequency. Neglecting the rise of R_{DC} explains the difference in Table 3.4 and Table 3.5 between the estimated and measured values. The rise of R_{DC} along with the winding temperature will be taken into account in future work. Nevertheless, when the stator alone was tested, it was verified that the windings would cool down to the ambient temperature before performing another test and when the whole machine was tested, several minutes were waited as inserting a thermocouple in the epoxy would have been difficult. Before the tests, the phase-to-phase resistance was measured as 2.664 Ω with a micro-ohmmeter. The inductance values was also verified with an LCR meter.

Table 3.2: Experimental results for a direct VSI on the whole machine.

I_{rms} [A]	**True** I_{rms} [A]	P_{loss} [W]	$R_{DC} \cdot I_{rms}^2$ [W]	$P_{exp.,AC\,only}$ [W]	$P_{sim,AC\,only,approx.}$ [W]	$P_{sim,AC\,only,cond.}$ [W]
Tests at fundamental electrical frequency of 50 Hz						
3	3.087	27.68	19.041	8.641	9.223	9.612
4	4.017	47.791	32.246	15.546	15.238	15.883
5	5.136	77.875	52.701	25.175	24.504	25.54
6	6.068	109.237	73.570	35.667	34.589	36.051
7	7.095	150.608	100.578	50.03	46.688	48.643
8	8.169	199.338	133.319	66.019	61.066	63.652
Tests at fundamental frequency of 100 Hz						
3	3.130	29.438	19.576	9.863	9.723	10.129
4	4.020	48.497	32.247	16.250	15.541	16.189
5	5.120	79.377	52.400	26.977	24.95	26.034
6	6.200	117.240	76.822	40.418	36.74	38.57
7	7.026	152.602	98.617	53.985	47.013	48.974
8	8.214	207.364	134.796	72.568	63.334	65.967
Tests at fundamental frequency of 200 Hz						
3	3.178	31.296	20.177	11.119	11.031	11.308
4	4.009	50.135	32.105	18.030	16.914	17.088
5	5.002	78.089	49.993	28.096	25.964	26.181
6	6.053	114.467	73.214	41.253	38.541	38.357
7	7.102	157.785	100.776	57.009	51.927	53.649
8	8.054	204.226	129.596	74.630	66.174	69.500
Tests at fundamental frequency of 400 Hz						
3	3.087	32.125	19.040	13.085	13.291	13.757
4	4.048	55.362	32.739	22.623	23.188	24.088
5	5.000	84.748	49.918	34.830	33.631	34.780
6	6.019	123.519	72.389	51.131	48.839	50.51
7	6.919	164.291	95.652	68.639	65.214	67.444
8	8.180	228.792	133.705	95.087	91.008	94.089
Tests at fundamental frequency of 600 Hz						
3	3.171	37.762	20.088	17.674	20.056	20.686
4	4.061	62.000	32.951	29.048	31.88	32.978
5	5.093	98.423	51.831	46.593	50.427	51.942
6	5.913	132.901	69.848	63.053	67.236	69.246
7	6.950	183.429	96.509	86.920	93.883	96.702
8	8.184	255.818	133.817	122.001	128.549	132.395

Table 3.3: Experimental results for a direct VSI on the stator windings.

I_{rms} [A]	**True** I_{rms} [A]	P_{loss} [W]	$R_{DC} \cdot I_{rms}^2$ [W]	$P_{exp.,AC\,only}$ [W]	$P_{sim,AC\,only,approx.}$ [W]	$P_{sim,AC\,only,cond.}$ [W]
Tests at fundamental electrical frequency of 50 Hz						
3	3.088	22.308	19.052	3.257	2.897	3.22
4	4.029	38.138	32.438	5.700	4.786	5.315
5	5.133	62.166	52.644	9.522	7.697	8.548
6	6.07	88.438	73.614	14.824	10.864	12.0651
7	7.079	120.749	100.136	20.613	14.664	16.279
8	8.151	159.842	132.758	27.084	19.09	21.205
Tests at fundamental frequency of 100 Hz						
3	3.138	23.218	19.673	3.545	3.005	3.337
4	4.056	38.847	32.875	5.972	4.800	5.331
5	5.130	63.583	52.575	11.008	7.675	8.571
6	6.184	92.118	76.405	15.712	11.146	12.702
7	7.025	120.704	98.605	22.137	14.518	16.124
8	8.195	164.088	134.191	29.897	19.491	21.641
Tests at fundamental frequency of 200 Hz						
3	3.117	22.482	19.407	3.075	3.086	3.381
4	4.217	41.169	35.523	5.646	5.460	5.874
5	5.086	60.459	51.674	8.784	7.832	8.396
6	6.102	87.745	74.404	13.340	11.381	12.0858
7	7.047	117.501	99.214	18.287	14.815	16.318
8	8.031	154.427	128.864	25.563	19.082	21.424
Tests at fundamental frequency of 400 Hz						
3	3.106	22.339	19.279	3.060	3.241	3.610
4	4.088	38.991	33.384	5.607	5.650	6.376
5	5.145	62.212	52.892	9.321	8.543	9.487
6	6.130	88.694	75.077	13.617	12.147	13.489
7	7.114	120.014	101.128	18.887	16.549	18.371
8	8.316	164.183	138.163	26.020	22.592	25.070
Tests at fundamental frequency of 600 Hz						
3	3.092	22.291	19.106	3.186	3.860	4.298
4	4.202	41.203	35.285	5.918	6.828	7.708
5	5.140	62.047	52.777	9.270	10.355	11.494
6	6.032	86.464	72.695	13.769	13.993	15.531
7	7.063	117.615	99.661	17.954	19.525	21.670
8	7.988	152.816	127.485	25.331	24.643	27.352

Table 3.4: Experimental results with PWM filter interposition for the whole machine.

I_{rms} [A]	**True** I_{rms} [A]	P_{loss} [W]	$R_{DC} \cdot I_{rms}^2$ [W]	$P_{exp.,AC\,only}$ [W]	$P_{sim,AC\,only,approx.}$ [W]	$P_{sim,AC\,only,cond.}$ [W]
Tests at fundamental frequency of 100 Hz						
3	3.055	20.327	18.648	1.679	0.206	0.209
4	4.05	36.099	32.764	3.335	0.367	0.371
5	5.053	56.608	51.016	5.592	0.574	0.580
6	6.067	82.473	73.536	8.937	0.825	0.835
7	7.039	110.825	98.993	11.832	1.121	1.137
8	8.069	146.412	130.090	16.322	1.466	1.485
Tests at fundamental frequency of 600 Hz						
3	3.065	25.795	18.775	7.020	6.802	6.874
4	4.042	44.92	32.639	12.281	11.944	12.220
5	5.122	74.706	52.421	22.284	18.892	19.094
6	6.168	108.401	76.007	32.394	27.206	27.494
7	7.161	147.432	102.455	44.977	37.03	37.423
8	7.962	182.241	126.657	55.584	48.365	48.880

Table 3.5: Experimental results with PWM filter interposition on the stator windings.

I_{rms} [A]	**True** I_{rms} [A]	P_{loss} [W]	$R_{DC} \cdot I_{rms}^2$ [W]	$P_{exp.,AC\,only}$ [W]	$P_{sim,AC\,only,approx.}$ [W]	$P_{sim,AC\,only,cond.}$ [W]
Tests at fundamental frequency of 100 Hz						
3	3.053	20.450	18.617	1.833	0.004	0.005
4	4.045	35.846	32.697	3.1483	0.005	0.008
5	5.05	55.741	50.965	4.777	0.009	0.013
6	6.050	80.116	73.135	6.981	0.013	0.019
7	7.041	110.007	99.057	10.950	0.018	0.024
8	8.022	143.311	128.566	16.745	0.023	0.031
Tests at fundamental frequency of 600 Hz						
3	2.956	18.909	17.453	1.455	0.105	0.120
4	3.971	34.186	31.506	2.680	0.187	0.214
5	5.051	55.528	50.956	4.570	0.292	0.334
6	6.009	79.163	72.146	7.018	0.421	0.482
7	7.059	111.285	99.567	11.716	0.574	0.655
8	7.993	140.427	127.634	12.793	0.750	0.855

3.11 Discussion on the advantages of employing a CSI topology

The first study investigated the performance of CSI-fed and VSI-fed drives from the standpoint of the total inverter losses, phase currents THD and torque ripple. The complete motor drive, with control system, VSI/CSI and MechSTOR machine were modeled in PLECS in the same

conditions, i.e. by keeping the same switching frequency and simulation parameters. The thermal model of devices, obtained from their datasheets, was inserted into PLECS model of both converter in order to compute their losses. Simulations were conducted for various switching frequency values: the phase current total harmonic distortion (THD); and torque ripple were evaluated for each condition.

The estimated values for current THD, percent peak-to-peak torque ripple and inverter efficiency are summarized in Figure 3.6 and Figure 3.7 for increasing values of the switching frequency for both VSI and CSI. The CSI exhibits significantly improved current waveforms and reduced torque ripple, even at lower switching frequencies, while also demonstrating a slight improvement in efficiency. Specifically, the substantial difference in total harmonic distortion (THD) motivated further investigation into the impact of different feeding strategies on the ironless machine. The comparison between Table 3.2 and 3.4 perfectly explains the advantage of a CSI, i.e. sinusoidal fed on the electrical machine. A sinusoidal current waveform, without any higher harmonic contribution, enhances a significant loss reduction, especially in overload condition, for an ironless machine with low phase inductances, as the MechSTOR is. Of course to compare the two drives a further extended analysis is needed to evaluate the overall efficiency in both cases, but this work shows the CSI potential on the motor side, in this sense it represents an extension of the work presented before and published at ECCE Conference [30].

3.12 Conclusions and Future Development

This chapter concludes the study on the MechSTOR ironless prototype. First, it presented a comparison between a CSI and a VSI feed and then it showed a AC loss model for an ironless machine. Ironless motors are characterized by inherently low inductance values, which result in substantial current ripple when powered by a VSI. Therefore, AC losses become relevant at the switching frequencies, as has been shown in the results. Here, a fast and approximate 2D-FEA method was proposed and compared with the experimental tests, which were carried out at different fundamental frequencies and under different load conditions. A minimum mean absolute error of 3.55 % was achieved with the proposed method. Minimal differences have been found with a more accurate 2D-FEA model, thus not justifying its computational effort for an ironless machine. The comparison was strengthened by a complete and detailed test on the motor. In order to split the contribution on the AC losses and prove the goodness of the model, several tests were conducted, interposing a PWM filter and removing the magnets. The

main limitation on the model, which consists in the accountability of the winding resistance temperature increment, was stated and discussed as well. In this context, the advantages of CSI technology become more pronounced, leading to a significant reduction in torque ripple and AC losses. As expected, AC losses in the VSI configuration, without the PWM filter, were found to be significant. However, losses decreased drastically when a PWM filter was interposed, emulating the CSI-fed. These findings demonstrate that CSI technology is not only a promising alternative, but also a proven effective solution for driving ironless motors, enabling a substantial reduction in AC losses and a marked decrease in torque ripple. It should be pointed out that the full comparison should be done driving the machine with both inverters and computing the overall efficiency. The main limitation of the simulations of this chapter do not concern the output capacitors of the CSI, which are film capacitors, instead the omission of the calculation of the losses on the inductance. Therefore, the result of the simulations in terms of efficiency should be taken with caution. In a future work, the final comparison will be made between the two drives.

3.13 References

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4. Extended Flux-Weakening Control Technique with a Current Source Inverter

4.1 Introduction

In chapter 3 a study on the potential advantage of a CSI feed was carried out for an ironless machine motor, with a final focus on the potential advantages on motor losses. However, CSI architecture becomes interesting also when driving more common and known permanent magnet machines. Especially if WBG transistors are employed, the main drawback of CSI-drive, i.e. the efficiency, can be compensated for by them. This makes the architecture potentially interesting, also for a traction application.

Especially high performance interior permanent magnet (IPM) machines are widely used for electric vehicles. Some of their main advantages are the robust rotor structure, field weakening capability, and high power density and efficiency. Generally, the most common motor drive for these electric powertrain is the well-known Voltage Source Inverter (VSI).

Current Source Inverter (CSI) is becoming interesting in high power applications because of several advantages. With a VSI, in the event of fault under Flux Weakening (FW) condition, uncontrolled generator operation could occur since the motor back EMFs could exceed the dc supply voltage, damaging the drive and the battery. The CSI, instead, is absolutely more resilient against this condition: in fact, when VSI is used, if a fault occurred in FW conditions, the diodes connected anti-parallel to the transistors would work as a not controlled rectifier bridge and they could cause intolerable over-voltages. Furthermore, they may not be able to sustain such high currents, causing the failure of the components. With a CSI instead, if the diodes in series with the transistors are sized correctly, they can tolerate the voltages imposed by the load. Moreover, as pointed out in [1], VSI shows a high dv/dt coming from the pulse width modulated (PWM) output voltages, which causes degradation of motor insulation, especially because of partial discharges (PD) [2]. Moreover, PWM causes additional losses in the motor, acoustic noise, and higher electromagnetic interference. CSI, instead, allows driving the motor with a reduced harmonic content in the voltages and the currents, reducing the dv/dt stress on

the insulation systems, the losses and the torque ripple.

The intrinsic boost capability of the CSI is certainly another advantage. The authors in [3], studied the comparison between VSI and CSI when interfaced with the grid in a distributed and renewable energy system. Thanks to its step-up capability, the CSI was proven to be a very interesting topology for wide input voltage applications. Although the VSI needs an additional boost converter, using a CSI grants a single-stage power conversion system. For a motor drive, the intrinsic boost capability can be employed to delay the flux-weakening, as has been done here.

The main drawback of a CSI is represented by the higher power losses in comparison to traditional VSI. The authors in [4] and [5] proposed a new CSI topology for a photovoltaic application that employs an additional leg with another switch, which should be operated during overlap periods, reducing conduction losses. Instead, efforts are made in [6], [7] and [8] to avoid the need for a pre-stage. Few examples of CSI-fed electric drives exist in the literature, mainly with regard to field-oriented control, such as [9], without considering a FW strategy.

In [10], a comparison loss modeling study is presented between a VSI with a boost/buck converter and a CSI for the traction drive of electric vehicles. The study showed that the CSI had lower losses for the majority of vehicle operating points during the aggressive driving schedule. The voltage boost feature could be used up until the desired speed value is reached, but this would lead to high voltage values, not suitable for the insulation system and the voltage rating of the power devices. Furthermore, the inverter would be highly oversized in terms of voltage per ampere. Hence, FW operation must also be implemented for a CSI-fed drive but with an increased base speed with respect to a VSI-fed drive.

In [11] the authors present the development of a CSI based motor drive using wide-bandgap power switches. The experimental results showed that the prototype can achieve an efficiency greater than 97.6 % at a switching frequency of 125 kHz.

Here, a new control strategy combining CSI boost capability and FW control strategy is presented. FW is started once the voltage at the motor terminals is reached in order to reach higher speed values with a reasonable voltage. Furthermore, thanks to this the MTPV can be avoided, simplifying the overall control loop and, at the same time, reaching higher speed at higher power. In traction applications, a powertrain that exhibits an extended constant power speed range is one of the most important performance parameter.

When a VSI is employed, in order to obtain a wide speed range a flux weakening control strategy

must be implemented to take under control the voltages at the motor terminal above the base speed. The maximum voltage that the VSI can impose is limited by the DC BUS voltage.

On the other hand, The CSI has an intrinsic boost capability that can be exploited to impose a voltage at the inverter terminal above the battery voltage of the power train. Ideally, the CSI could be increased until the motor reaches the desired maximum speed, but the voltage at the motor terminals could be very high. Constraints are transferred to the motor side.

In subsection 4.2 the main parameters of the IPM motor considered for the motor drive are reported. In subsection 4.3 the conventional VSI model is presented in MTPA, FW, and MTPV conditions, and its results are analyzed. Then, subsection 4.4 describes the new extended MTPA-FW model applied to a CSI and in subsection 4.5 the two architectures are compared in terms of efficiency. In the end (Section 4.6) conclusions and future developments are presented.

4.2 Motor Parameters and Reference Trajectories

The machine taken into account is an IPM synchronous machine. IPM machines are widely used in this field since they allow to obtain high performance by combining the different torque source of synchronous reluctance machines and traditional permanent magnets machines. In Table 4.1 the main parameters of the motor considered for the simulations are reported and Figure 4.1 shows the geometry of the motor considered.

Table 4.1: Motor Data.

Motor Parameter	**Symbol**	**Value**	**Unit**
Slot number	Q	24	-
Pole pairs number	p	2	-
Nominal current	I	425	A_{rms}
Nominal torque	T	44	Nm
Mechanical power	P_{mec}	14	kW
Maximum speed	ω_{max}	23000	rpm
Stator phase resistance	R_s	3.2	mΩ
Stator d-axis inductance	L_d	3.1	mH
Stator q-axis inductance	L_q	8	mH

The overall performance of the motor are given by the interaction of the motor, the drive, and the power source, therefore the torque-speed characteristic is determined only when all the

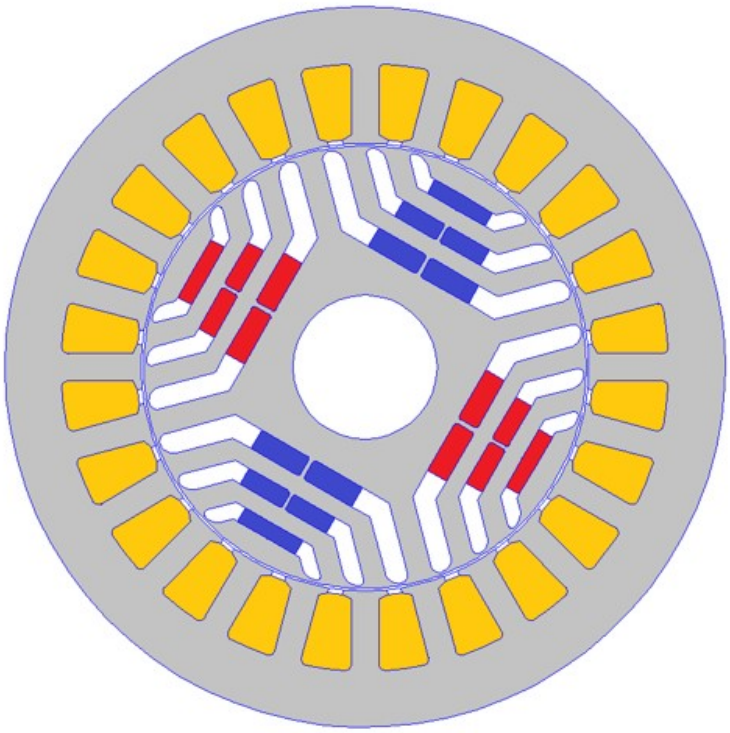

Figure 4.1: Reference motor considered for the application.

system parameter are defined and a control strategy is chosen.

To obtain an extended speed range a proper control strategy must be implemented to reduce the main machine flux, usually an external control loop is added to the vector control to move toward the negative id axis the current vector when the required voltage exceed the voltage limit. When the characteristic current is inside the current limit circle an additional control loop must added to reduce the current vector amplitude in order to move from the FW control strategy to MTPV control strategy.

In the following the motor model is simplified and the inductance values on d and q axis are considered constant (as reported in Table 4.1) for a simpler comparison between VSI and CSI performance, a more detailed approach considering variable inductances can be found in [12].

The electric power train model was created in PLECS, where all the simulations were made.

Neglecting magnetic saturation of the machine, the optimal control trajectories obtained are shown in Figure 4.2. As expexcted MTPA, FW and MTPV are needed to reach the maximum speed value desired, so the control implementation can become quite complicated with a traditional VSI as the maximum speed value is limited by the DC BUS Voltage.

Another important advantage of the CSI topology is that it allows to control directly the

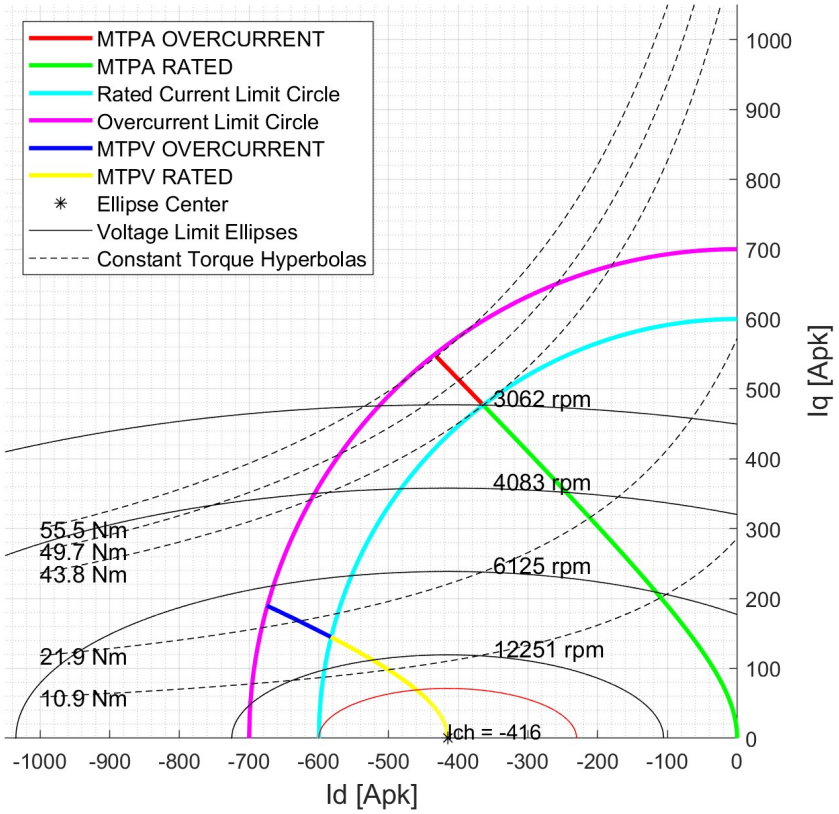

Figure 4.2: Optimal control trajectories.

current given as an input to the stator of the motor. Thanks to this, their shape is almost a pure sinusoidal waveform with almost null ripple, leading to a minimization of the traditional PWM losses in magnets and iron that are normally generated from VSI current ripple.

4.3 VSI Model

A traditional VSI architecture was chosen, with 6 switches With a DC BUS as input ideal voltage source, see Figure 4.3. The voltage source inverter was employed to drive the electric motor, whose parameters are the one presented in subsection 4.2, all the components and the control blocks were modeled in PLECS.

In Figure 4.4 the block diagram of the control mode for the MTPA is reported. The current vector angle for MTPA is given as a function of the current amplitude.

With the purpose of reaching the desired speed of 23000 rpm, a flux weakening strategy must be implemented, in this case an outer voltage loop is employed to modify the current vector angle. The voltage required by the current loop is compared to the DC BUS voltage, when the

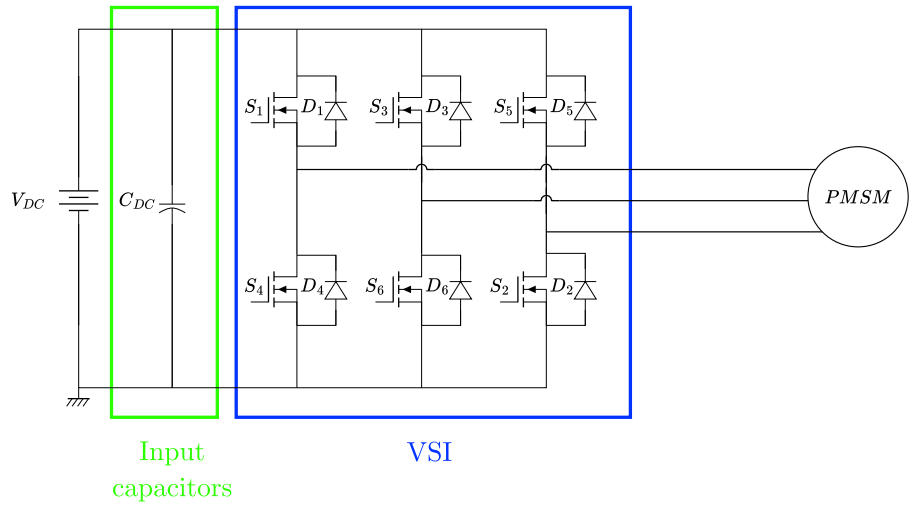

Figure 4.3: VSI schematic.

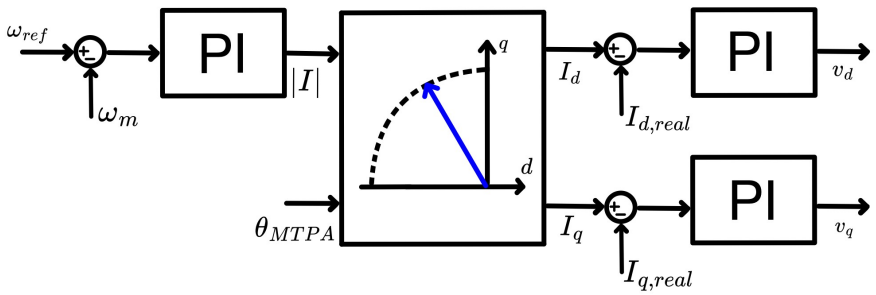

Figure 4.4: Block diagram of the VSI control mode in MTPA conditions.

required phase voltage exceeds the available DC BUS limit the flux weakening loop will add an additional angle to the current vector to increase the negative id current and decrease the iq current as shown in Figure 4.5.

In this case, a MTPV control strategy must be implemented to reach the speed setpoint. Initially, the maximum speed reachable with FW is computed according to (4.1).

$$\omega_{FW,end} = \frac{V_{lim}}{p_p(L_d I_{lim} + \lambda_{pm})} \tag{4.1}$$

When the mechanical speed of the motor reaches ω_{FW_end}, the MTPV control strategy starts to act; the saturation blocks which limits the current module obtained at the output of the speed

loop and the d axis current obtained from the outer voltage loop. So the current amplitude is reduced dynamically, according to the desired MTPV trajectory found which maximize the motor performance.

When the current values on d and q axis are found, they must be converted into voltage values, needed to find the correct PWM modulation for the VSI. Several types of already known modulation exist: the one chosen was a Symmetrical Space Vector Modulation (Symmetrical SVM), since it allows chasing sinusoidal voltages with a peak value up to $\sqrt{3}/2 \cdot V_{dc}$.

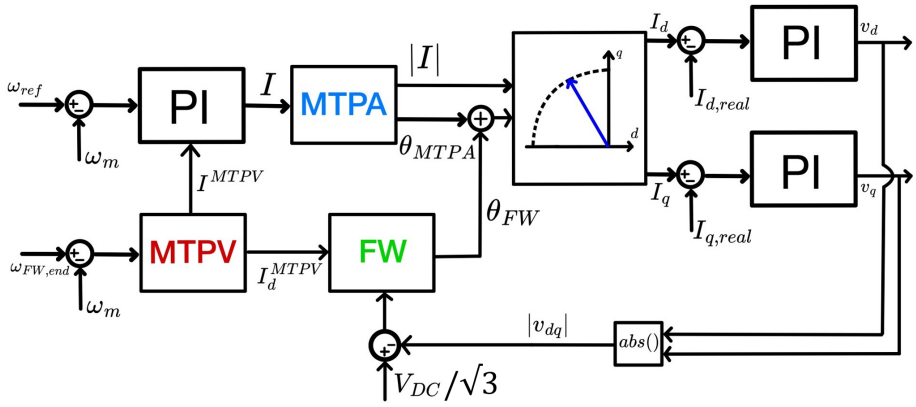

Figure 4.5: Block diagram of the VSI control mode in MTPA, FW and MTPV conditions.

In PLECS a constant set point of 23000 rpm was applied. In order to get to the desired speed set point, MTPA, FW and MTPV must be used in the control loop. Differently from what it is shown in the following section it is not possible to delay the flux weakening for a VSI without increasing the input DC voltage.

4.4 CSI Model

4.4.1 CSI Architecture

The traditional CSI architecture includes an half-bridge pre-stage to generate the input DC current and six switches, SiC MOSFETs in this case, Figure 4.6.

The need of a pre-stage was already explained in the low-speed range, since the back-EMF peak values of the motor are lower than then the DC input voltage. Several efforts have been made in literature to eliminate the pre-stage: authors of [6] and [7] proposed its elimination in the high speed range and its maintenance in the low speed range. More recently, authors of [8] proposed to substitute the pre-stage with a coupled inductor and a diode. However, these works

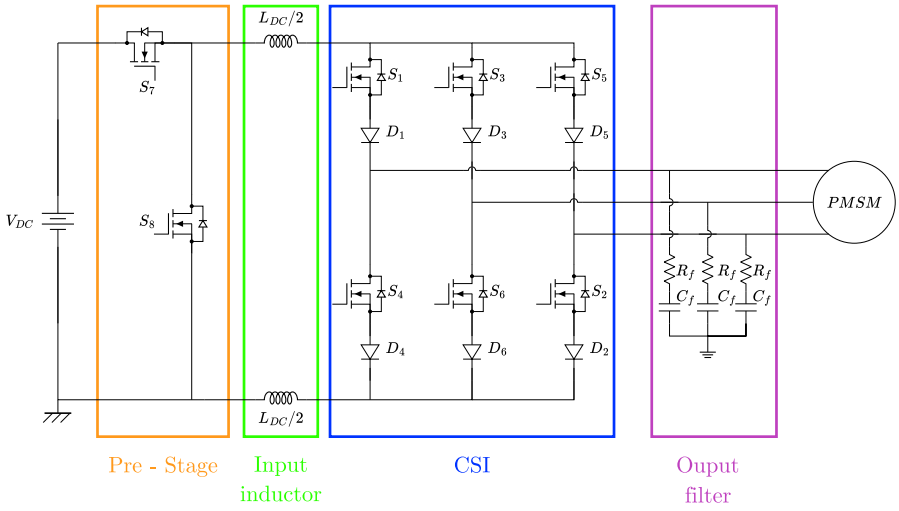

Figure 4.6: CSI schematic.

did not consider a FW strategy, which is necessary if the motor back EMFs cannot surpass the input DC voltage and the boost capability of the CSI can be exploited only for a limited speed range. That explains the need of a pre-stage in this work. Particularly a bidirectional boost was chosen since it allows to reduce the number of devices and switching losses for obvious reasons. Of course, the input inductance L_{DC} and the output filter C_f, should be designed. For the DC-link inductance a margin has been taken with respect to the formula in (4.2), well-known in literature, that defines the minimum value.

$$L_{DC} = \frac{\sqrt{3} T_{sw} V_m}{4 \Delta I_{DC,max}} \tag{4.2}$$

Where T_{sw} is the switching frequency period, chosen equal to $1/60kHz$, V_m is the peak value of the voltage awaited on the motor side and $\Delta I_{DC,max} = 5\%\, I_{DC}$. The resulting inductance $L_{DC} = 0.1\ mH$. About the output C_f filter instead, the problem of the LCL resonance was deeply studied in [13]. $C_f = 300\ \mu F$ was found to be a value that kept the electrical torque ripple moderate at low mechanical speeds, the switching frequency influences the filter design too. Torque "glitches" are reduced thanks to an alternate modulation too.

4.4.2 Proposed Control scheme and Flux-Weakening Technique

Similarly to the procedure followed for the control design of the VSI, the CSI control strategy was defined. In Figure 4.7 the simple MTPA control strategy is reported. In this case, the

current value obtained in output are called m_d and m_q, since they are directly used for the modulation strategy of the CSI, that, differently from VSI, is driven in current. In Figure 4.8

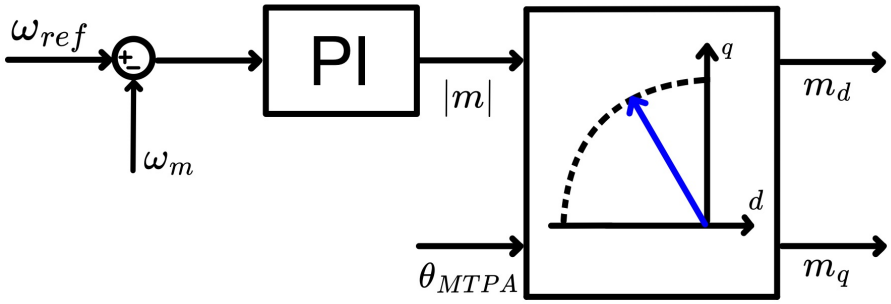

Figure 4.7: Block diagram of the CSI control mode in MTPA conditions.

the MTPA and FW more traditional control strategy is reported. This implementation for the CSI simplifies the total number of control loops since there is not the passage from d-q currents to d-q voltages, compared to a more traditional MTPA and FW control applied to a VSI. It should be stated that all the articles reported in the bibliography did not treat the FW problem for a CSI, however for very high speed range it becomes necessary. In [14], the authors explained different ways to delay the flux weakening and decided to implement the reduction of the modulation index, i.e. the ratio between the module of the reference current and the DC current. Decreasing the ratio, reduces the efficiency but allows reaching higher speeds without implementing a FW algorithm, because a higher current from the DC source and therefore the output voltages of the CSI increase: here another method is employed and the FW implementation proposed is shown in Figure 4.9 is quite different. In order to exploit the CSI boost capability, an additional control loop is added to modify the overlap time when the voltage limit is near. In this way the motor can receive more voltage and the base speed increase with respect to the VSI application. In Figure 4.9 two gains of 10^9 are found. These are used just to translate $t_{ov,start}$ from s to ns. Instead, the specific gain of 0.85 was calibrated to have a suitable additional voltage that adds up to the reference voltage v_{ref}. Initially, the gain should be left to 1 and then progressively reduced to reach the maximum speed, 23000 rpm in this case and at the same time avoid exceeding or coming close to the rated voltage of the power devices.

When the maximum overlap time is considered, the maximum voltage is reached, and the flux weakening can begin, reaching higher torque at the maximum final speed. In Figure 4.10, the advantage of employing an overlap time variation is clear: the green curve was obtained keeping the overlap constant at 10 ns, instead the red curve was obtained, varying it from 10

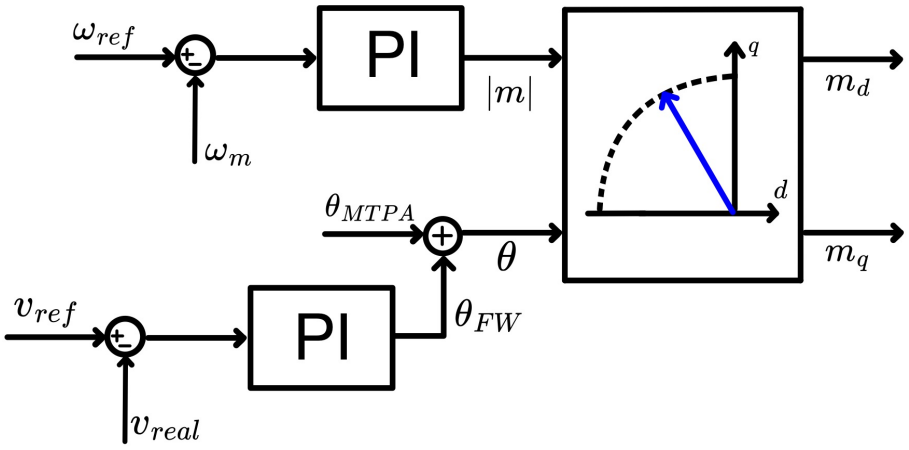

Figure 4.8: Block diagram of the CSI control mode in MTPA and FW conditions.

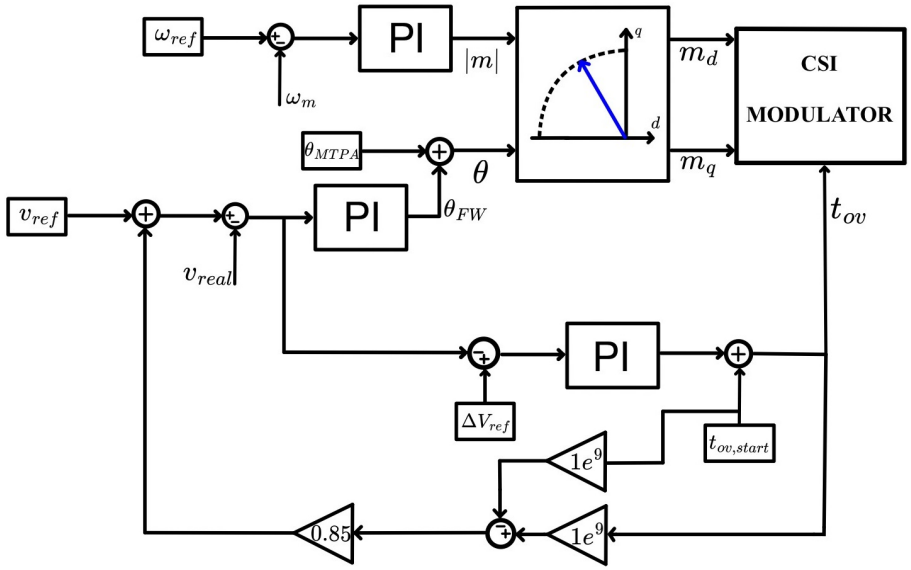

Figure 4.9: Block diagram of the CSI control mode in MTPA and FW conditions with voltage boost.

ns to 100 ns. In addition to for the VSI, simulations were performed at $f_{sw,CSI} = 60$ kHz and $f_{sw,pre} = 60$ kHz. The efficiency results are reported and compared with the VSI in subsection 4.5. In Figure 4.10, at 17500 rpm, the blue line increases. Here control is lost and simulation does not make sense anymore: with an overlap of 10 ns it is not possible to reach the desired maximum speed of 23000 rpm.

In the previous figures, the MTPA angle is a constant: this is generally a bad approximation. θ_{MTPA} depends on the inductances L_d and L_q, which are non-linear and can change significantly, especially with saturation. Moreover, depending on the load, i.e., the magnitude of $|\vec{I}| = \sqrt{i_d^2 + i_q^2}$, the same angle changes, recall the green curve in Figure 4.2. However, because the MTPA mapping of the motor was not the aim of this work, a single operating point, or load,

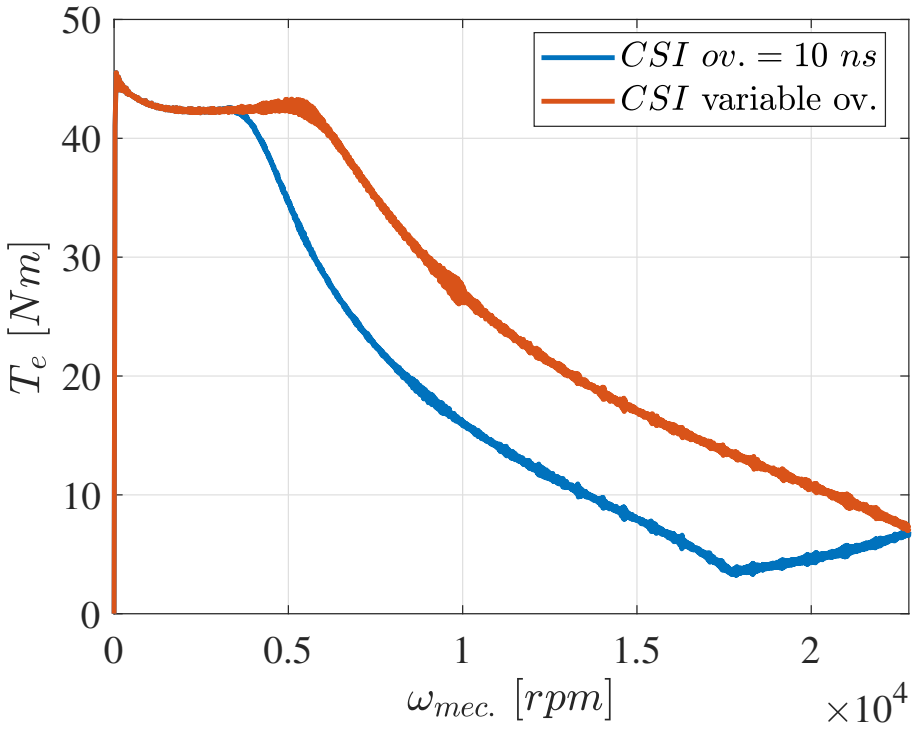

Figure 4.10: Motor electrical torque with constant overlap of 10 ns and controlled overlap (up to 100 ns).

was considered for each simulations. In the following paragraph, simulations are reported at nominal load. Instead, with respect to saturation of L_d and L_q, the issue was not considered here and it is part of a future work to integrate this simulation model with the lumped parameters model of the IPM machine created in [15], to which the author participated.

The proposed control scheme is based on a traditional Field Oriented Control (FOC) with a FW technique, based on the back EMFs of the electric motor. Since a FOC control was chosen for the CSI, it was considered fair to apply the same type of control to the traditional VSI. However, traditional inverters can implement a Direct Flux FOC, which differs from the most common technique, as it is implemented on the (f, τ) reference frame: the stator flux λ lies on the axis f. This type of control, which is not investigated here, allows one to directly manipulate the flux: first the flux is observed [16], then MTPA and MTPV curves derived from analytical formulae and motor parameters are followed [17]. With respect to the current FOC, direct flux control is less sensitive to variation in motor parameters and iron core losses, which are significant for IPM at high speed. Current-controlled drives, like the one presented here, require a deeper knowledge of the electrical machine and its behavior at different loads (losses, etc...) for a correct implementation of FW. However, in this specific case, one advantage of the boost capability of the CSI is to avoid the MTPV, the maximum speed can be reached without

the need of following this curve.

4.4.3 Modulation Technique

Regarding the modulation technique, the most effective was chosen, based on the potential resonance damping, which is a common problem for CSI converters at certain speeds [18]. Before delving into the applied modulation technique, it is worth mentioning that the SVPWM (Space-Vector Pulse Width Modulation) works exactly like the respective SVPWM of a VSI. The difference only consists of the controlled vector: for a VSI the voltage is modulated, and for a CSI instead, the current is modulated. Considering, for example, that the resulting vector is in the first sextant, Figure 4.11 represents graphically the SVPWM for a CSI. The reference vector $\vec{I}_{ref}$ is obtained by applying two active vectors and one zero vector. Each applicable vector consists of a modulation sequence.

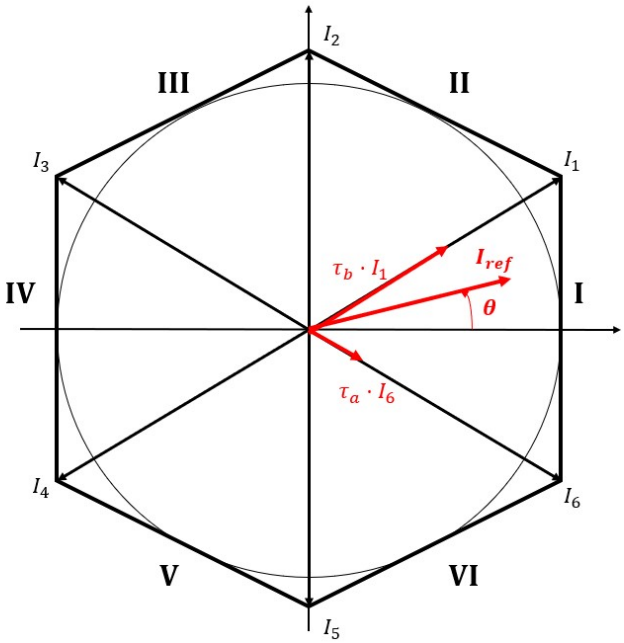

Figure 4.11: Space Vector Modulation for a CSI.

τ_a and τ_b are the times for which the vectors $\vec{I}_a$ and $\vec{I}_b$ are applied. Given a certain $I_{ref} = |\vec{I}_{ref}|$, the main formulae for which the portions and the times for which the vectors are applied are

defined in (4.3) and (4.4).

$$\begin{cases} I_{ref} = \sqrt{I_\alpha^2 + I_\beta^2} \\ \tau_a = \frac{2}{\sqrt{3}} \cdot \frac{I_{ref}}{I_{DC}} \cdot \sin\left(\frac{\pi}{3} - \theta\right) \\ \tau_b = \frac{2}{\sqrt{3}} \cdot \frac{I_{ref}}{I_{DC}} \cdot \sin\theta \\ \tau_0 = 1 - \tau_a - \tau_b \end{cases} \tag{4.3}$$

$$\begin{cases} T_a = \tau_a \cdot T_{sw} \\ T_b = \tau_b \cdot T_{sw} \\ T_0 = \tau_0 \cdot T_{sw} \end{cases} \tag{4.4}$$

Initially in this work, a base modulation was chosen, the sequence of applied vectors is $\vec{I}_0$-$\vec{I}_a$-$\vec{I}_b$ for each switching period T_{sw}, for each sextant, Table 4.2 describes all possible sequences associated with each vector in each sextant ("1" = MOSFET on, "0" = MOSFET off). In Table 4.2 the intermediate overlap sequences are not mentioned.

Base modulation is not the only existing one: an overview is presented in [19]. Even if the switching frequency is limited for medium voltage applications, the paper describes very well the influence on the 5^{th} and 7^{th} harmonic components of different modulation techniques, as well as the idea of selective harmonic cancellation. Simulations showed that the base modulation, when applied to the motor of subsection 4.2, did not cancel out the 5^{th} and 7^{th} harmonics. After applying Clarke and Park transformations, passing from (a, b, c) to (d, q), both harmonics sum up to the 6^{th} harmonic. Therefore, a 6^{th} harmonic will be present in i_q current. When the electric motor spins at a certain speed, such as that the corresponding electrical frequency is $1/6^{th}$, $1/12^{th}$,... of the resonance frequency of the LC circuit formed by the motor inductances and the output capacitors, the resonance can be activated [18]. The consequence is a strong oscillation of i_q and therefore a strong oscillation of the torque. If the oscillation is great, it could lead to uncontrollability of the motor. For this reason, an alternate SVPWM modulation was chosen: during the first switching period $\vec{I}_0$-$\vec{I}_a$-$\vec{I}_b$ are applied, and at the next one the sequence switches to $\vec{I}_b$-$\vec{I}_a$-$\vec{I}_0$. This alternate modulation reduces the frequency at which the transistors commute, reducing the switching losses, the switching frequency of the converter

Table 4.2: Base SVPWM modulation.

Sextant	Vector	S_1	S_2	S_3	S_4	S_5	S_6
I	$\vec{I}_0$	1	0	0	1	0	0
	$\vec{I}_a$	1	0	0	0	1	0
	$\vec{I}_b$	1	0	0	0	0	1
II	$\vec{I}_0$	0	0	1	0	0	1
	$\vec{I}_a$	1	0	0	0	0	1
	$\vec{I}_b$	0	1	0	0	0	1
III	$\vec{I}_0$	0	1	0	0	1	0
	I_a	0	1	0	0	0	1
	$\vec{I}_b$	0	1	0	1	0	0
IV	$\vec{I}_0$	1	0	0	1	0	0
	I_a	0	1	0	1	0	0
	$\vec{I}_b$	0	0	1	1	0	0
V	$\vec{I}_0$	0	0	1	0	0	1
	$\vec{I}_a$	0	0	1	1	0	0
	$\vec{I}_b$	0	0	1	0	1	0
VI	$\vec{I}_0$	0	1	0	0	1	0
	$\vec{I}_a$	0	0	1	0	1	0
	$\vec{I}_b$	1	0	0	0	1	0

is in fact reduced to $2/3\, f_{sw}$. It naturally follows that the high frequency harmonic injection gets worse with respect to the traditional SVPWM, but the resonance is damped, since the 5^{th} and 7^{th} harmonics of the injected currents are damped. A comparison between the two modulations, when the electric drive follows MTPA and Flux-Weakening strategy described in subsection 4.4.2, is shown in Figure 4.12. Around 9800 rpm, the base modulation enables the resonance, which has a proper frequency of ~ 1960 Hz (around six times the equivalent electric frequency of the motor). Figure 4.13 compares the results of the Fast Fourier Transform (FFT) for base and alternate modulation. Even if, the alternate modulation has high order harmonics at 30 kHz, it does not have low order harmonics. Instead, the base modulation has a better spectrum at high frequencies, but at 1633 Hz and 2286 Hz there are two small harmonics of amplitude 10.8 and 10.3 A compared to the fundamental frequency, but big enough to enable the resonance.

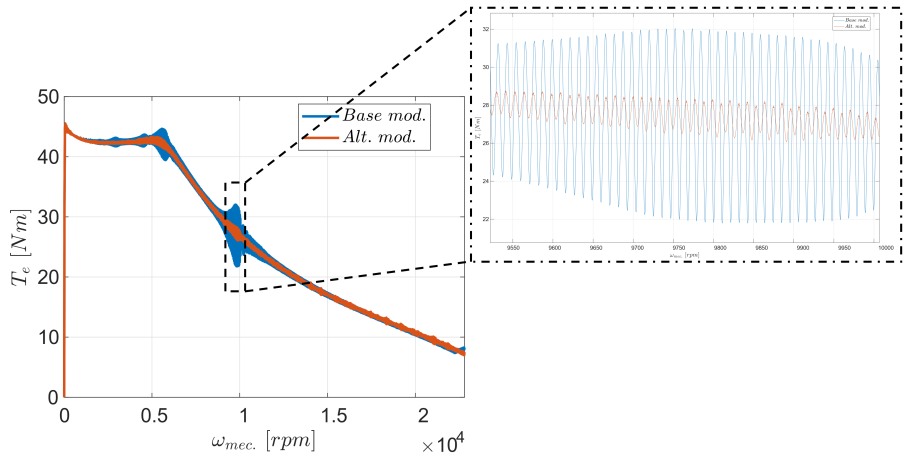

Figure 4.12: Motor electrical torque with with base and alternate modulation.

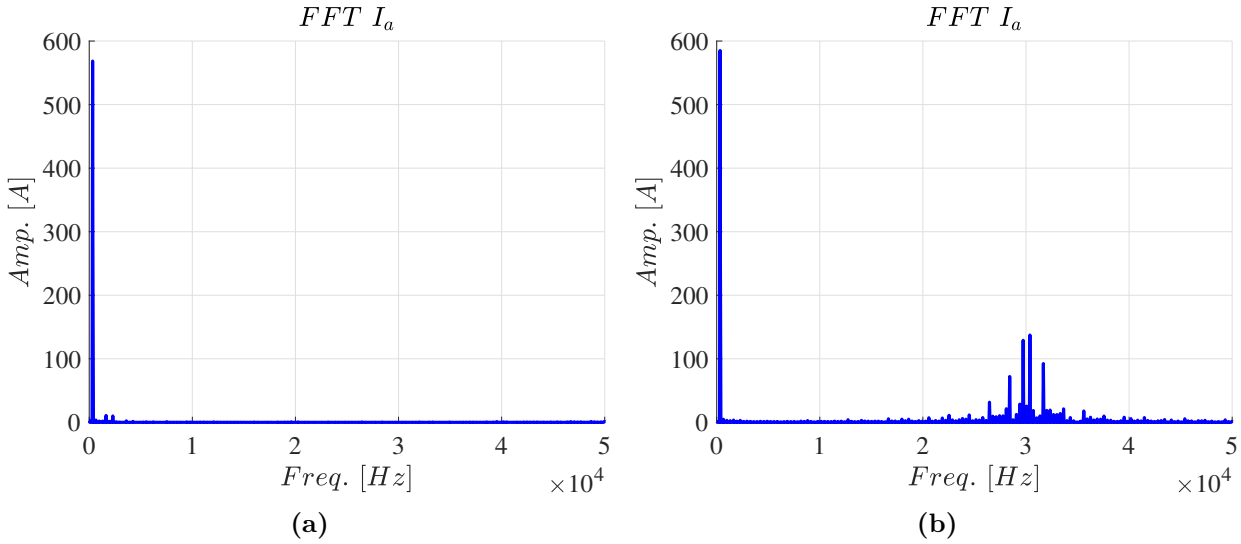

Figure 4.13: FFT of phase current i_a near the resonance: a) base modulation and b) alternate modulation.

4.5 Performance Comparison

In terms of performance comparison, the power in the most significant point should be evaluated. In Figure 4.14 a comparison is reported between the torque-speed curves of the motor with VSI and CSI (with and without overlap control). The power is evaluated in three significant points:

1. Base speed at nominal torque;
2. Final flux weakening speed for VSI (9000 rpm);
3. Final maximum speed reached (23000 rpm).

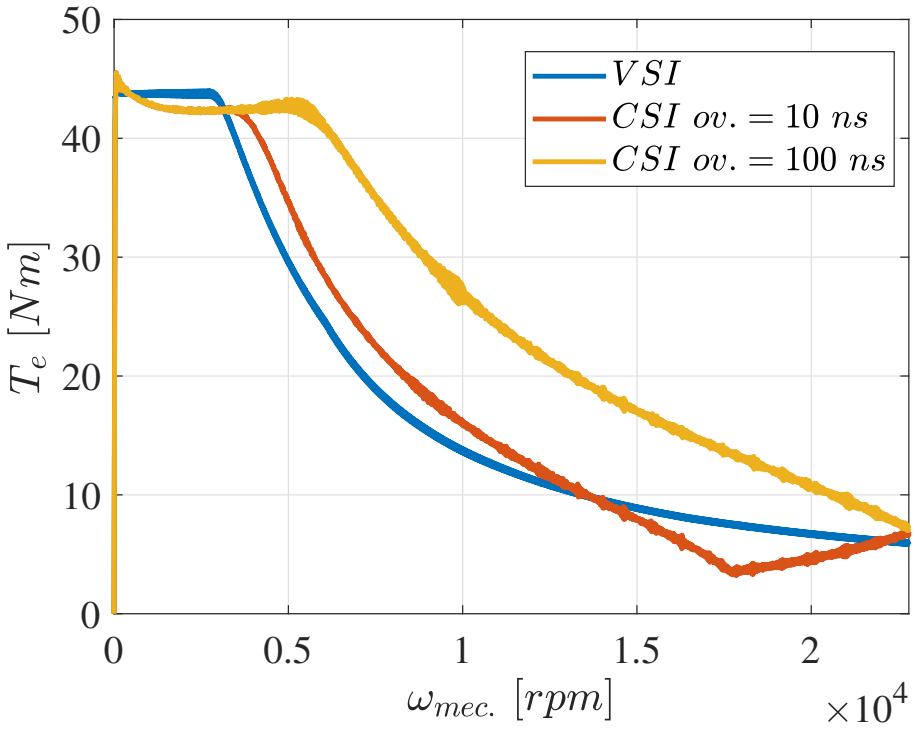

Figure 4.14: Motor electrical torque with VSI and with CSI with and without the overlap control. With an overlap of 10 ns (red curve) is not possible to reach 23000 rpm.

Table 4.3: Power Comparison

Configuration	Speed [rpm]	Torque [Nm]	Power [kW]
VSI	3062	43.8	14
CSI with $OV = 10$ ns	3420	42.4	15.2
CSI with controlled OV	5000	43.2	22.6
VSI	9000	15.2	14.3
CSI with $OV = 10$ ns	9000	17.9	16.8
CSI with controlled OV	9000	29.2	27.5
VSI	23000	5.9	14.2
CSI with $OV = 10$ ns	23000	6.7	16.1
CSI with controlled OV	23000	7.7	18.6

One of the main key performance indicator for an electric drive is the efficiency, therefore it is important to correctly compute both the motor and the inverter efficiency. Here, it must be specified that losses on L_{DC} for the CSI and on C_f for the VSI have not been taken into account. In the first subsection, the efficiency computation of the converter stage is explained and in the second one the power losses on the motor are compared.

As already mentioned one of the main advantage in employing a CSI is that the voltage waveform applied to the motor have a significant lower dv/dt with respect to the PWM output voltage of a VSI. However, in order to study the different effects on the insulation degradation a separate and complicated model of the insulation system should be made and that is not the aim of this work. In the first subsection, the efficiency computation of the converter stage is explained and in the second one the power losses on the motor are compared.

4.5.1 Converter efficiency comparison

To compute the efficiency a PLECS feature is employed [20], in fact, the software allows computing the power losses of a switch, if a thermal model is defined. When creating a new thermal model in PLECS, conduction and switching losses need to be specified: both can be derived from the device datasheet. Conduction losses are easy to evaluate since it is sufficient to extrapolate points from the drain-source voltage- drain current curve $v_{DS} - i_D$. Switching losses, instead, are more complicated to compute: an efficient way is to derive a value of the switch-on and switch-off losses E_{on} and E_{off} for a specific value of the couple ($V_{block} - I_{load}$) and then upload the results in PLECS. The same algorithm of Chapter 1 was employed. In this study, EPC2304 GaN FETs in parallel are used. EPC2304 [21] and VS-100BGQ100 diode [22] were chosen for the comparison. For both architectures, the efficiency values were evaluated under three different conditions: base speed ω_B, 9000 rpm and highest speed reached $\omega_{max} = 23000$ rpm. The switching frequency chosen for both VSI and CSI was $f_{sw} = 60$ kHz. Results are resumed in Table 4.4 for the CSI and in Table 4.5 for the VSI. When comparing the two architectures, Table 4.4 and 4.5, it appears that the CSI has lower efficiency, and that is due to the diodes continuous conduction over time; however, differences are very slight. Considering the possibility of avoiding MTPV, the lower stress on the motor insulation and the lower THD % of the motor currents, CSI becomes very interesting for traction application. Moreover, consideration on the motor losses should also be made, to make the whole comparison.

Table 4.4: Efficiency of CSI.

$f_{sw,CSI} = 60$ **kHz**	**Input Power** [W]	**Power losses pre-stage** [W]	**Power losses CSI** [W]	**Efficiency** [%]
Base speed $\omega_B = 5000$ **rpm**	11937	320	675	91.70
Final FW speed $\omega = 9000$ **rpm**	13733.8	88.04	176.4	98.04
Max speed $\omega_{max} = 23000$ **rpm**	22286.8	115.9	256.7	98.33

Table 4.5: Efficiency of VSI.

$f_{sw} = 60$ **kHz**	**Input Power [W]**	**Power losses VSI** [W]	**Efficiency** [%]
Base speed $\omega_B = 3500$ **rpm**	7570	545.73	92.83
Final FW speed $\omega = 9000$ **rpm**	13906	251.52	98.2
Max speed $\omega_{max} = 23000$ **rpm**	14420	234	98.39

4.5.2 Motor losses

From the motor efficiency point of view, one of the most critical point is to reduce the ripple of the current in input to the motor, because it leads to important drawbacks that can affect significantly the overall performance of the machine. The machine simulated with perfect sinusoidal stator currents (ideal condition reached with CSI) has a global efficiency of 88.3 % at 23000 rpm, where considering a current ripple of about 4% of the main current component, so with an overall good sinusoidal shape of the currents, a reduction of the efficiency of the motor of 1 % can be obtained. Nevertheless, the overall efficiency is not the only advantage; the losses on the magnets also depends on the current ripple. Although they can be reduced by segmenting the magnet along the axial direction but this affects the K_e of the machine. By using a CSI these losses are highly reduced, leading to a minor risk of magnet demagnetization and overheating. The previous study on the ironless motor in Chapter 3, showed the potential of driving a CSI for an ironless motor, from the motor point of view. Even if the advantages are less evident, the statement remains true.

4.6 Conclusion

A new extended MTPA-FW control technique for a CSI and a comparison with a more traditional VSI topology are presented: the FW control for the CSI was implemented to obtain the maximum exploitation of the system for a typical constant power region profile; thanks to the CSI the base speed can be increased by modifying dynamically in the control loop the overlap time, in order to exploit the CSI intrinsic capability to boost in voltage, so a new control model was proposed. The extended speed above the base speed was obtained combining the intrinsic boosting capability of the CSI with a flux weakening control strategy. This combined control strategy allows one to obtain high speed region without MTPV, which, on the other side, is mandatory with the traditional VSI topology when high speed values are desired, incrementing the complexity of the motor control.

The comparison was made considering a 13.8 kW liquid cooled IPM machine for light electric vehicle. In order to simplify the analysis, the magnetic saturation effect is not considered, so the inductance on d and q axis are kept constant. In the comparison also the pre-stage losses for the CSI are considered and the additional losses in the motor related to the current ripple for the VSI.

Thanks to the new extended MTPA-FW control mode of the CSI and its boost capability, the overall torque (and power) obtained is maximized in the entire speed range taken into account. Furthermore, the current given as an input to the motor has almost null ripple, so the PWM losses which generally affect the total output power are very low compared to the one traditionally obtained with the VSI topology. Even if the CSI converter is slightly less efficient compared to the VSI, the overall system efficiency, considering also the motor losses and performance, supports the proposed topology.

4.7 References

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5. Innovative Asymmetric Modulation for a Resonant Dual Active Bridge

5.1 Introduction

This work was made possible by the collaboration with the company SMART INDUCTION CONVERTER TECHNOLOGIES S.L. (SiCtech Induction) in Valencia. The project was developed during the period abroad in 2024 and then ended in 2025, leaving space for interesting further developments. Hardware and FPGA code are protected as they were developed by employees of the company. The conceptualization, analytical dissertation, simulation, and Hardware-in-the-Loop (HIL) validation were entirely made by the author. Polytechnic of Turin gently borrowed the instrumentation for HIL.

As stated in the Introduction, several power converters have been employing WBG and especially SiC technology for a long period of time. Out of those, resonant converters for induction systems, which is SiCTech core business and DC/DC resonant converter are worth mentioning. With the world pushing towards transportation electrification and with the wide spreading of utilitarian and non- electric vehicles (EVs) into the market, the idea of integrating battery chargers directly on vehicles raised. On board chargers are composed by three elements [1]: an EMI filter, an AC/DC converter which rectifies the grid voltage over a Bus DC, most-likely film capacitors and an efficient Bidirectional DC/DC converter that allows the power transfer from the grid to battery and vice versa in a V2G (Vehicle to Grid) configuration. Achieving a very high efficiency in the DC/DC conversion is trivial and needed, but not as easy as for low power applications. Several investigations on the converter topology have been made throughout the years along with several studies on different modulation techniques. The most common topologies are either Dual Active Bridges, DAB, or resonant DAB, since they are suited for achieving Zero-Voltage Switching (ZVS), Zero-Current Switching (ZCS) or in some cases both. ZVS condition is satisfied when the energy stored into the inductance seen by the full-bridge output is higher than the energy needed to charge and discharge the output capacitance C_{oss} of the commutation switches during dead-time, [2]. As stated by the same authors, an incomplete

ZVS, or iZVS, causes non-negligible turn-on losses in the switch and leads to an efficiency drop. ZCS condition is instead achieved when the device is switching off at zero current. ZCS is generally harder to obtain and a precise measurement of the current flowing in the resonant tank is needed. In [3], ZVZCS (Zero-Voltage Zero-Current Switching) is achieved for four out of eight switches, but requires additional snubber circuits. Moreover, even if very impressive, this condition is reached over 1 kW of power range which is too small for an on-board charger application. A similar consideration can be made for the work in [4]. For this reason, a more stable and easier to implement ZVS condition is seek for all the eight switches of a CLLC resonant DAB, while trying to minimize the total turn-off power losses of the converter, therefore aiming but not reaching a ZCS condition over a wide power range as required by the application. Some papers employed a tunable resonant network or transformer to achieve a wide power range application [5]–[8]. The problem with these types of application are both the architecture complexity and the cost of the magnetic parts. An investigation on the effect of a non-traditional modulation on resonant series DC/DC converter was made in [9]. A triple-phase shift modulation, briefly described in the next subsection and optimized for a DAB converter in [10]–[12], was also adopted for the topology studied in [13], [14]. Authors of [13] employed a TPS (Triple phase shift) with fixed frequency, however, a more efficient modulation is proposed with the aim of minimizing the total losses without varying the switching frequency as in [14] and [15]. Changing the frequency guarantees high efficiencies as demonstrated in [16] and [17], however without a tunable resonant network, the designer should employ a transformer which is not optimized for every switching frequency in the range of variation. At the same time, given a certain RMS current, the switching losses in the transistors increase. The control of the converter also becomes more complex with a frequency modulation. In [17] the output power is obtained through frequency variation but the hyperbolic law describing the relation is practically hard to replicate. Moreover, a variable switching frequency modulation would require a careful analysis on the transformer losses and deteriorates Electromagnetic Interference, that implies higher costs for EMI/EMC filters. Because several studies on the possible modulation techniques applicable to a DAB already exist in literature and also optimal converter designs were already studied [18], focus was given to a new fixed frequency modulation pattern applied to a Resonant CLLC DAB.

The focus of this project is the development of a modulation inspired by the AVC (Asymmetric Voltage Cancellation) technique described in [19] for a resonant FB (complete bridge) converter, that was extended to a resonant DAB, creating a new modulation strategy called Double AVC

modulation. Specifically, the resonant DAB architecture will be described in subsection 5.2 and the technique in subsection 5.3. In subsection 5.4, the algorithm used to define the optimal operating conditions over the desirable power range is described, in subsection 5.5 the simulation results are presented, and in subsection 5.6 the experimental setup and the results of the tests are shown. Finally, conclusions are drawn in subsection .

5.2 Resonant DAB configuration

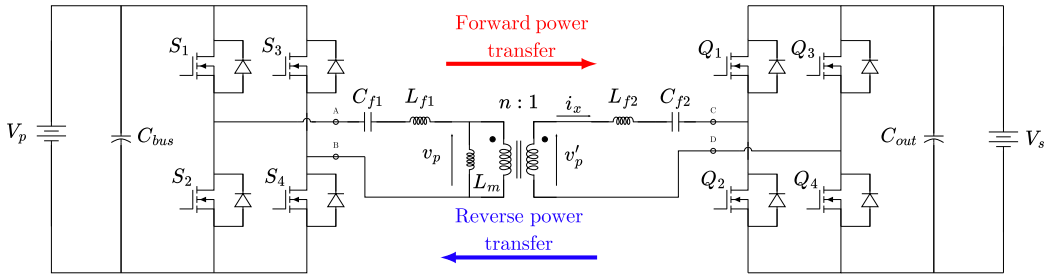

Figure 5.1: Series resonant CLLC Dual-Active Bridge topology.

The CLLC Resonant Dual-Active Bridge studied is shown in Figure 5.1. V_p and V_s represent the primary and secondary voltage, respectively: the first one represents the rectified grid voltage by the AC/DC converter, which is omitted in the schematic, and the second one the battery voltage. S_1, S_2, S_3 and S_4 are the switches of the first full-bridge (FB1) and Q_1, Q_2, Q_3 and Q_4 are the switches of the second full-bridge (FB2). Regarding tank topology, a CLLC resonant tank is defined. An conventional LC resonant topology is not suited for the asymmetric modulation presented in the next subsection, since an asymmetric voltage inevitably leads to a DC current component which could saturate the transformer core. For this reason, the resonant inductance L_f the resonant capacitor C_f are split on the two sides of the transformer, in order to eliminate the continuous component and allow the power transfer in both directions avoiding the transformer saturation. The employed values will be enounced in subsection 5.5. Having said that, a single equivalent LC tank will be considered for a more transparent dissertation and the relation between the values are defined in (5.1).

$$\begin{cases} L_f = \frac{L_{f1}}{n^2} + L_{f2} \\ C_f = \frac{n^2 C_{f1} \cdot C_{f2}}{n^2 C_{f1} + C_{f2}} \end{cases} \tag{5.1}$$

where n is the transformer ratio. L_m of Figure 1 represents the magnetizing inductance of the transformer and both C_{bus} and C_{out} are just DC Bus capacitors. Here, the adopted convention is the most common in literature: *forward power transfer* when the battery is charged by the grid and *reverse power transfer* when the battery injects power into the grid.

5.3 Modulation techniques

5.3.1 Introduction to the modulation techniques

As mentioned in subsection 5.1, several modulation techniques exist in literature. In this subsection, an existing technique, TPS modulation, is briefly explained and compared to the proposed asymmetric voltage modulation for this resonant DAB. For a deeper understanding of the traditional technique, see papers [10]–[15]. A comparison in terms of simulations, will be carried out in subsection 5.5. The following is dedicated to the Triple Phase Shift (TPS) modulation, which is considered the state-of-the-art and will be compared with the proposed modulation, the double AVC and that will be explained in details.

5.3.2 TPS modulation

The TPS modulation is a symmetrical modulation applicable to a DAB converter. In papers [10] and [11] it has been applied to a non-resonant and in paper [12], the TPS modulation is optimized for a closed-loop control at fixed switching frequency f_{sw}. The concept has already been transferred to a series LC resonant DAB in papers [13]–[15]. Especially in [15], a TPS that minimizes the power losses has been developed. TPS modulation includes six possible states, forward power transfer is considered, from FB1 to FB2. six additional states can be defined for the reverse power transfer, therefore it allows a significant flexibility. However, as it will be shown in the comparison, the AVC modulation applied to the resonant DAB guarantees higher performances due to the lower tank current and at the same time, lower currents during turn-off in the whole power range. Differently from the research in [12], the shift from one state to the other, for both TPS and AVC modulation, is dictated by the algorithm described in the next subsection. The choice was made to have a fair comparison between the two modulations. As shown by Table 5.1, the difference between one mode and another one depends on the relation between the three variables, or degree of freedom, d_1, d_2 and d_3. Their meaning is explained in Figure 5.2: d_1 represents FB1 duty-cycle, d_2 FB2 duty-cycle and d_3 the internal phase shift

between the two bridges. It is sufficient to multiply for $T_{sw}/2$ to obtain t_1, t_2 and t_3. t_5, t_6 and t_7 are defined from t_1,t_2 and t_3 by the symmetry of the modulation in the second half of the switching period.

Table 5.1: TPS modulation modes.

Mode	t_0	t_1	t_2	t_3	t_4
1	0	$d_3 \cdot \frac{T_{sw}}{2}$	$(d_2+d_3) \cdot \frac{T_{sw}}{2}$	$d_1 \cdot \frac{T_{sw}}{2}$	$\frac{T_{sw}}{2}$
2	0	$d_1 \cdot \frac{T_{sw}}{2}$	$(d_2+d_3-1) \cdot \frac{T_{sw}}{2}$	$d_3 \cdot \frac{T_{sw}}{2}$	$\frac{T_{sw}}{2}$
3	0	$d_1 \cdot \frac{T_{sw}}{2}$	$d_3 \cdot \frac{T_{sw}}{2}$	$(d_2+d_3) \cdot \frac{T_{sw}}{2}$	$\frac{T_{sw}}{2}$
4	0	$(d_2+d_3-1) \cdot \frac{T_{sw}}{2}$	$d_1 \cdot \frac{T_{sw}}{2}$	$d_3 \cdot \frac{T_{sw}}{2}$	$\frac{T_{sw}}{2}$
5	0	$(d_3+1) \cdot \frac{T_{sw}}{2}$	$d_1 \cdot \frac{T_{sw}}{2}$	$(d_2+d_3) \cdot \frac{T_{sw}}{2}$	$\frac{T_{sw}}{2}$
6	0	$(d_2+d_3-1) \cdot \frac{T_{sw}}{2}$	$d_3 \cdot \frac{T_{sw}}{2}$	$d_1 \cdot \frac{T_{sw}}{2}$	$\frac{T_{sw}}{2}$

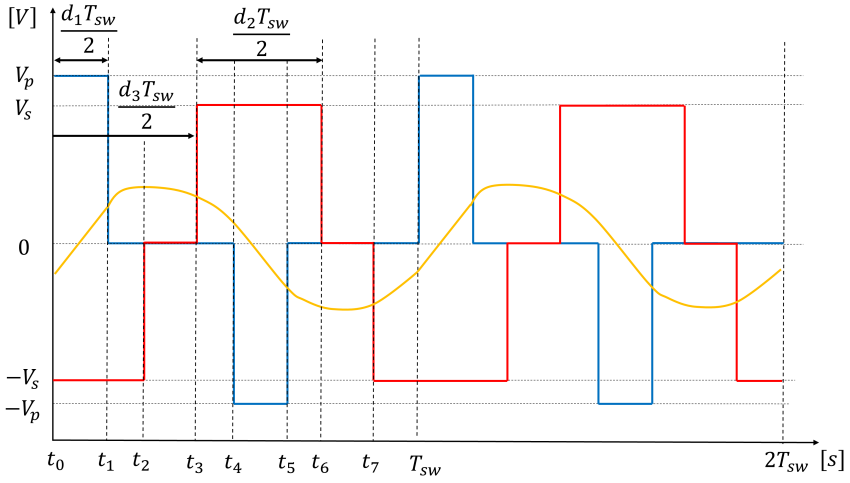

Figure 5.2: TPS modulation applied to a resonant DAB, mode 2. Primary full-bridge FB1, output voltage (blue), secondary full-bridge FB2, output voltage (red) and resonant tank or inductor current seen by the transformer primary circuit (yellow).

Figure 5.2 refers to the case $V_p > V_s$, where the primary voltage is superior to the secondary voltage. The classification of the modes does not change if the relation is inverted.

5.3.3 Proposed Double AVC Modulation

The Asymmetric Voltage Modulation (AVC) was applied by the authors of [19] to a full-bridge with a series LC resonant tank on a resistive load. The AVC technique is here applied to a resonant DAB. The advantage of applying a double AVC modulation to this type of converter

is the possibility of obtaining ZVS for all switches over a wide range of power while keeping the switching frequency f_{sw} fixed to a value superior to the resonant frequency f_r. A fixed switching frequency, in fact, allows to exploit the resonant tank at the best possible efficiency, close to its resonance and simplify the converter control as well. Mathematically, the output voltages of FB1 and FB2 can be expressed with Fourier series with an infinite number of harmonics, (5.2).

$$\begin{cases} v_{AB}(t) = V_{AB.0} + \sum_{i=1}^{\infty} a_{i,p}\cos(\omega t) + b_{i,p}\sin(\omega t) \\ v_{CD}(t) = V_{CD.0} + \sum_{i=1}^{\infty} a_{i,s}\cos(\omega t) + b_{i,s}\sin(\omega t) \end{cases} \tag{5.2}$$

where $a_{i,p}$, $b_{i,p}$, $a_{i,s}$ and $b_{i,s}$ are the Fourier coefficients and $V_{AB,0}$, $V_{CD,0}$ are the continuous components of both voltages. In literature, the most common approach employed to study the CLLC Resonant DAB topology is the FHA or first harmonic approximation, employed in [20] for example, which is taken into account here. Other sophisticated methods like State Space Analysis (SPA) in [21] already exist in literature, but since the FHA allowed obtaining ZVS for each of the eight switches, it is tolerated the over- or underestimation of the losses in a single operating point. The approximation consists of the omission of the 2nd and 3rd harmonics, which are usually the most significant excluding the first. Because the FHA led to experimental results that are consistent with the analytical dissertation, in-depth analyses were not considered. Indeed, the aim is not to provide a detailed and precise description of the converter. Employing the FHA, only four coefficients need to be calculated (5.3)-(5.6), each of them corresponding to a coefficient of the Fourier series. Substituting them in (5.2), the expression in (5.7) can be found.

$$a_{1,p} = \frac{2}{T_s}\cdot\left\{\int_0^{\frac{\beta_p-\alpha_{+,p}}{\omega}} V_p\cos(\omega t)dt - \int_{\frac{2\pi-\beta_p}{\omega}}^{\frac{2\pi-\alpha_{-,p}}{\omega}} V_p\cos(\omega t)dt\right\} \tag{5.3}$$

$$\begin{aligned} a_{1,s} = \frac{2}{T_s}\Bigg\{ &-\int_0^{\frac{\theta-\alpha_{+,s}}{\omega}} V_s\cos(\omega t)dt + \int_{\frac{\theta}{\omega}}^{\frac{\theta+\beta_s-\alpha_{+,s}}{\omega}} V_s\cos(\omega t)dt \\ &- \int_{\frac{\theta+\beta_s-\alpha_{+,s}+\alpha_{-,s}}{\omega}}^{\frac{2\pi}{\omega}} V_s\cos(\omega t)dt\Bigg\} \end{aligned} \tag{5.4}$$

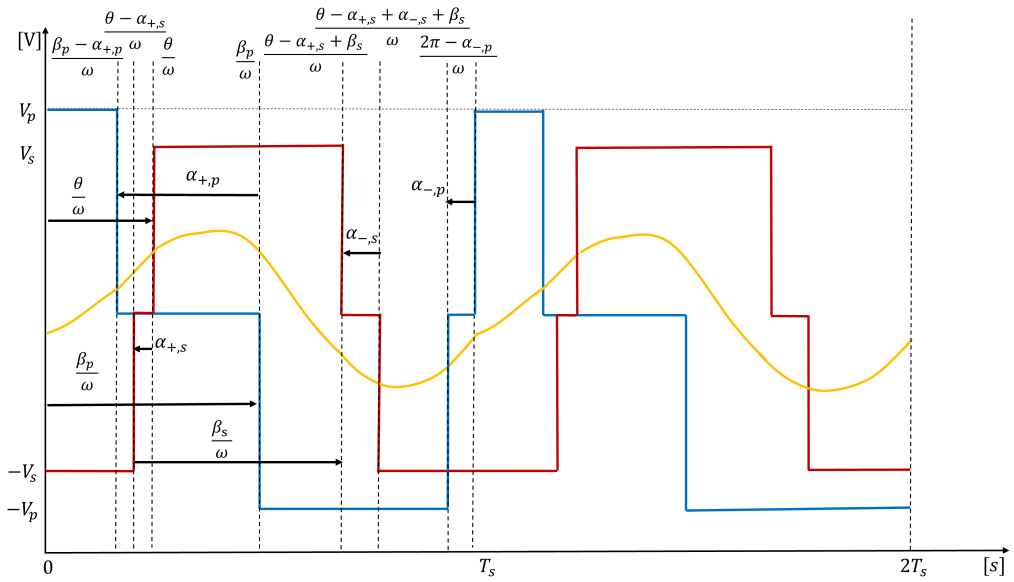

Figure 5.3: General conceptualization of the Double AVC modulation.

$$b_{1,p} = \frac{2}{T_s} \cdot \left\{ \int_0^{\frac{\beta_p - \alpha_{+,p}}{\omega}} V_p \sin(\omega t) dt \; - \int_{\frac{\beta_p}{\omega}}^{\frac{2\pi - \alpha_{-,p}}{\omega}} V_p \sin(\omega t) dt \right\} \tag{5.5}$$

$$\begin{aligned} b_{1,s} = \frac{2}{T_s} \Bigg\{ & - \int_0^{\frac{\theta - \alpha_{+,s}}{\omega}} V_s \sin(\omega t) dt \; + \int_{\frac{\theta}{\omega}}^{\frac{\theta + \beta_s - \alpha_{+,s}}{\omega}} V_s \sin(\omega t) dt \\ & - \int_{\frac{\theta + \beta_s - \alpha_{+,s} + \alpha_{-,s}}{\omega}}^{\frac{2\pi}{\omega}} V_s \sin(\omega t) dt \Bigg\} \end{aligned} \tag{5.6}$$

The variables $\alpha_{+,p}$, $\alpha_{-,p}$, β_p, $\alpha_{+,s}$, $\alpha_{-,s}$, β_s and θ are explained in Figure 5.3.

$$\begin{cases} v_{AB}(t) = V_{AB.0} + \; a_{1,p} \cos(\omega t) + b_{1,p} \sin(\omega t) \\ v_{CD}(t) = V_{CD.0} + a_{1,s} \cos(\omega t) + b_{1,s} \sin(\omega t) \end{cases} \tag{5.7}$$

The calculation of the two continuous components is not necessary to derive the tank current $i_x(t)$, since the resonant tank cuts out the DC components from both output voltages of the two full-bridges. The expression of $\bar{I}_x$, which is the corresponding phasor considering the first harmonic approximation, can be found considering the system of two equations in (5.8) and

equalizing them (5.9). Thus, the expression of $i_x(t)$ is found in (5.10).

$$\begin{cases} \bar{I}_x = \frac{\bar{V}_{AB} - \bar{V}_p}{\bar{Z}_1} \\ \bar{I}_x = \frac{\bar{V}_p' - \bar{V}_{CD}}{\bar{Z}_2} \end{cases} \tag{5.8}$$

$$\bar{I}_x = \frac{\left(\frac{\bar{V}_{AB}}{n} - \bar{V}_{CD}\right)}{\left(\frac{\bar{Z}_1}{n^2} + \bar{Z}_2\right)} \tag{5.9}$$

$$i_x(t) = k \cdot \left[\left(\frac{b_{1,p}}{n} - b_{1,s} \right) \cdot \cos(\omega t) + \left(a_{1,s} - \frac{a_{1,p}}{n} \right) \cdot \sin(\omega t) \right] \tag{5.10}$$

where $k = (\omega C_f)/(1 - \omega^2 L_f C_f)$, which is always negative if the switching frequency is higher than the resonant frequency. This condition also corresponds to the choice made here, since ZVS increases the converter efficiency with respect to ZCS. Any variation or mismatch of L_f and C_f would shift the resonant frequency. A sensitivity analysis on the variation of these parameters was not carried out; however, if the resonant capacitor employed C_f has a maximum capacitance variation of +/- 10% around the nominal value, this would not compromise the converter functioning. Due to the high switching frequency, L_f value is very low and wound in air, therefore it could be adjusted based on the leakage inductance of the transformer and on the value of C_f. Even if this issue was not investigated, the author believes that small discrepancies of the resonant frequency f_r do not impact dramatically the normal operation of the converter. Once the tank current expression is found, also its RMS value $I_{x,rms}$, the power output P_o, calculated as it is absorbed by FB2, and the output current I_o can consequently be derived in (5.11), (5.12) and (5.13).

$$I_{x,rms} = \sqrt{\frac{1}{2\pi} \int_0^{2\pi} {i_x}^2(\theta)\, d\theta} = |k| \sqrt{\frac{1}{2} \cdot \left[\left(\frac{b_{1,p}}{n} - b_{1,s} \right)^2 + \left(a_{1,s} - \frac{a_{1,p}}{n} \right)^2 \right]} \tag{5.11}$$

$$P_o = \frac{1}{2\pi}\int_0^{2\pi} v_{CD}(\theta)\cdot i_x(\theta)\,d\theta = \frac{k}{2}\cdot\left[a_{1,s}\cdot\left(\frac{b_{1,p}}{n}-b_{1,s}\right)+b_{1.s}\cdot\left(a_{1,s}-\frac{a_{1,p}}{n}\right)\right] \tag{5.12}$$

$$I_o = \frac{k}{2V_s}\cdot\left[a_{1,s}\left(\frac{b_{1,p}}{n}-b_{1,s}\right)+b_{1.s}\left(a_{1,s}-\frac{a_{1,p}}{n}\right)\right] \tag{5.13}$$

$I_{x,rms}$, P_o and I_o depend on k and therefore on the switching frequency and passive components of the resonant tank, as well as on the set of parameters ($a_{1,p}$, $b_{1,p}$, $a_{1,s}$, $b_{1,s}$). Looking at the expressions in (5.3)-(5.6), it is evident that there are seven variables that can be changed to obtain a specific value of the output power P_o. The mathematical dissertation would become extremely complicated, therefore some variables are set to constant values, see (5.14), in this first work for the sake of simplicity and industrial implementation without the need of an optimization solver of a non-linear set of equations. Consider that $\alpha_{+,p}$, $\alpha_{+,s}$ and β_s, β_p were simply renamed.

$$\begin{cases} \alpha_{-,p} = 0 \\ \alpha_{-,s} = 0 \\ \beta_p = \beta = \pi \\ \beta_s = \beta = \pi \\ \alpha_{+,p} = \alpha_p \\ \alpha_{+,s} = \alpha_s \end{cases} \tag{5.14}$$

Thus, as for the TPS modulation, several modes can be defined, especially for the double AVC modulation, and five cases can be distinguished: these are summarized in Table 5.2 and shown from Figure 5.4 to Figure 5.8. All figures refer to the case $V_p > V_s$, but the mode classification does not depend on the voltage levels, in fact, the classification of the modes does not change if the relation is inverted. The description of the curves is the same for all figures and is just declared in Figure 5.8.

Table 5.2: Double AVC modulation modes.

Mode	t_0	t_1	t_2	t_3	t_4	t_5
1	0	$\frac{\beta-\alpha_p}{\omega}$	$\frac{\theta-\alpha_s}{\omega}$	$\frac{\theta}{\omega}$	$\frac{\beta}{\omega}$	$\frac{\theta+\beta-\alpha_s}{\omega}$
2	0	$\frac{\beta-\alpha_p}{\omega}$	$\frac{\theta-\alpha_s}{\omega}$	$\frac{\beta}{\omega}$	$\frac{\theta}{\omega}$	$\frac{\theta+\beta-\alpha_s}{\omega}$
3	0	$\frac{\theta-\alpha_s}{\omega}$	$\frac{\beta-\alpha_p}{\omega}$	$\frac{\theta}{\omega}$	$\frac{\beta}{\omega}$	$\frac{\theta+\beta-\alpha_s}{\omega}$
4	0	$\frac{\theta-\alpha_s}{\omega}$	$\frac{\beta-\alpha_p}{\omega}$	$\frac{\beta}{\omega}$	$\frac{\theta}{\omega}$	$\frac{\theta+\beta-\alpha_s}{\omega}$
5	0	$\frac{\theta-\alpha_s}{\omega}$	$\frac{\beta-\alpha_p}{\omega}$	$\frac{\beta}{\omega}$	$\frac{\theta}{\omega}$	$\frac{\theta+\beta-\alpha_s}{\omega}$
6	0	$\frac{\theta-\alpha_s}{\omega}$	$\frac{\theta}{\omega}$	$\frac{\beta-\alpha_p}{\omega}$	$\frac{\beta}{\omega}$	$\frac{\theta+\beta-\alpha_s}{\omega}$

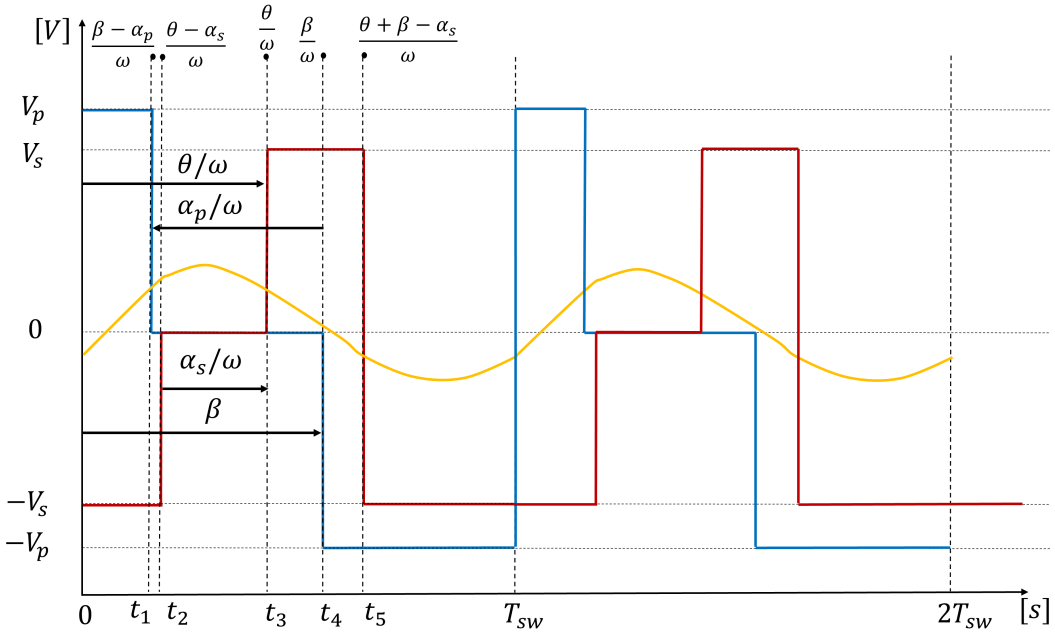

Figure 5.4: Modulation mode 1: $\beta - \alpha_p < \theta - \alpha_s < \theta < \beta$.

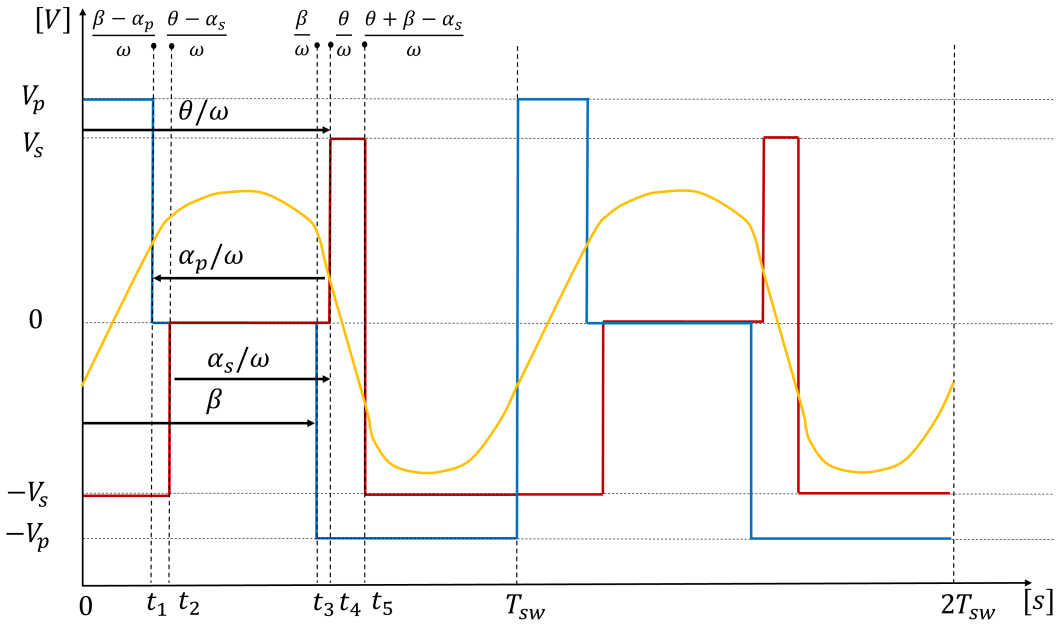

Figure 5.5: Modulation mode 2: $\beta - \alpha_p < \theta - \alpha_s < \beta < \theta$.

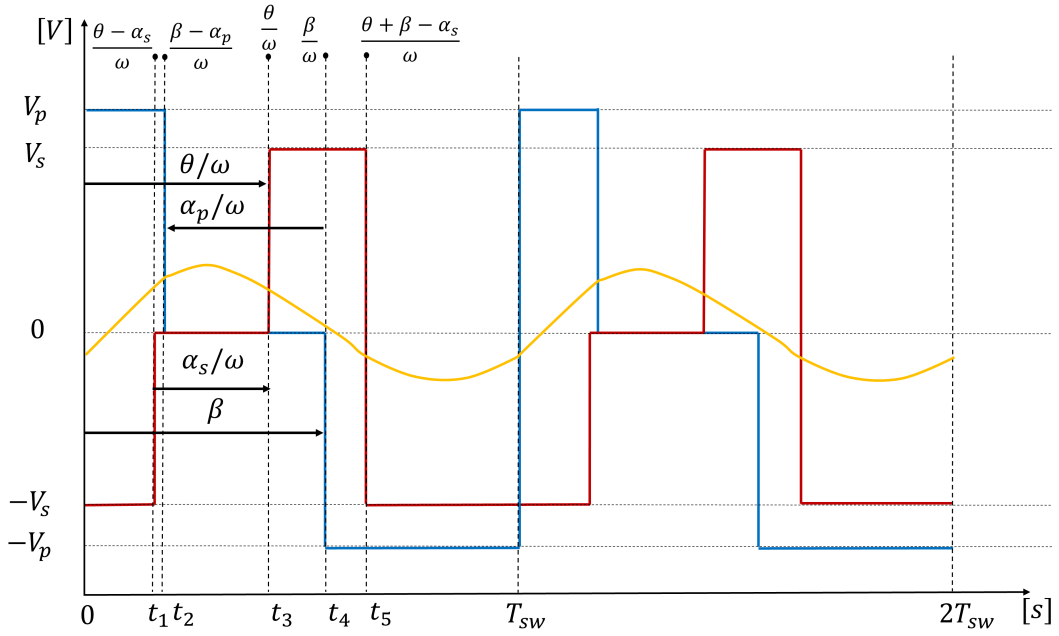

Figure 5.6: Modulation mode 3: $\theta - \alpha_s < \beta - \alpha_p < \theta < \beta$.

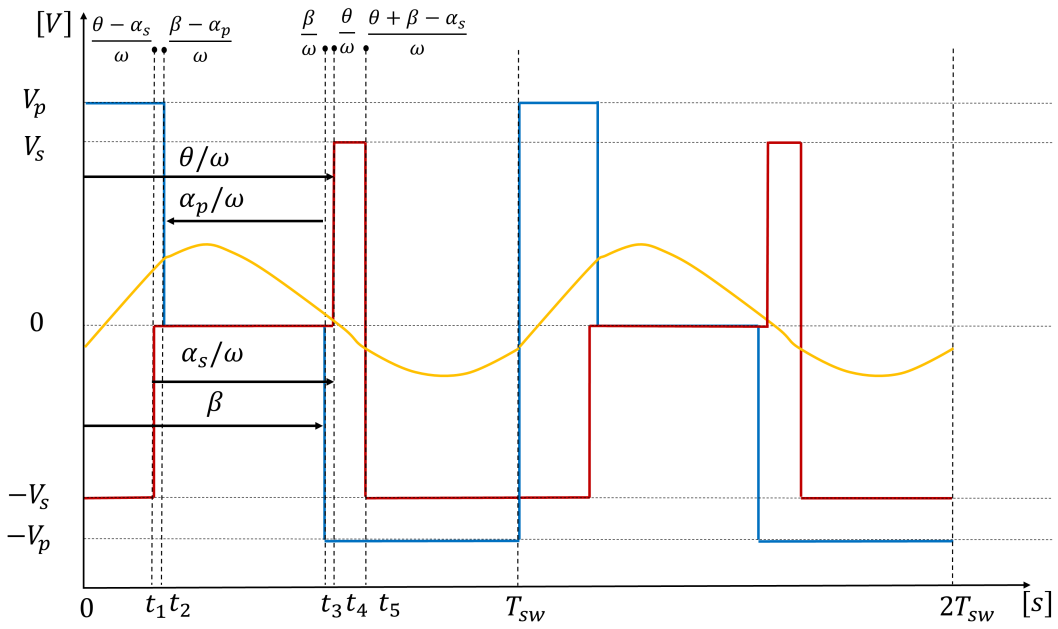

Figure 5.7: Modulation mode 4: $\theta - \alpha_s < \beta - \alpha_p < \beta < \theta$.

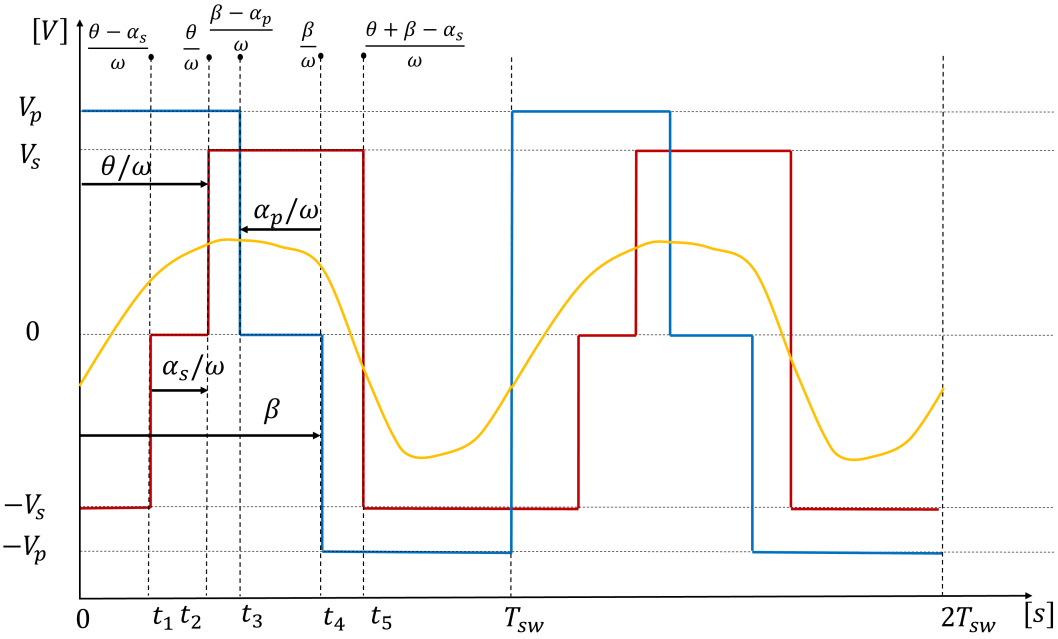

Figure 5.8: Modulation mode 5: $\theta - \alpha_s < \beta - \alpha_p < \theta < \beta$. Primary full-bridge, FB1, output voltage (blue), secondary full-bridge, FB2, output voltage (red) and resonant tank or inductor current seen by the transformer primary circuit (yellow).

Expressions (5.10)-(5.14) will be used in the next subsection to obtain an optimum array of values of the variable set $(a_{1,p}, b_{1,p}, a_{1,s}, b_{1,s})$ that minimizes the sum of power losses, imputable to the transistors, for each value of the requested power P_o. The approximate sinusoidal expression of the tank current in (5.10) is employed to guarantee the ZVS switching condition for each

transistor. (5.11), (5.12), (5.13) and (5.14) are used for the extraction of optimal parameters. Sixteen possible sequences are described in Table 5.3 and each mode is a set of six sequences, which may become five if α_p or α_s is equal to zero or four if both are null. In Table 5.5, modes are associated with their set of sequences when $\alpha_p = \alpha_s \neq 0$.

Table 5.3: Possible sequences of AVC modulation.

Sequence	S_1	S_2	S_3	S_4	Q_1	Q_2	Q_3	Q_4
1	1	0	0	1	0	1	1	0
1	1	0	0	1	1	0	1	0
3	1	0	0	1	0	1	0	1
4	1	0	0	1	1	0	0	1
5	1	0	1	0	0	1	1	0
6	0	1	0	1	0	1	1	0
7	1	0	1	0	1	0	1	0
8	1	0	1	0	0	1	0	1
9	0	1	0	1	1	0	1	0
10	0	1	0	1	0	1	0	1
11	1	0	1	0	1	0	0	1
12	0	1	0	1	1	0	0	1
13	0	1	1	0	0	1	1	0
14	0	1	1	0	1	0	1	0
15	0	1	1	0	0	1	0	1
16	0	1	1	0	1	0	0	1

Table 5.4: Association between modes and sequences.

Mode	**Seq. 1**	**Seq. 2**	**Seq. 3**	**Seq. 4**	**Seq. 5**	**Seq. 6**
1	1	5	7	11	16	13
2	1	5	7	14	16	13
3	1	2	7	11	16	13
4	1	2	7	14	16	13
5	1	2	4	11	16	13

There are other possible mode, which are not included in Table 5.5, but they could not guarantee ZVS for all the eight switches of the converter, therefore they do not represent a possible outcome of the algorithm described in subsection 5.4.

5.4 Optimal operating conditions and power output control

5.4.1 Algorithm for optimal operating conditions

The algorithm employed to find the optimal operating points is implemented in MATLAB, based on a root finding method: the bisectional method, which is very useful to solve systems of non-linear equations. First of all, some variables are fixed to a known value, in this way the number of degree of freedom can be reduced from seven to three. In this first work, it was considered to implement a modulation that does not require any use of non-linear solver.

$$\begin{cases} \alpha_{-,p} = 0 \\ \alpha_{-,s} = 0 \\ \beta_p = \pi \\ \beta_s = \pi \end{cases} \tag{5.15}$$

Therefore, the expressions of the four coefficients in (5.3)-(5.6), become the ones in (5.16).

$$\begin{cases} a_{1,p} = \frac{V_p}{\pi} \cdot \sin\left(\alpha_{+,p}\right) \\ b_{1,p} = \frac{V_p}{\pi} \cdot \left[3 + \cos\left(\alpha_{+,p}\right)\right] \\ a_{1,s} = \frac{V_s}{\pi} \cdot \left[-3\sin\left(\theta - \alpha_{+,s}\right) - \sin\left(\theta\right)\right] \\ b_{1,s} = \frac{V_s}{\pi} \cdot \left[3\cos\left(\theta - \alpha_{+,s}\right) + \cos\left(\theta\right)\right] \end{cases} \tag{5.16}$$

Then, values of $\alpha_{+,p}$ and$\alpha_{+,s}$ are swept over the range $[0, \pi]$ within two concatenated "for" cycles. Finally for each couple of values $[\alpha_{+,p}(i^{th}), \alpha_{+,s}(j^{th})]$, where i^{th} and j^{th} are the generic iterations of the for cycles, a solution to the problem needs to be seek. Here, the bisectional method starts until a value for θ is found for the aforementioned couple: particularly, substituting the expression in (5.16) inside (5.12) the value of P_o can be evaluated and when the stop condition

is satisfied (5.17), a valid solution is taken out.

$$P_{o,r} \ -\varepsilon < P_o < P_{o,r} \ +\varepsilon \tag{5.17}$$

where ε is a small error chosen at the start point and $P_{o,r}$ is the requested power. Only if (5.17) is satisfied, for each given requested power, a value of the triplet $[\alpha_{+,p}(i^{th}), \alpha_{+,s}(j^{th}), \theta]$ is saved, if it also allows ZVS for every transistor. The triplet becomes the optimal solution of the problem after all values are swept, if it also minimizes the converter power losses P_{loss}, excluding the losses due to the transformer which hard to estimate offline. The condition of ZVS is represented by the set of equations in (5.18).

$$\begin{cases} i_{x,1} = k\left[\left(\frac{b_{1,p}}{n} - b_{1,s}\right)\cos(0)\right] < -z \\ i_{x,2} = k\left[\left(\frac{b_{1,p}}{n} - b_{1,s}\right)\cos(\theta) + \left(a_{1,s} - \frac{a_{1,p}}{n}\right)\sin(\theta)\right] > z \\ i_{x,3} = k\left[\left(\frac{b_{1,p}}{n} - b_{1,s}\right)\cos(\pi)\right] > z \\ i_{x,4} = k\left[\left(\frac{b_{1,p}}{n} - b_{1,s}\right)\cos(\theta + \pi - \alpha_{+,s}) + \left(a_{1,s} - \frac{a_{1,p}}{n}\right)\sin(\theta + \pi - \alpha_{+,s})\right] < -z \end{cases} \tag{5.18}$$

where $a_{1,p}$,$b_{1,p}$, $a_{1,s}$,$b_{1,s}$ assume the expression in (5.16). Since the FHA assumes a sinusoidal shape for the tank current and since a non-zero current should circulate in the body-diode to allow the output capacitance discharge, value of c must be greater than zero: $z > 0$. P_{loss} are instead calculated as the sum of the conduction losses and turn-of losses for every MOSFET: turn-on losses are neglected since the ZVS condition is imposed. Conduction losses can be estimated through the resistance offered by the MOSFET while conducting $R_{DS,on}$, that is provided by the manufacturer. The resultant conduction losses are therefore computed as in (5.19).

$$P_{cond,M} = R_{DS,on} \cdot I_{x,rms,M} \tag{5.19}$$

where $I_{rms,M}$ is the rms current flowing in the power transistor M during a switching period. The applied formula does not change, but the value of $I_{rms,M}$ differs from one MOSFET to another. Since for the ZVS conditions, the tank current was considered sinusoidal, the same

approximation is perpetuated for the conduction losses calculations. The switching losses, instead, are always determined from the datasheet and, in addition, assuming the independency from the junction temperature since E_{off} losses are usually provided for a single temperature value. E_{off} are the only contribution to the switching losses and they are evaluated interpolating the datasheet curve, see (5.20).

$$E_{off,M} = a \cdot I_{off,M}^2 + b \cdot I_{off,M} + c \tag{5.20}$$

where $I_{off,M}$ is the switch-off current of the MOSFET M and a,b and c are the interpolation coefficients. The switching power losses are obtained multiplying (5.20) times the switching frequency f_{sw}. As for the conduction losses, the sinusoidal approximation is considered. The combination of (5.19) and (5.20) for each MOSFET returns the total P_{loss} (5.21). The discrimination between two or more possible solutions is made on the minimum value for these losses.

$$P_{loss} = \sum_{i=1}^{4} (P_{cond,S_i} + P_{off,S_i}) + \sum_{i=1}^{4} (P_{cond,Q_i} + P_{off,Q_i}) \tag{5.21}$$

For each power level: zero, one or more solutions are possible. At the end of the algorithm, which is summarized in , for each $P_{o,r}$ a ZVS solution that minimizes the power losses is found. The algorithm can be applied to different voltage levels: in this study the battery voltage changes from a low value, 250 V, discharged battery, to a high value 400 V, charged battery. If $P_{o,r} > 0$, the battery is charging, if $P_{o,r} < 0$, the battery is discharging, but the algorithm works in the same way. A summary of the algorithm for the optimal operational points is presented in Figure 5.9.

The algorithm is run offline and the values of α_p, α_s and θ are saved in three different size look-up tables $[v, p]$, where v is the vector size $\bar{V_s} = [V_{s,1}, V_{s,2}, \ldots, V_{s,v}]$ and p is the size of the requested power vector $\bar{P}_{o,r} = [P_{o,r,1}, P_{o,r,2}, \ldots, P_{o,r,p}]$.

It is worth to specify that this algorithm is hard to implement in real-time: a more efficient algorithm, in terms of computation, should be chosen for an online implementation. However, for on-board chargers, it is also very common in industrial applications to implement control through look-up tables interpolation. For this reason, the need to implement the algorithm

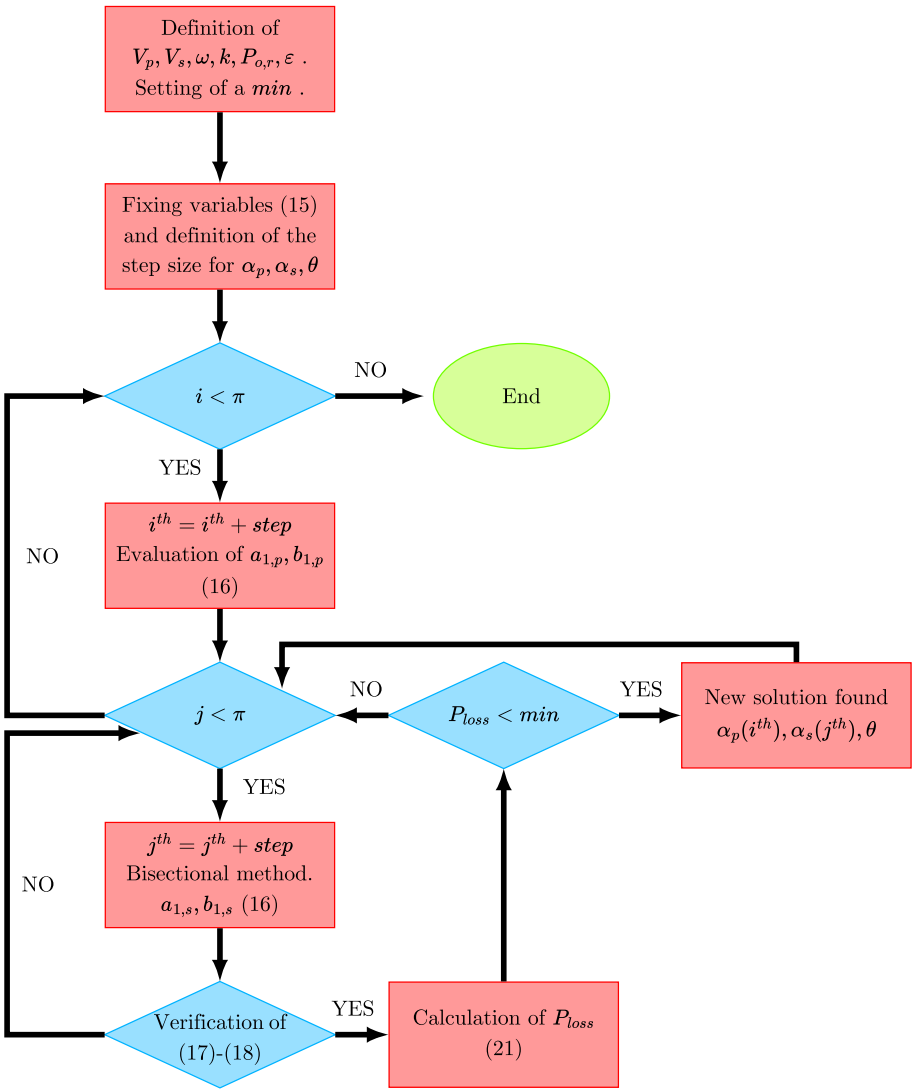

Figure 5.9: Optimal operation point algorithm.

online was not considered necessary.

5.4.2 Control strategy

The control strategy presented in this algorithm is based on a proper interpolation between the different look-up tables. Since a double AVC modulation can have five different modes which allows ZVS, depending on the mode, one, two or three look-up tables should be interpolated. The control strategy is therefore summarized in Figure 5.10 and implemented in C-script in the simulation.

The main idea behind this control is to obtain any power value for any voltage value of the battery on both reverse and forward power transfer, through a selective interpolation of the

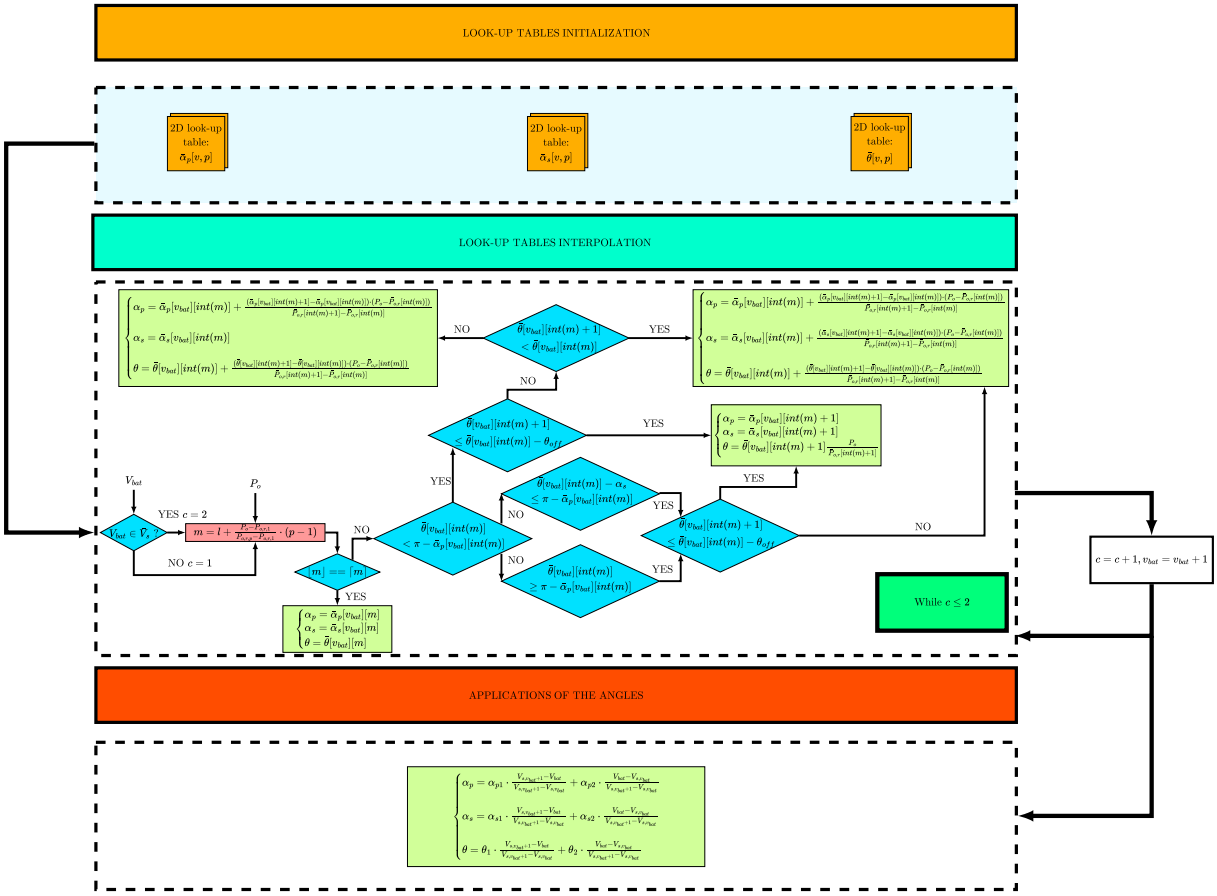

Figure 5.10: Control and interpolation strategy between optimal points.

look-up tables. Figure 5.10 is the graphical representation of the code. To further simplify, depending on the mode, one to three degrees of freedom should be interpolated. If $V_{bat} \notin \bar{V}_s$, then the portion of code represented at the center of Figure 5.10 is executed twice and a weighted average between the two solutions is chosen. α_{p1}, α_{p2}, α_{s1}, α_{s2}, θ_1 and θ_2 are the set of solutions evaluated during interpolation. θ_{off} should be set empirically: the idea consists of modulating just the internal phase shift θ between the two bridges based on the ratio between the requested power P_o and the closest greater value of the vector $P_{o,r}$. Basically, when the value of θ drops from one optimal point to the other of the look-up table, the described strategy is implemented. Instead, if the condition does not occur and the mode is 3 or 4, a full interpolation is made. The same goes for mode 5, with the exception $\bar{\theta}[v_{bat}][int(m)+1] < \bar{\theta}[v_{bat}][int(m)]$, in this case α_s is not interpolated. Consider $v_{bat} : \{\bar{V}_s[v_{bat}] \leq V_{bat} \quad \& \quad \bar{V}_s[v_{bat}+1] > V_{bat}\}$. With just one voltage sensor, the resonant CLLC converter can be precisely controlled in open-loop by an FPGA or a commercial microcontroller. A HIL (Hardware In the Loop) simulation in subsection 5.5, demonstrates the statement on a SMT32G474RE microcontroller. In subsection 5.6, experimental tests are instead carried out on real hardware.

5.5 Simulation results

This subsection is divided between an offline simulation, carried out in PLECS and a HIL simulation, that employed a SMT32G474RE nucleo board and RT Box 3.

5.5.1 PLECS offline simulations

Simulations of the CLLC resonant DAB converter have been carried out on PLECS. In Figure 5.11, the converter schematic is shown. Modulator subsystem only contains the control strategy explained in the previous subsection. If modulation = 1 is selected, the AVC modulator is activated, otherwise if modulation = 2 is selected, the TPS modulation is chosen. The converter parameters are summarized in Table 5: parasitic elements, including transformer ratio and magnetizing inductance, were chosen based on available passive components. It is not explicit, but $L_{f1} = L_{f2}$ and $C_{f1} = C_{f2}$ and the output power range is valid for forward and reverse power transfer.

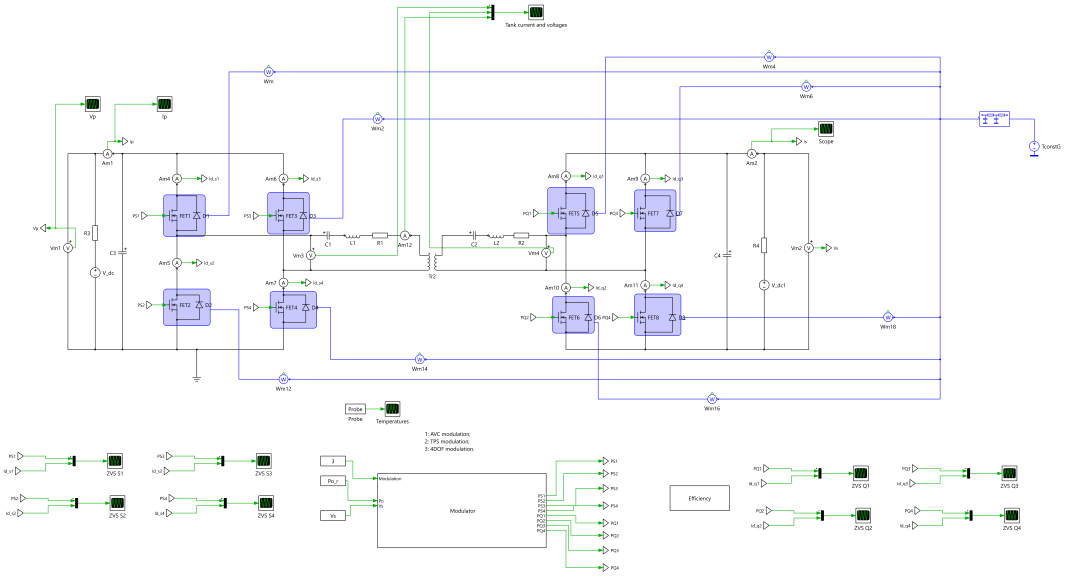

Figure 5.11: CLLC Resonant DAB schematic in PLECS.

In the next figures, the resulting waveforms for forward and reverse power transfer are shown in comparison between the AVC, TPS and a four degree of freedom modulation (4DOF) modulation, presented in [17]. Figure 5.12 and Figure 5.15 both refer to the proposed modulation, Figure 5.13 and Figure 5.16 to the TPS modulation and finally Figure 5.14 and Figure 5.17 refer to 4DOF modulation with variable switching frequency.

Table 5.5: CLLC Resonant DAB converter parameters.

Parameter	Symbol	Value
Rectified primary voltage	V_p	$230\sqrt{2}$ V
Battery voltage range	V_s	250 ÷ 400 V
Output power range	P_o	4 ÷ 14 kW
Transformer ratio	n	1
Magnetizing inductance	L_m	5.266 mH
Resonant inductance	L_{f1}	8.1 µH
Resonant capacitor	C_{f1}	330 nF
Resonant frequency	f_r	∼ 97.35 kHz
Fixed switching frequency	f_{sw}	122 kHz

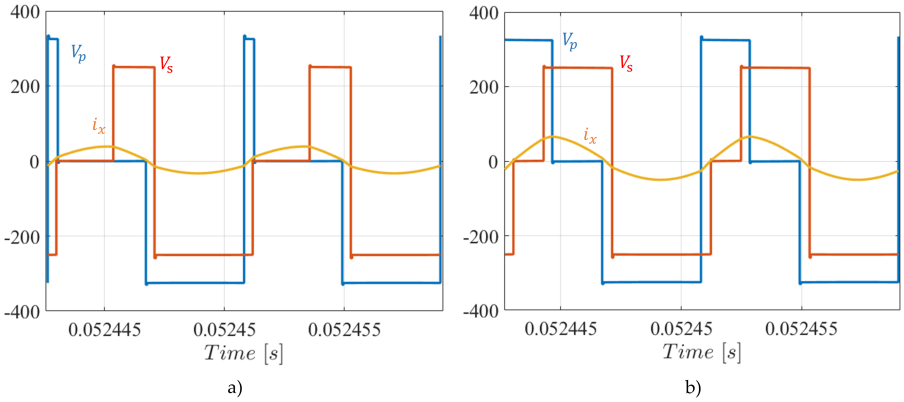

Figure 5.12: Double AVC modulation. Battery charging (250 V) from the grid: a) at 4 kW and b) at 8 kW. FB1 output voltage (blue), FB2 output voltage (red) and current in the resonant tank (yellow, $I_{rms} = 26.55$ A_{rms} and $I_{rms} = 41.2$ A_{rms}).

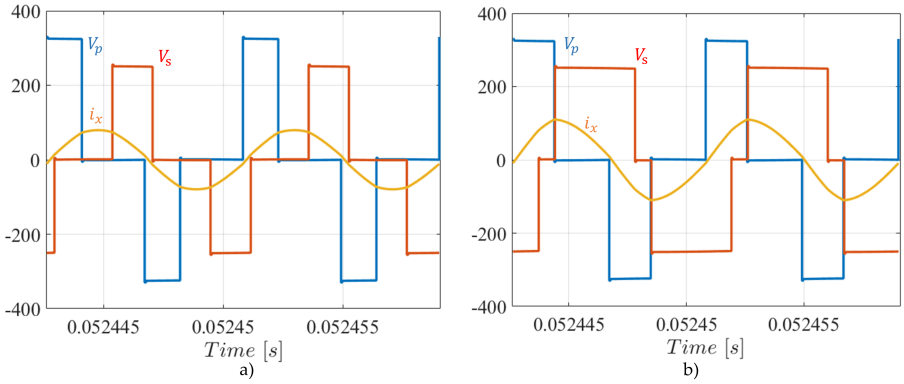

Figure 5.13: TPS modulation. Battery charging (250 V) from the grid: a) at 4 kW and b) at 8 kW. FB1 output voltage (blue), FB2 output voltage (red) and current in the resonant tank (yellow, $I_{rms} = 57.48$ A_{rms} and $I_{rms} = 74.87$ A_{rms}).

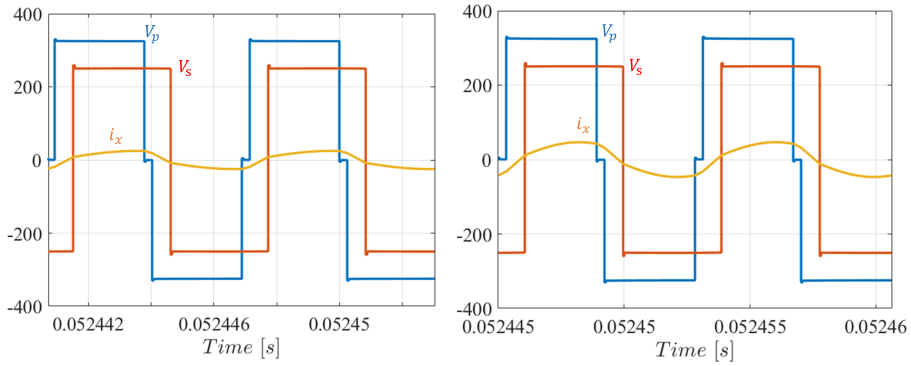

Figure 5.14: 4DOF modulation. Battery charging (250 V) from the grid: a) at 4 kW and b) at 8 kW. FB1 output voltage (blue), FB2 output voltage (red) and current in the resonant tank (yellow, $I_{rms} = 35.19$ A_{rms} and $I_{rms} = 18.77$ A_{rms}).

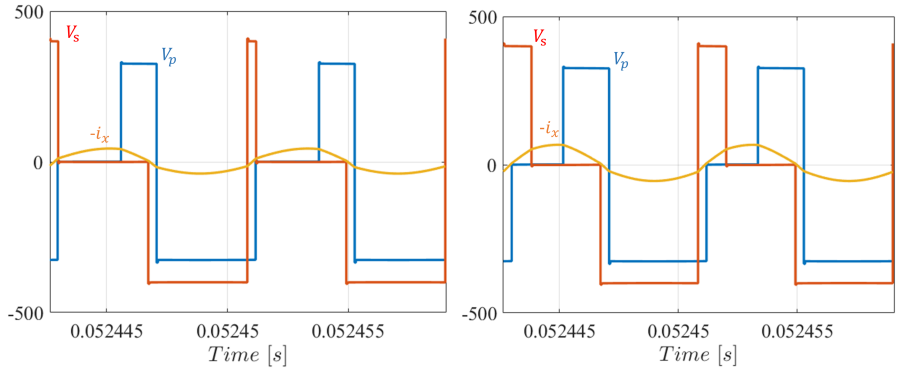

Figure 5.15: Double AVC modulation. Battery discharging (400 V): a) at 5.4 kW and b) 8.5 kW. FB1 output voltage (blue), FB2 output voltage (red) and current in the resonant tank (yellow, $I_{rms} = 31.18$ A_{rms} and $I_{rms} = 45.00$ A_{rms}).

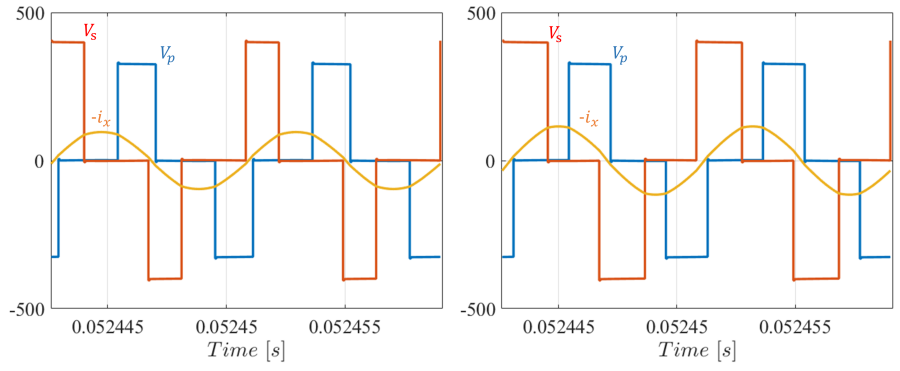

Figure 5.16: TPS modulation. Battery discharging (400 V): a) at 5.4 kW and b) 8.5 kW. FB1 output voltage (blue), FB2 output voltage (red) and current in the resonant tank (yellow, $I_{rms} = 70$ A_{rms} and $I_{rms} = 87.46$ A_{rms}).

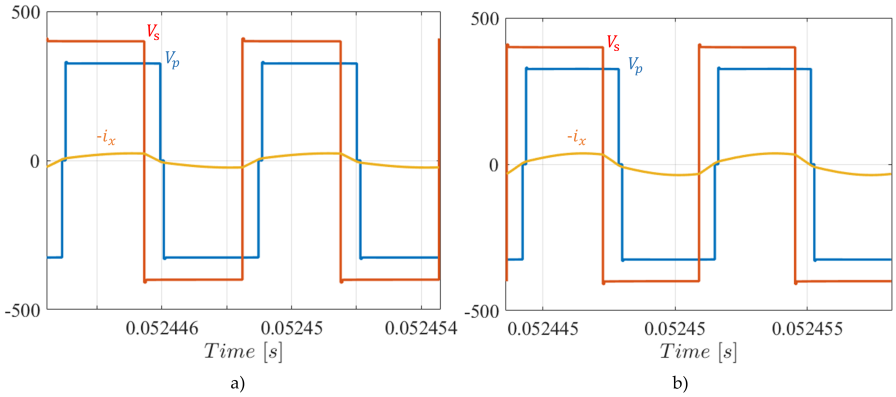

Figure 5.17: 4DOF modulation. Battery discharging (400 V): a) at 5.4 kW and b) 8.5 kW. FB1 output voltage (blue), FB2 output voltage (red) and current in the resonant tank (yellow, $I_{rms} = 18.22$ A_{rms} and $I_{rms} = 28.33$ A_{rms}).

5.5.2 HIL simulations

Hardware In the Loop (HIL) simulations have been carried out with the purpose of validating the control technique of the converter on a commercial MCU (microcontroller), employing code generation. A STM32G474RE nucleo board has been programmed with PLECS Coder while simulating the converter model on the RT Box 3. The converter is simulated through the Flex Array feature; therefore, it runs on the FPGA, Xilinx Zynq Ultrascale+ ZU9EG, inside the Box. PWM signals are injected by four high-resolution timers (HRTIM) driven by the same master on the MCU. Due to the current limitations of the hardware, all passive components were scaled to have a switching frequency of 20 kHz. The control routine runs at 10 kHz in open-loop, which is fast enough to trace any variation in power output demand, under reasonable operating conditions. Setup is shown in Figure 5.18. The exact same control summarized in Figure 5.10 was implemented on the microcontroller.

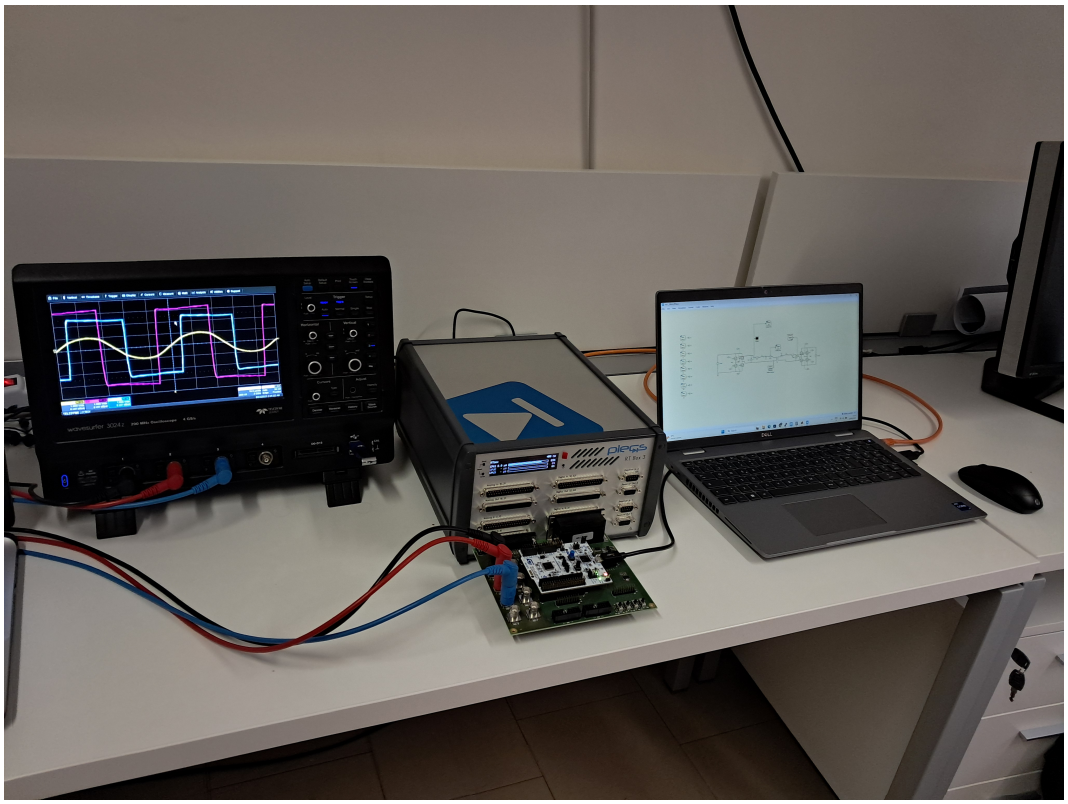

Figure 5.18: HIL simulation of the Resonant DAB CLLC converter.

Figure 5.19 and Figure 5.20 show the behavior of the converter under a load variation, in this case for forward power transfer, but the same consideration can be made for reverse power transfer. All waveforms detected on the oscilloscope should be scaled according to the descriptions of the figure, since these signals are provided by the Analog Outputs of the RT Box and thus limited to the range $[-10, +10]$ V. In 500 µs the transition is fully achieved: ZVS is not satisfied for all switches, only during this period.

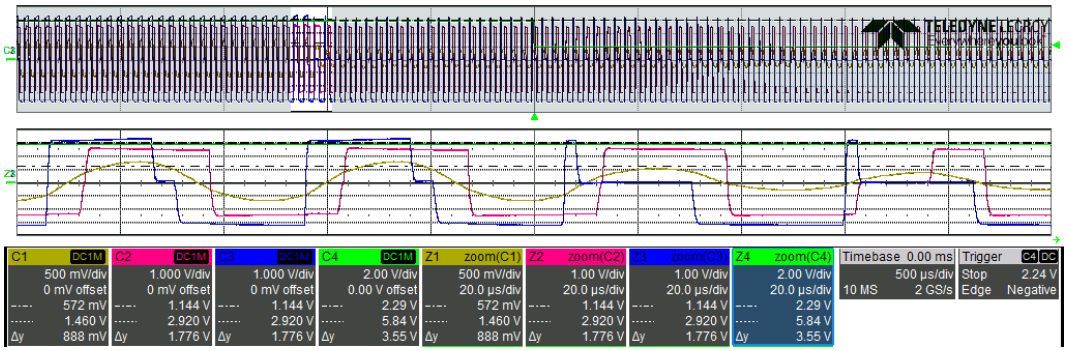

Figure 5.19: Battery charge: transition from 12 kW to 4 kW power (modulation transition). FB1 output voltage (blue), FB2 output voltage (pink), current in the resonant tank (yellow) and output power (green). Scales are: 1:100 for the output voltages and current and 1:2000 for the average output power.

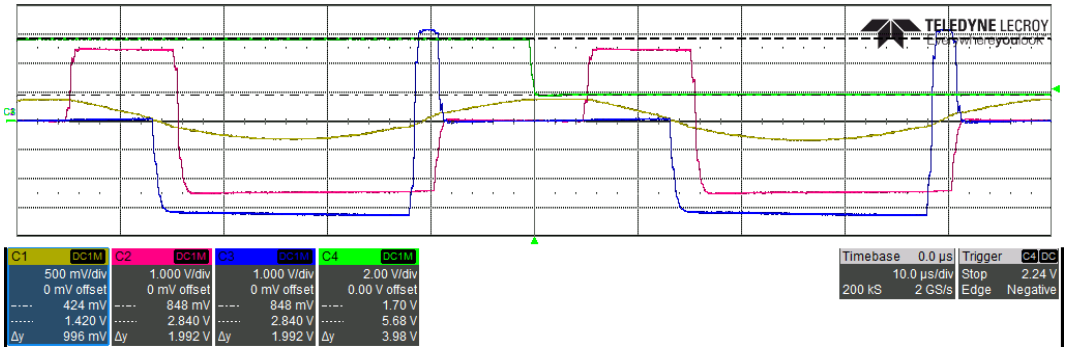

Figure 5.20: Battery charge: transition from 12 kW to 4 kW power (output power transition). FB1 output voltage (blue), FB2 output voltage (pink), current in the resonant tank (yellow) and output power (green). Scales are: 1:100 for the output voltages and current and 1:2000 for the average output power.

The purpose of the HIL dissertation is limited to applicability on a commercial MCU and should not be intended as a substitute for the validation of the proposed modulation on real hardware. Therefore, in the following subsection, experimental tests have been carried out at the switching frequency of the offline simulation and on a real converter. Furthermore, different modulations have been compared in the following.

5.6 Experimental results

Offline simulations described in subsection 5.5 are meant to replicate the experimental tests described here. Of course ringing effects and true ZVS for the switches can only be proven having the real waveforms. Some operating points are shown here for the three modulation techniques: double AVC, TPS and 4DOF [17]. In Table 5.6, details of the experimental setup are shown.

The experimental tests setup is shown in Figure 5.21, control board is under the converter. Control and modulation were implemented on the FPGA SoC Zynq 7000 on VHDL. As demonstrated in subsection 5.5, control and modulation can also be implemented on a commercial MCU. In Figure 5.21, the experimental setup is presented: two full bridges are visible on the right along with two power supplies on the left. Transformer, additional resonant inductances and resonant capacitors are external. The control board instead is under the converter. The experimental waveforms are summarized in Figures 5.22-5.27. Those figures represent two operating points (one for battery charge and one for battery discharge): the maximum output power is not shown here, because every modulation technique would tend to the condition

Table 5.6: Main variables and parameters of the experimental tests.

Parameter	Symbol	Part number	Value
Rectified primary voltage	V_p	/	$230\sqrt{2}$ V
Battery voltage range	V_s	/	250, 400 V
Output power range	P_o	/	$4 \div 14$ kW
Transformer ratio	n	/	1
Magnetizing inductance	L_m	/	5.266 mH
Leakage inductance	L_{lk}	/	3.85 µH
Resonant additional inductance	L_{f1}	/	4.25 µH
Resonant capacitor	C_{f1}	CSM 150	330 nF
Resonant frequency	f_r	/	$\sim$ 97.35 kHz
2 parallel SiC MOSFETs	/	C3M0040120K	/
SoC FPGA	/	Zynq 7000	/
Fixed switching frequency (AVC & TPS)	f_{sw}	/	122 kHz
Variable switching frequency (4DOF)	f_{sw}	/	$128 - 165$ kHz

$\theta = \pi/2$, $\alpha_p = \alpha_s = 0$. Therefore, the difference in terms of the RMS current and efficiency would be minimal. It is clear from the tests that the double AVC modulation improves the efficiency and reduces the tank current with respect to the TPS modulation at fixed frequency. The four degree of freedom modulation, 4DOF, allows even lower tank currents, even though the operating frequency has been selected manually by means of trials and errors to reach ZVS and required output power: converter control is instead much easier implementing the double AVC modulation and for even larger power ranges, transformer would not operate at its optimal frequency range.

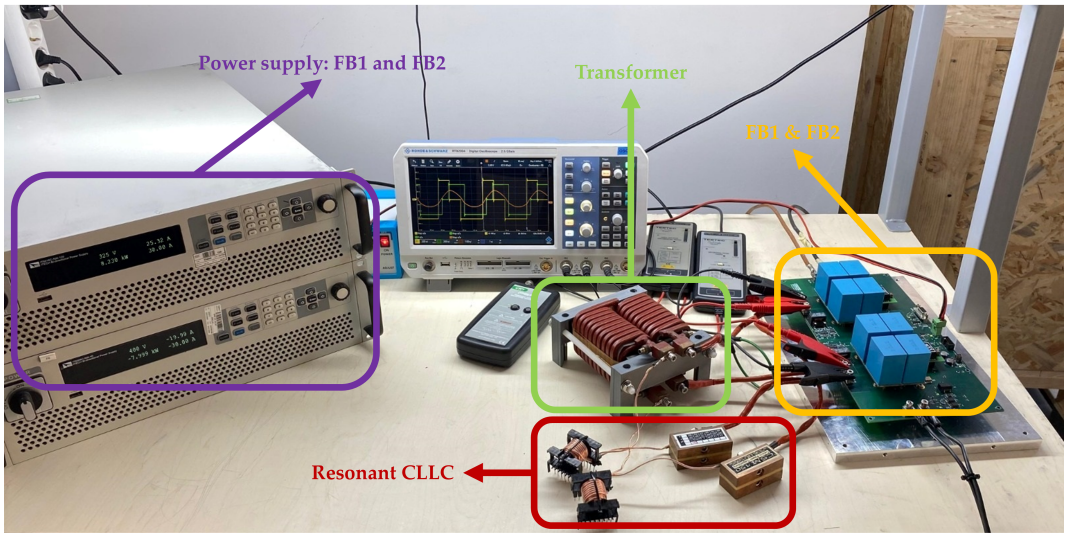

Figure 5.21: Experimental setup: full-bridges, resonant capacitors, transformer, additional resonant inductors and two bidirectional power supplies. Control board is under the converter.

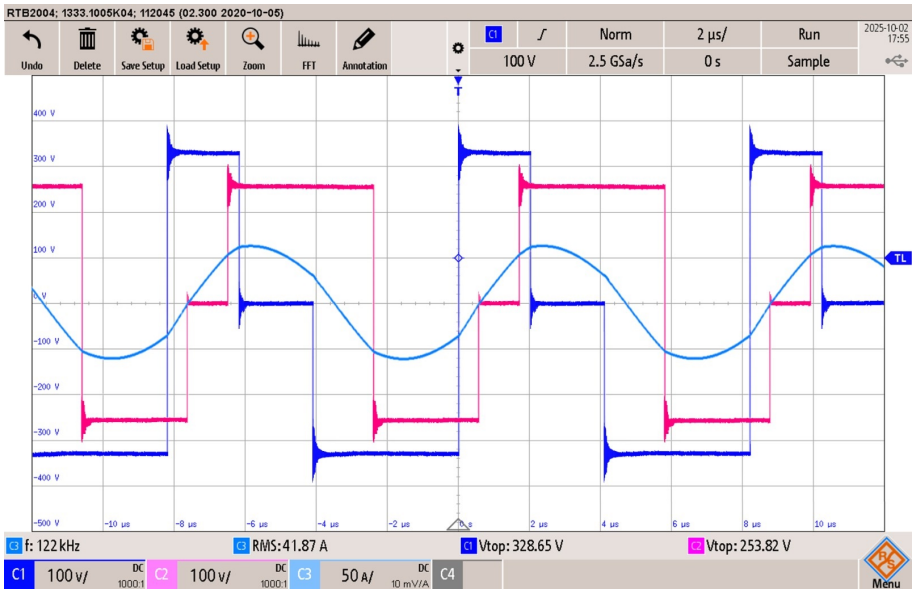

Figure 5.22: Double AVC modulation, battery charge at 8 kW: FB1 output voltage (blue trace), FB2 output voltage (pink trace) and resonant tank current (light blue), $\eta = 96.3$ %.

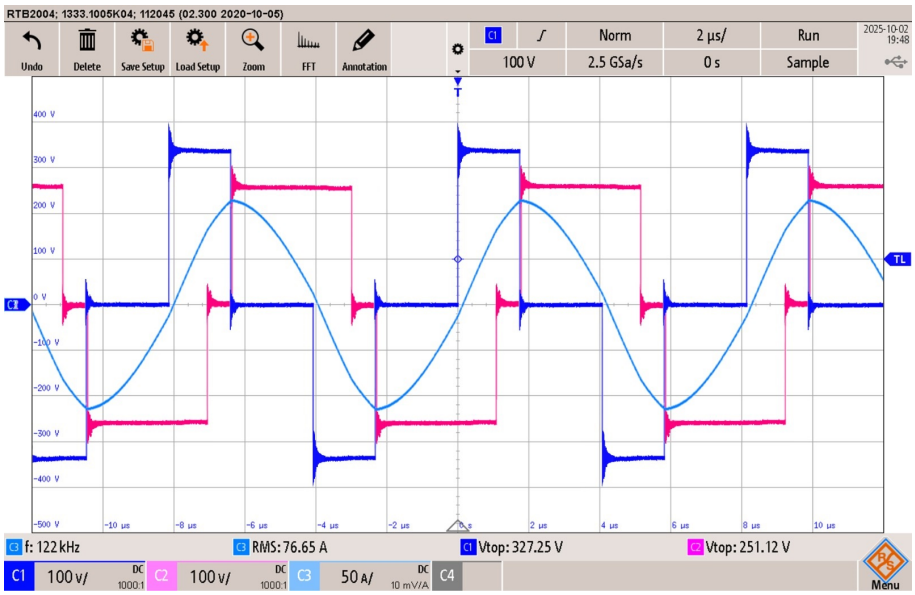

Figure 5.23: TPS modulation, battery charge at 8 kW: FB1 output voltage (blue trace), FB2 output voltage (pink trace) and resonant tank current (light blue), $\eta = 91.5$ %.

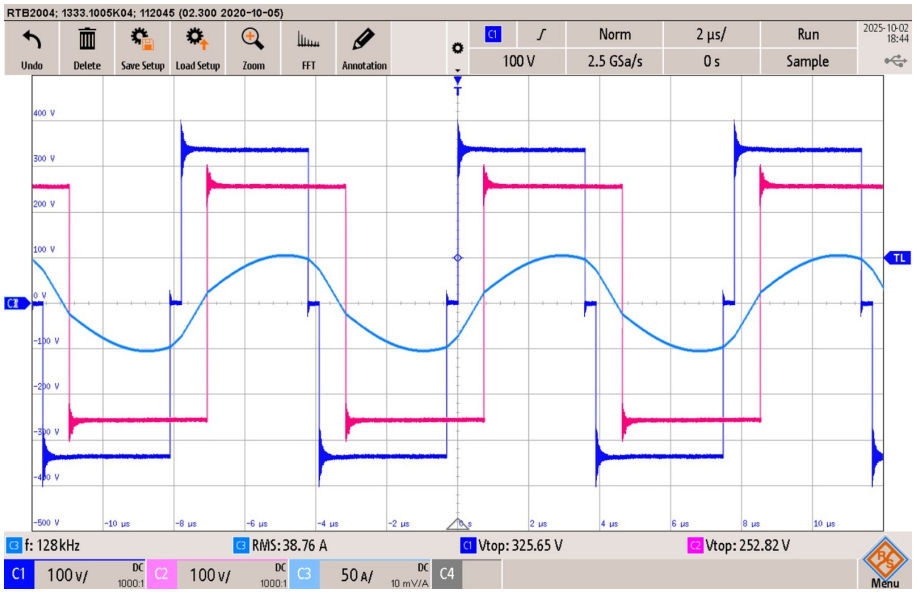

Figure 5.24: 4DOF modulation, battery charge at 8 kW: FB1 output voltage (blue trace), FB2 output voltage (pink trace) and resonant tank current (light blue), $\eta = 97.2$ %.

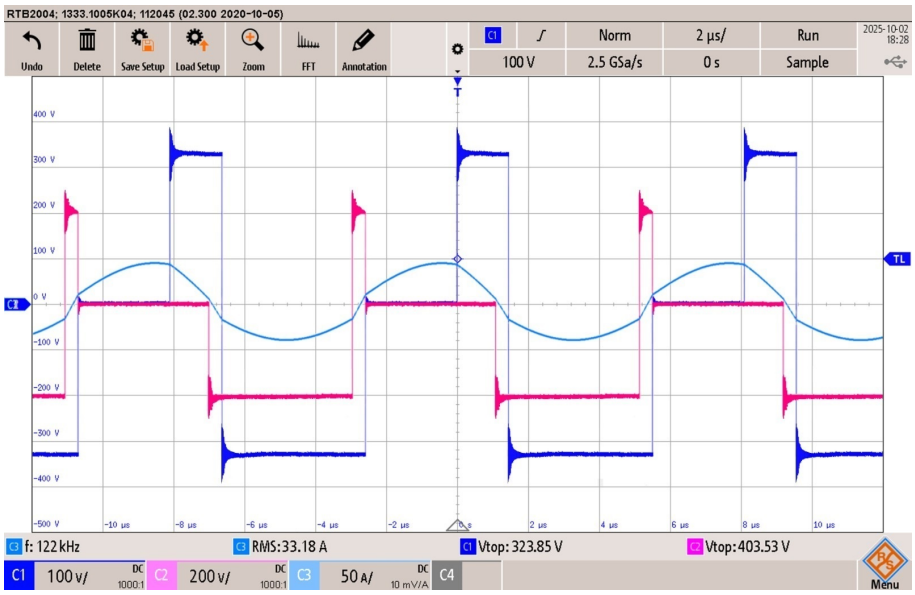

Figure 5.25: Double AVC modulation, battery discharge at 5.5 kW: FB1 output voltage (blue trace), FB2 output voltage (pink trace) and resonant tank current (light blue), $\eta = 96.8$ %.

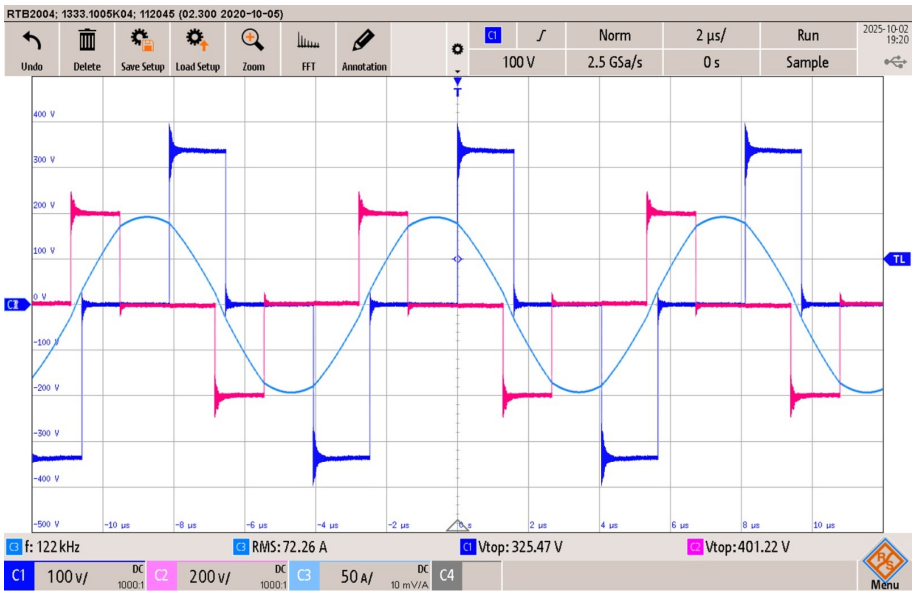

Figure 5.26: TPS modulation, battery discharge at 5.5 kW: FB1 output voltage (blue trace), FB2 output voltage (pink trace) and resonant tank current (light blue), $\eta = 87.7$ %.

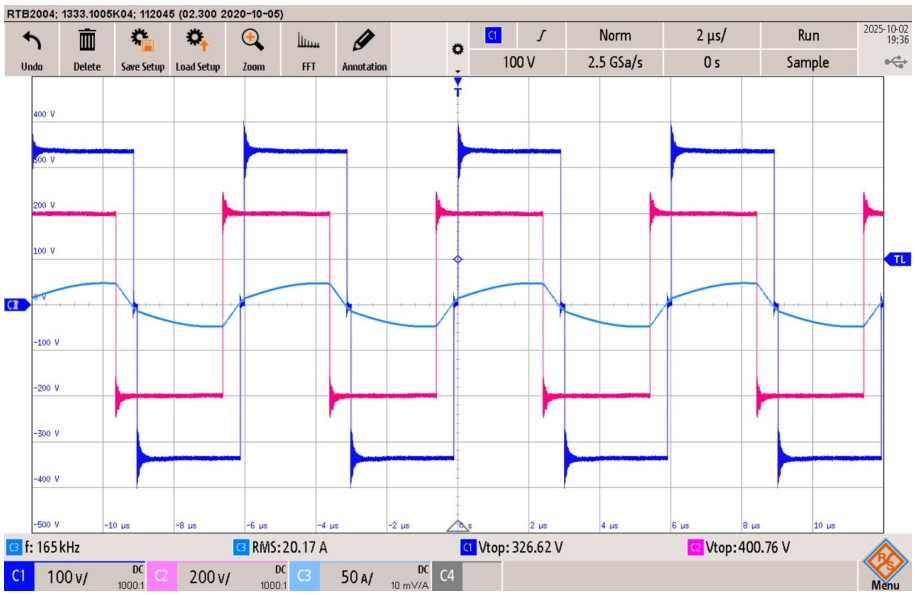

Figure 5.27: 4DOF modulation, battery discharge at 5.5 kW: FB1 output voltage (blue trace), FB2 output voltage (pink trace) and resonant tank current (light blue), $\eta = 97.4$ %.

The double asymmetric modulation technique was proposed and described in this paper. Since it was compared to two other existing techniques, TPS and 4DOF, the following table summarizes the differences both in qualitative and quantitative terms. The efficiency in the simulations, reported in Table 5.7, has been calculated as in [22] and does not account for the transformer losses: estimating the transformer losses is indeed very challenging and beyond the scope of this work. The discrepancy between the experimental tests and simulation results can be attributed to the neglect of the aforementioned losses. However, simulations have been found to comply with the results found during the experimental tests and the switching losses analysis suggests quantification of MOSFETs power losses. The simulated $I_{x,rms}$ is very similar to the one measured experimentally.

5.7 Conclusions

An innovative modulation technique for a CLLC Resonant DAB was presented in comparison with two existing modulation techniques in the literature: TPS and 4DOF. These modulations allow us to enhance the efficiency with respect to a traditional fixed frequency modulation, while keeping a very good controllability of the converter. Choosing a fixed frequency, rather than variable frequency, like the 4DOF allows us to size a transformer for a specific frequency, rather than a wide range. Furthermore, it avoids the employment of expensive and complex

Table 5.7: Comparison of the three modulation techniques.

KPI	TPS	4DOF	Double AVC
Symmetry	Yes	Yes	No
Switching frequency [kHz]	122 (fixed)	113.5 – 165 (variable)	122 (fixed)
Control	Easy	Hard	Easy
Sim. $I_{x,rms}$ [A_{rms}]	74.87 (8 kW)	35.11 (8 kW)	41.2 (8 kW)
	70.0 (−5.5 kW)	18.22 (−5.5 kW)	31.8 (−5.5 kW)
Sim. η [%]	92.65 (+8 kW)	97.4 (+8 kW)	97.1 (+8 kW)
	89.65 (−5.5 kW)	96.8 (−5.5 kW)	96.6 (−5.5 kW)
Sim. $I_{x,rms}$ [A_{rms}]	76.65 (8 kW)	38.76 (8 kW)	41.87 (8 kW)
	72.26 (−5.5 kW)	20.17 (−5.5 kW)	33.18 (−5.5 kW)
Exp. η [%]	91.5 (+8 kW)	97.2 (+8 kW)	96.3 (+8 kW)
	87.7 (−5.5 kW)	97.4 (−5.5 kW)	96.8 (−5.5 kW)

EMI/EMC additional filters and allows reducing the switching losses of the transistors. With this modulation, efficiencies are kept very high, and it is believed that further improvements are possible. The control can be implemented easily on a commercial microcontroller, and that was demonstrated by the code generation on a STM32G474RE. An open-loop control with selective interpolation was found to be very effective in the HIL simulation. The same modulation was implemented on a SoC FPGA and was applied in comparison with the aforementioned techniques on a CLLC converter. Experimental tests showed a good compliance with the simulations, especially regarding the estimation of the RMS current flowing in tank. Among the experimental tests that made, an maximum efficiency of around 97 % was found. As a future development, authors are willing to further improve the modulation technique adding other degree of freedoms and adapting the control accordingly.

5.8 References

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Conclusions

The main contributions of this thesis are discussed here, and a few words are also given on the future work that the author is willing to carry-on. The projects the author worked on can appear very different from each other, since they refer to different converter topologies. However, all chapters are bonded to the main topic: the development of high-efficiency and reliable converter topologies based on WBG technology. At the end of each chapter, conclusions are defined and written strictly relating to the chapter itself; therefore, a summary is reported here and general conclusions are drawn.

Chapter 1 is the first work and represents the basis for the other works. Especially a SiC switching losses model based on available data from the manufacturers is developed. This is essential to obtain a good estimate of the losses in any power converter with WBG technology and correctly size the heat sink subsequently, not mentioning the great impact of one type of model or another on any reliability analysis based on the failure of the transistors. The model was proven to be effective, and in compliance with the experimental tests which have been carried out and relatively easy to implement. A comparison with well-known and recent models strengthens the statement. The merits of this specific work are also the change in the approach: efficiency measurement instead of energy-loss measurement and the introduction of the uncertainty of measures. The tests were carried out under different load conditions and different switching frequencies to have a good set of experimental tests on a half-bridge board. Surely, future work can be made on the exact temperature estimation and on the reliability analysis that would follow from this switching losses model. A further proof of the extensibility of the work would be to compare simulation results with tests made on different parts numbers.

Chapter 2 proposes a brief dissertation on photovoltaic inverters, because the development of a prototype was a task for the YESvGaN project, as well as the entire content of the first chapter. This work was paused because of the end of the project, and it is the one that requires most of the future work. As explained at the end of the chapter, the author is willing to carry out the main ideas: make a lifetime estimation of this PV inverter topology with respect to the most commonly used in the literature in order to prove or disprove the effectiveness of simplifying the architecture when using WBG converters; carry out experimental tests, since the board

had already been developed and inject power into the grid, emulating a typical mission profile of Emilia-Romagna.

Chapters 3 and 4 are both related to the Current Source Inverter architecture. The first one proposes the advantages in terms of current and torque ripple and THD %, that can be gained employing a CSI instead of VSI. The main issue of the efficiency can be mitigated by the presence of SiC MOSFETs and SiC Schottky diodes. A merit of the first one are also an accurate losses model of the ironless machine, that is validated throughout detailed experimental results and gives strength to the CSI-fed idea. The mathematical dissertation of the 2D-FEA model, employed to estimate the losses, in the middle of the chapter should also be considered a significant contribution to the literature. An idea to further extend the work would be the development of the CSI drive and its comparison with the VSI drive plus an LC output filter, in order to find the most efficient solution. The second work on CSI is related to the flux-weakening strategy for an IPM machine. Merits are the extension of the MTPA strategy over a wider speed-range and the conceptualization of an alternate modulation technique that mitigates the resonance problem. The same CSI board, which is part of a future work, could be used to validate the control strategy.

Chapter 5 is related to static conversion and especially in an on-board charger application. The main contribution of this chapter is the conceptualization of an innovative modulation technique for a resonant dual-active bridge. The new fixed frequency modulation was found to be more efficient than another one which exists in literature. A good merit of the model is the complete explanation of this technique along with the control strategy, which was tested in hardware in the loop and run on a commercial microcontroller. Experimental tests were carried out on real hardware and the effectiveness of this modulation was proved for some operating points. Because a variable frequency modulation is still more efficient, future work will concern the introduction of additional degrees of freedom in order to also match the efficiency of a variable frequency modulation, which anyway has several drawbacks, stated and explained in the chapter.

Overall, the thesis treated the theme of "Wide-bandgap based power converters for improved efficiency and reliability" on different converter topology, and the author hopes that at least one of these analyzes will have a good impact on the research and industrial field in the nearby future. Finally, lists of published and under revision works are reported here.

List of published works:

1. C. Bianchini, G. Sala, M. Frigieri, **M. Vogni**, N. Giannotta and E. Macrelli, "Extended MTPA-FW Control Technique for PM Electrical Machines with CSI". *2024 International Conference on Electrical Machines (ICEM)*, Torino, Italy, 2024, pp. 1-7, doi: 10.1109/ICEM60801.2024.10700071.

2. C. Bianchini, G. Sala, M. Frigieri, **M. Vogni**, N. Giannotta and A. Capitanio, "Inductance Based Lumped Parameter IPM Machine Model for Fast Simulation". *2024 IEEE Energy Conversion Congress and Exposition (ECCE)*, Phoenix, AZ, USA, 2024, pp. 5262-5268, doi: 10.1109/ECCE55643.2024.10861024.

3. G. Sala, C. Bianchini, **M. Vogni**, E. Macrelli and A. Bellini, "Current Source Inverter Drive of an Ironless Motor for Flywheel Batteries". *2024 IEEE Energy Conversion Congress and Exposition (ECCE)*, Phoenix, AZ, USA, 2024, pp. 354-358, doi: 10.1109/ECCE55643.2024.10861673.

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5. G. Sala, N. Giannotta, **M. Vogni**, C. Bianchini, and F. Immovilli. "Analytical Model and Feasibility Assessment of a Synchronous Reluctance Tubular Machine with an Additively Manufactured Mover". *Energies*, 2025, 18, 3918. https://doi.org/10.3390/en18153918.

6. **M. Vogni**, G. Sala, E. Macrelli, C. Bianchini and A. Bellini. "Comprehensive Load Loss Model of an Ironless Machine Demonstrating the Advantage of Current Source Inverter Supply". *IEEE Transaction on Industry Applications*, doi: 10.1109/TIA.2026.3656127.

7. **M. Vogni**, J. L. Bellido Ruiz, F. Stella, L. Stefanini, C. Bianchini and V. Esteve. "Application and Development of a Double Asymmetric Voltage Modulation on a Resonant Dual Active Bridge". *Electronics*, 2025, 14, 4625. https://doi.org/10.3390/electronics14234625

Of those, the second and fifth works were outside the scope of this thesis and therefore have

not been mentioned.

The following article was accepted, but not yet published. It is related to traditional Silicon devices and, therefore, is out of the scope of the thesis.

- D. Anchieri, **M. Vogni**, D. David, M. Ricco, and R. Mandrioli. "Three-Layer Stacked PCB Design of a Low-Voltage High-Current Inverter for Motorsport Applications". Accepted on *IEEE iEnergy*.